



**2x2Mx16 5V FLASH MODULE** *ADVANCED\**

**FEATURES**

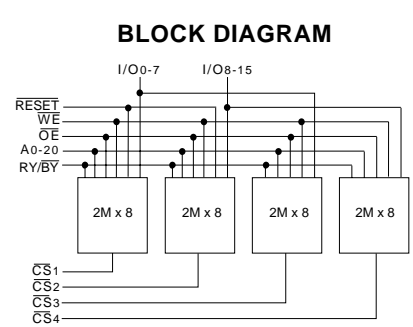
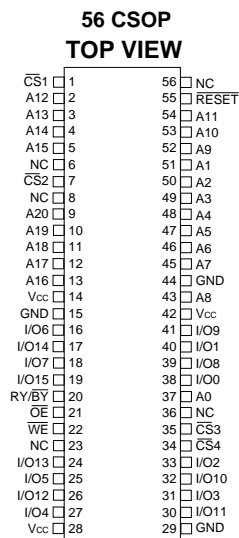
- Access Time of 90, 120, 150ns
- Packaging:
  - 56 Lead, Hermetic Ceramic, 0.520" CSOP (Package 213). Fits standard 56 SSOP footprint.
- Sector Architecture
  - 32 equal size sectors of 64KBytes per each 2Mx8 chip
  - Any combination of sectors can be erased. Also supports full chip erase.
- Minimum 100,000 Write/Erase Cycles Minimum
- Organized as two banks of 2Mx16; User Configurable as 4 x 2Mx8
- Commercial, Industrial, and Military Temperature Ranges
- 5 Volt Read and Write. 5V ±10% Supply.
- Low Power CMOS

- Data Polling and Toggle Bit feature for detection of program or erase cycle completion.
- Supports reading or programming data to a sector not being erased.
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation, Separate Power and Ground Planes to improve noise immunity
- $\overline{\text{RESET}}$  pin resets internal state machine to the read mode.
- Ready/Busy (RY/BY) output for direction of program or erase cycle completion.

*\* This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

*Note: For programming information refer to Flash Programming 16M5 Application Note.*

**FIG. 1 PIN CONFIGURATION FOR WF4M16-XDTX5**



**PIN DESCRIPTION**

I/O0-15	Data Inputs/Outputs
A0-20	Address Inputs
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CS}}_{1-4}$	Chip Selects
$\overline{\text{OE}}$	Output Enable
Vcc	Power Supply
GND	Ground
RY/ $\overline{\text{BY}}$	Ready/Busy
RESET	Reset

- NOTE:**
1. RY/BY is an open drain output and should be pulled-up to Vcc with an external resistor.
  2.  $\overline{\text{CS}}_1$  and  $\overline{\text{CS}}_3$  control the same data bus. Reads cannot be done with  $\overline{\text{CS}}_1$  and  $\overline{\text{CS}}_3$  both active.  $\overline{\text{CS}}_2$  and  $\overline{\text{CS}}_4$  control the same data bus. Reads cannot be done with  $\overline{\text{CS}}_2$  and  $\overline{\text{CS}}_4$  both active.
  3. Address compatible with Intel 2M8 56 SSOP.



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to Vss	V <sub>I</sub>	-2.0 to +7.0	V
Power Dissipation	P <sub>T</sub>	8	W
Storage Temperature	T <sub>stg</sub>	-65 to +125	°C
Short Circuit Output Current	I <sub>os</sub>	100	mA
Endurance - Write/Erase Cycles (Mil Temp)		100,000 min	cycles
Data Retention (Mil Temp)		20	years

**CAPACITANCE**

(T<sub>A</sub> = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C <sub>OE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	45	pF
$\overline{WE}$ capacitance	C <sub>WE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	45	pF
$\overline{CS}$ capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	15	pF
Data I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V, f = 1.0 MHz	25	pF
Address input capacitance	C <sub>AD</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	45	pF

This parameter is guaranteed by design but not tested.

**RECOMMENDED DC OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Ground	V <sub>SS</sub>	0	0	V
Input High Voltage	V <sub>IH</sub>	2.0	V <sub>CC</sub> + 0.5	V
Input Low Voltage	V <sub>IL</sub>	-0.5	+0.8	V
Operating Temperature (Mil.)	T <sub>A</sub>	-55	+125	°C
Operating Temperature (Ind.)	T <sub>A</sub>	-40	+85	°C

**DC CHARACTERISTICS - CMOS COMPATIBLE**

(V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10	μA
Output Leakage Current	I <sub>LOx32</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10	μA
V <sub>CC</sub> Active Current for Read (1)	I <sub>CC1</sub>	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}, f = 5\text{MHz}, V_{CC} = 5.5$		82	mA
V <sub>CC</sub> Active Current for Program or Erase (2)	I <sub>CC2</sub>	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}, V_{CC} = 5.5$		122	mA
V <sub>CC</sub> Standby Current	I <sub>CC3</sub>	V <sub>CC</sub> = 5.5, $\overline{CS} = V_{IH}, f = 5\text{MHz}$		8.0	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 12.0 mA, V <sub>CC</sub> = 4.5		0.45	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -2.5 mA, V <sub>CC</sub> = 4.5	0.85xV <sub>CC</sub>		V
Low V <sub>CC</sub> Lock-Out Voltage	V <sub>LKO</sub>		3.2	4.2	V

**NOTES:**

- The I<sub>CC</sub> current listed includes both the DC operating current and the frequency dependent component (@ 5MHz). The frequency component typically is less than 2mA/MHz, with  $\overline{OE}$  at V<sub>IH</sub>.
- I<sub>CC</sub> active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions V<sub>IL</sub> = 0.3V, V<sub>IH</sub> = V<sub>CC</sub> - 0.3V



**AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS - WE CONTROLLED**

(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>AVAV</sub>	t <sub>WC</sub>	90		120		150		ns
Chip Select Setup Time	t <sub>ELWL</sub>	t <sub>CS</sub>	0		0		0		ns
Write Enable Pulse Width	t <sub>WLWH</sub>	t <sub>WP</sub>	45		50		50		ns
Address Setup Time	t <sub>AVWL</sub>	t <sub>AS</sub>	0		0		0		ns
Data Setup Time	t <sub>DVWH</sub>	t <sub>DS</sub>	45		50		50		ns
Data Hold Time	t <sub>WHDX</sub>	t <sub>DH</sub>	0		0		0		ns
Address Hold Time	t <sub>WLAX</sub>	t <sub>AH</sub>	45		50		50		ns
Write Enable Pulse Width High	t <sub>WHWL</sub>	t <sub>WPH</sub>	20		20		20		ns
Duration of Byte Programming Operation (1)	t <sub>WHWH1</sub>			300		300		300	μs
Sector Erase (2)	t <sub>WHWH2</sub>			15		15		15	sec
Read Recovery Time before Write	t <sub>GHWL</sub>		0		0		0		μs
V <sub>CC</sub> Setup Time	t <sub>VCS</sub>		50		50		50		μs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		t <sub>OEH</sub>	10		10		10		ns

**NOTES:**

1. Typical value for t<sub>WHWH1</sub> is 7μs.
2. Typical value for t<sub>WHWH2</sub> is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

**AC CHARACTERISTICS – READ-ONLY OPERATIONS**

(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>AVAV</sub>	t <sub>RC</sub>	90		120		150		ns
Address Access Time	t <sub>AVQV</sub>	t <sub>ACC</sub>		90		120		150	ns
Chip Select Access Time	t <sub>ELQV</sub>	t <sub>CE</sub>		90		120		150	ns
Output Enable to Output Valid	t <sub>GLQV</sub>	t <sub>OE</sub>		40		50		55	ns
Chip Select High to Output High Z (1)	t <sub>EHOZ</sub>	t <sub>DF</sub>		20		30		35	ns
Output Enable High to Output High Z (1)	t <sub>GHOZ</sub>	t <sub>DF</sub>		20		30		35	ns
Output Hold from Addresses, CS or OE Change, whichever is First	t <sub>AXOX</sub>	t <sub>OH</sub>	0		0		0		ns

1. Guaranteed by design, not tested.



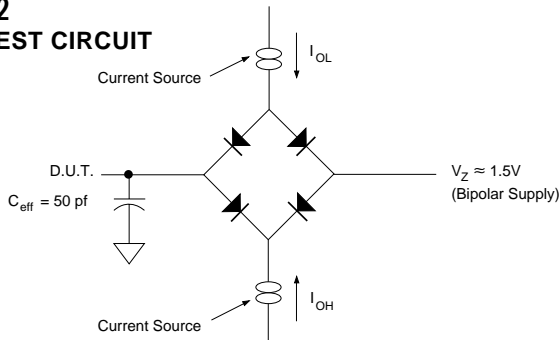
**AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS,  $\overline{CS}$  CONTROLLED**  
 ( $V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55^{\circ}C$  to  $+125^{\circ}C$ )

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	90		120		150		ns
Write Enable Setup Time	tWLEL	tWS	0		0		0		ns
Chip Select Pulse Width	tELEH	tCP	45		50		50		ns
Address Setup Time	tAVEL	tAS	0		0		0		ns
Data Setup Time	tDVEH	tDS	45		50		50		ns
Data Hold Time	tEHDX	tDH	0		0		0		ns
Address Hold Time	tELAX	tAH	45		50		50		ns
Chip Select Pulse Width High	tEHEL	tCPH	20		20		20		ns
Duration of Byte Programming Operation (1)	tWHWH1			300		300		300	$\mu$ s
Sector Erase Time (2)	tWHWH2			15		15		15	sec
Read Recovery Time	tGHEL		0		0		0		$\mu$ s
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		tOEH	10		10		10		ns

**NOTES:**

1. Typical value for tWHWH1 is 7 $\mu$ s.
2. Typical value for tWHWH2 is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

**FIG. 2**  
**AC TEST CIRCUIT**



**AC TEST CONDITIONS**

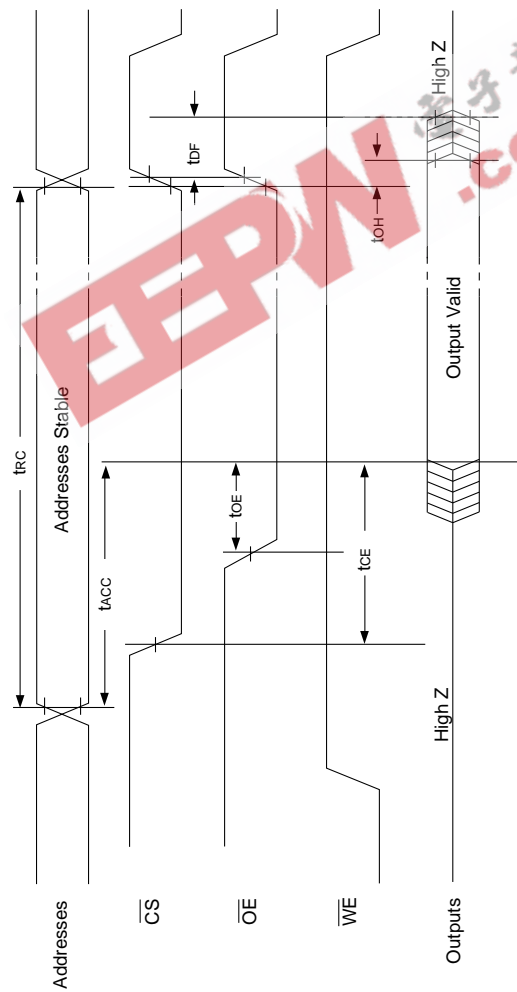
Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

**NOTES:**

$V_Z$  is programmable from -2V to +7V.  
 $I_{OL}$  &  $I_{OH}$  programmable from 0 to 16mA.  
 Tester Impedance  $Z_0 = 75 \Omega$ .  
 $V_Z$  is typically the midpoint of  $V_{OH}$  and  $V_{OL}$ .  
 $I_{OL}$  &  $I_{OH}$  are adjusted to simulate a typical resistive load circuit.  
 ATE tester includes jig capacitance.

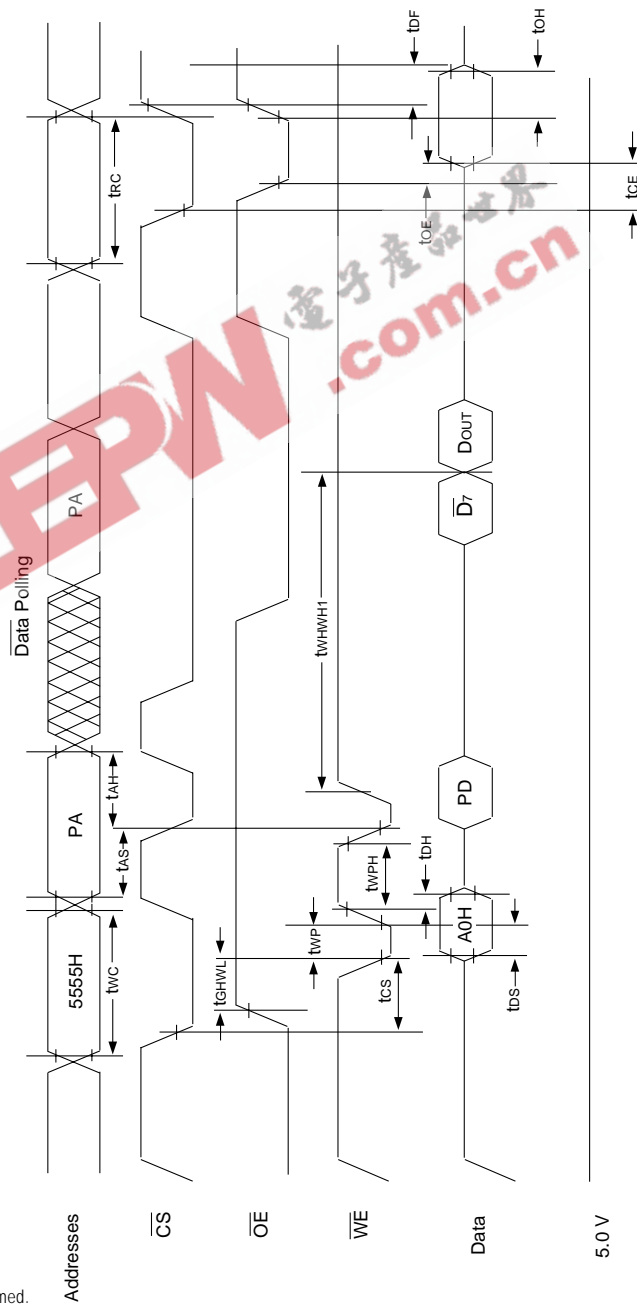


FIG. 3  
AC WAVEFORMS FOR READ OPERATIONS





**FIG. 4**  
**WRITE/ERASE/PROGRAM**  
**OPERATION, WE CONTROLLED**

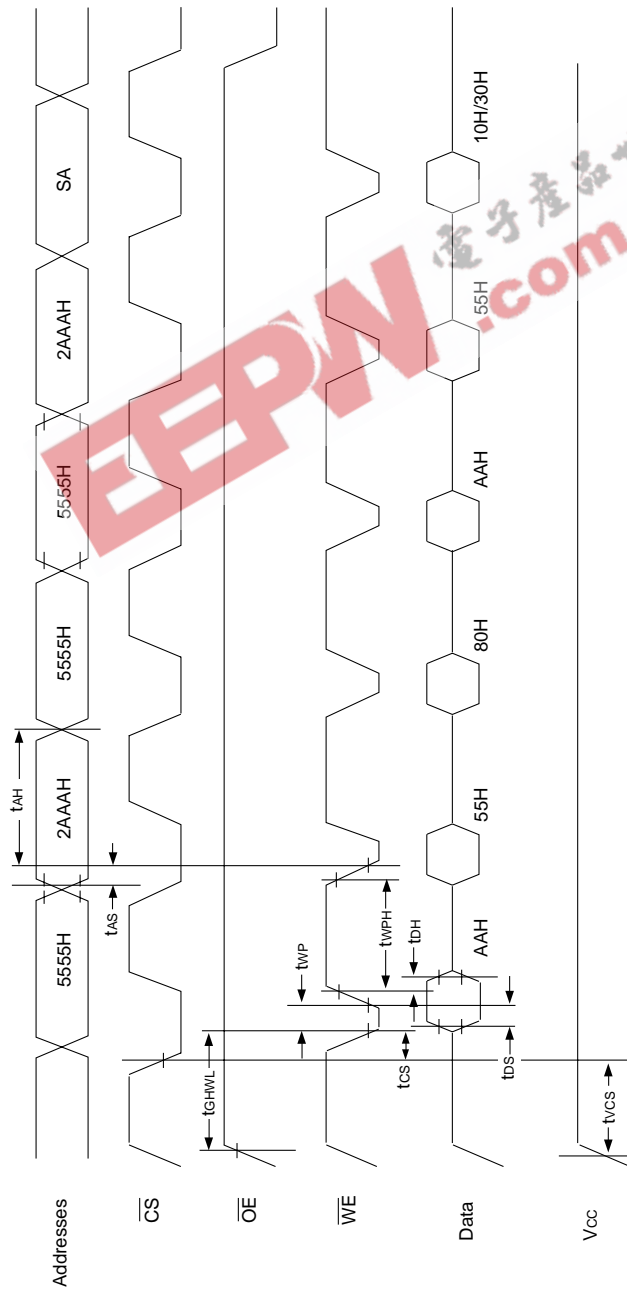


**NOTES:**

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7 is the output of the complement of the data written to each chip.
4. Dout is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.



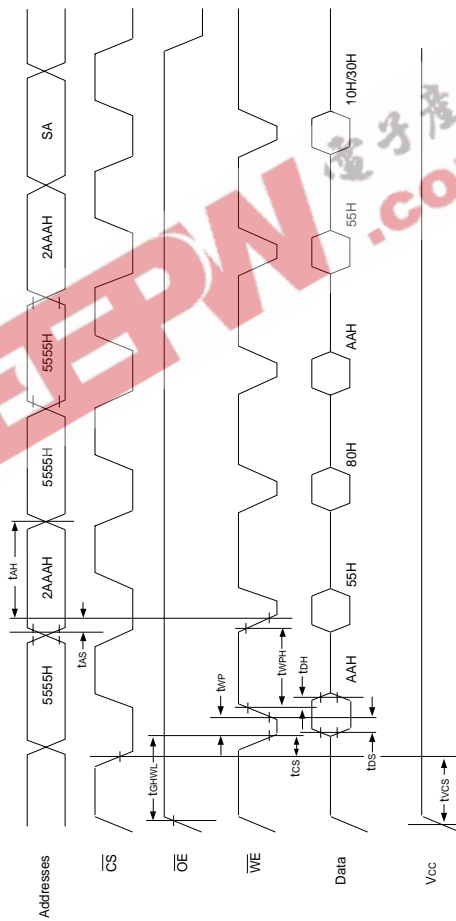
FIG. 5  
AC WAVEFORMS CHIP/SECTOR  
ERASE OPERATIONS



NOTE:  
1. SA is the sector address for Sector Erase.



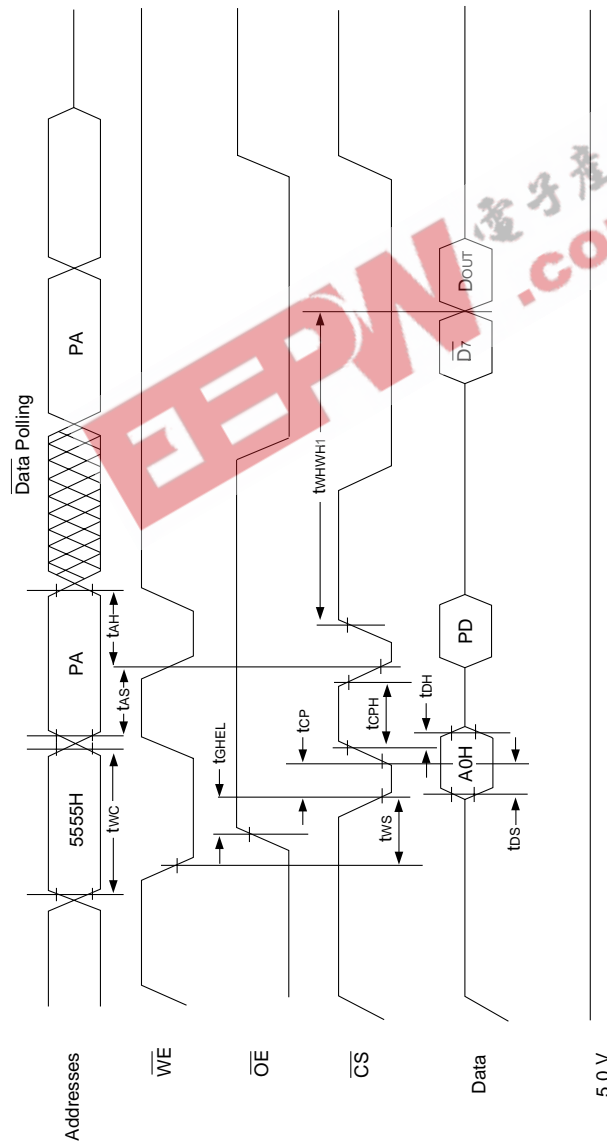
FIG. 6  
AC WAVEFORMS FOR DATA POLLING  
DURING EMBEDDED ALGORITHM OPERATIONS







**FIG. 7**  
**ALTERNATE  $\overline{CS}$  CONTROLLED**  
**PROGRAMMING OPERATION TIMINGS**

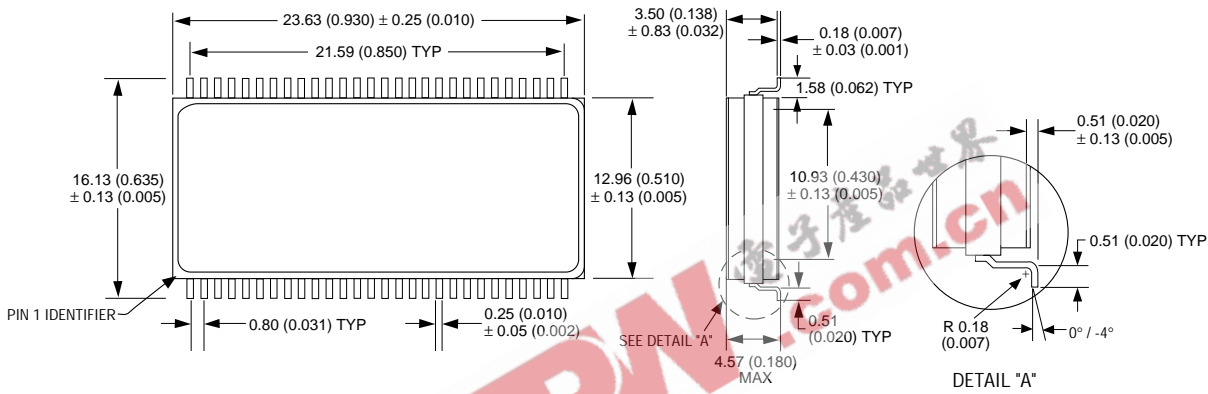


**NOTES:**

1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3.  $\overline{D7}$  is the output of the complement of the data written to each chip.
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.



PACKAGE 213: 56 LEAD, DUAL CAVITY CERAMIC SOP



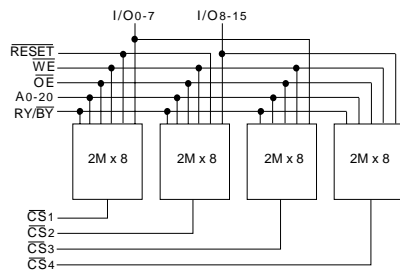
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

FIG. 8 ALTERNATE PIN CONFIGURATION FOR WF4M16W-XDTX5

**56 CSOP TOP VIEW**

CS1	1	56	NC
A11	2	55	RESET
A12	3	54	A10
A13	4	53	A9
A14	5	52	A8
NC	6	51	A0
CS2	7	50	A1
A20	8	49	A2
A19	9	48	A3
A18	10	47	A4
A17	11	46	A5
A16	12	45	A6
A15	13	44	GND
Vcc	14	43	A7
GND	15	42	Vcc
I/O6	16	41	I/O9
I/O14	17	40	I/O1
I/O7	18	39	I/O8
I/O15	19	38	I/O0
RY/BY	20	37	NC
OE	21	36	NC
WE	22	35	CS3
NC	23	34	CS4
I/O13	24	33	I/O2
I/O5	25	32	I/O10
I/O12	26	31	I/O3
I/O4	27	30	I/O11
Vcc	28	29	GND

**BLOCK DIAGRAM**



**NOTE:**

- RY/BY is an open drain output and should be pulled-up to Vcc with an external resistor.
- CS1 and CS3 control the same data bus. Reads cannot be done with CS1 and CS3 both active. CS2 and CS4 control the same data bus. Reads cannot be done with CS2 and CS4 both active.
- Address compatible with Intel 1M16 56 SSOP, with the addition of A20 at pin 8. Also refer to Note 2.

**PIN DESCRIPTION**

I/O0-15	Data Inputs/Outputs
A0-20	Address Inputs
WE	Write Enable
CS1-4	Chip Selects
OE	Output Enable
Vcc	Power Supply
GND	Ground
RY/BY	Ready/Busy
RESET	Reset



**ORDERING INFORMATION**

**W F 4M16 - XXX DT X 5 X**

**LEAD FINISH:**

Blank = Gold plated leads

A = Solder dip leads

**V<sub>PP</sub> PROGRAMMING VOLTAGE**

5 = 5 V

**DEVICE GRADE:**

M = Military, 883 Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

**PACKAGE TYPE:**

DT = 56 Lead Dual Cavity CSOP (Package 213)  
fits standard 56 SSOP footprint

**ACCESS TIME (ns)**

**ORGANIZATION, 2M x 16**

User configurable as 4 x 2M x 8

**Flash**

**WHITE ELECTRONIC DESIGNS CORP.**