



## 512Kx32 SRAM MULTI-CHIP PACKAGE

### FEATURES

- Access Times of 12, 15, 17, 20, ns
- Packaging
  - 16mm x 18mm, 143 PBGA
- Organized as 512Kx32, User Configurable as 1Mx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 5V Power Supply
- Low Power CMOS

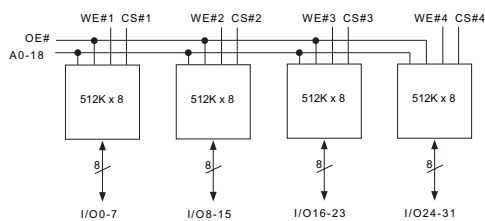
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### PIN CONFIGURATION FOR WEDPS512K32-XBX

TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12
<b>A</b>	-	A2	A1	A0	GND	GND	V <sub>CC</sub>	V <sub>CC</sub>	A18	A17	A16	GND
<b>B</b>	CS#2	A3	A4	D14	D15	NC	CS#4	D24	D25	OE#	A15	NC
<b>C</b>	D9	D8	NC	D12	D13	GND	V <sub>CC</sub>	D26	D27	WE#4	D31	D30
<b>D</b>	D10	D11	GND	GND	GND	GND	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	D28	D29
<b>E</b>	WE#2	GND	GND	GND	GND	GND	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	NC
<b>F</b>	GND	GND	GND	GND	GND	GND	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>
<b>G</b>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	GND	GND	GND	GND	GND	GND
<b>H</b>	CS#1	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	GND	GND	GND	GND	GND	NC
<b>J</b>	D1	D0	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	GND	GND	GND	GND	D23	D22
<b>K</b>	D2	D3	NC	D7	D5	V <sub>CC</sub>	GND	D17	D16	CS#3	D20	D21
<b>L</b>	WE#1	A6	A5	D6	D4	NC	WE#3	D19	D18	A14	A13	NC
<b>M</b>	GND	A7	A8	A9	V <sub>CC</sub>	V <sub>CC</sub>	GND	GND	A10	A11	A12	V <sub>CC</sub>

### BLOCK DIAGRAM



### PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
WE#1-4	Write Enables
CS#1-4	Chip Selects
OE#	Output Enable
V <sub>CC</sub>	Power Supply
GND	Ground
NC	Not Connected

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**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	V <sub>G</sub>	-0.5	V <sub>CC</sub> +0.5	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	7.0	V

**TRUTH TABLE**

CS	OE	WE	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.5	+0.8	V
Operating Temp (Mil)	T <sub>A</sub>	-55	+125	°C

**BGA THERMAL RESISTANCE**

Description	Symbol	Max	Unit	Notes
Junction to Ambient (No Airflow)	Theta JA	16.5	°C/W	1
Junction to Ball	Theta JB	11.3	°C/W	1
Junction to Case (Top)	Theta JC	9.8	°C/W	1

NOTE: Refer to Application Note "PBGA Thermal Resistance Correlation" at [www.whiteedc.com](http://www.whiteedc.com) in the application notes section for modeling conditions.

**CAPACITANCE**

(T<sub>A</sub> = +25°C)

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C <sub>OE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	30	pF
WE#1-4 capacitance	C <sub>WE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	10	pF
CS#1-4 capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	10	pF
Data I/O capacitance	C <sub>I/O</sub>	V <sub>IO</sub> = 0 V, f = 1.0 MHz	10	pF
Address input capacitance	C <sub>AD</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	30	pF

This parameter is guaranteed by design but not tested.

**DC CHARACTERISTICS**

(V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10	µA
Output Leakage Current	I <sub>LO</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10	µA
Operating Supply Current x 32 Mode	I <sub>CC</sub> x 32	CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		660	mA
Standby Current	I <sub>SB</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		80	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA	2.4		V

NOTE: DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V



**AC CHARACTERISTICS**

(V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	-12		-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle										
Read Cycle Time	t <sub>RC</sub>	12		15		17		20		ns
Address Access Time	t <sub>AA</sub>		12		15		17		20	ns
Output Hold from Address Change	t <sub>OH</sub>	0		0		0		0		ns
Chip Select Access Time	t <sub>ACS</sub>		12		15		17		20	ns
Output Enable to Output Valid	t <sub>OE</sub>		7		8		9		10	ns
Chip Select to Output in Low Z	t <sub>CLZ</sub> <sup>1</sup>	1		2		2		2		ns
Output Enable to Output in Low Z	t <sub>OLZ</sub> <sup>1</sup>	0		0		0		0		ns
Chip Disable to Output in High Z	t <sub>CHZ</sub> <sup>1</sup>		7		12		12		12	ns
Output Disable to Output in High Z	t <sub>OHZ</sub> <sup>1</sup>		7		12		12		12	ns

1. This parameter is guaranteed by design but not tested.

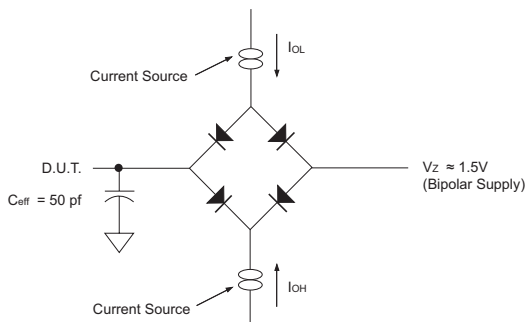
**AC CHARACTERISTICS**

(V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	-12		-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle										
Write Cycle Time	t <sub>WC</sub>	12		15		17		20		ns
Chip Select to End of Write	t <sub>CW</sub>	10		13		15		15		ns
Address Valid to End of Write	t <sub>AW</sub>	10		13		15		15		ns
Data Valid to End of Write	t <sub>DW</sub>	8		10		11		12		ns
Write Pulse Width	t <sub>WP</sub>	10		13		15		15		ns
Address Setup Time	t <sub>AS</sub>	0		2		2		2		ns
Address Hold Time	t <sub>AH</sub>	0		0		0		0		ns
Output Active from End of Write	t <sub>OW1</sub>	2		2		2		3		ns
Write Enable to Output in High Z	t <sub>WHZ1</sub>		7		8		9		11	ns
Data Hold Time	t <sub>DH</sub>	0		0		0		0		

1. This parameter is guaranteed by design but not tested.

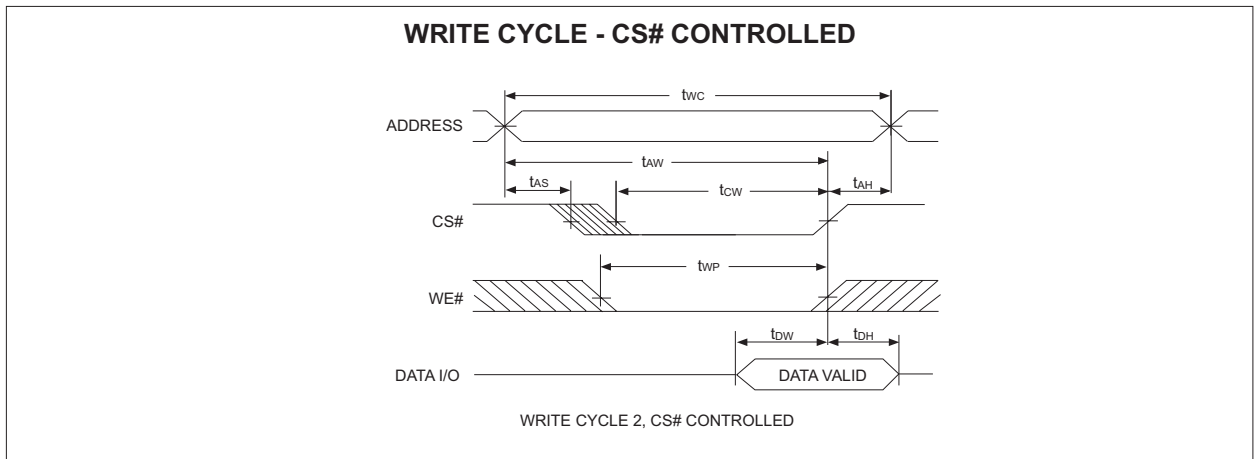
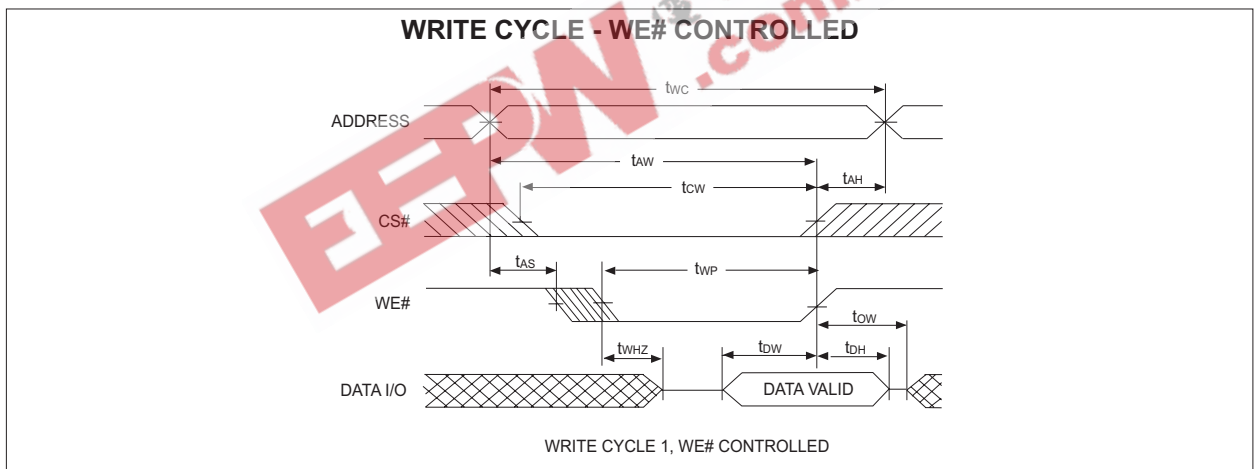
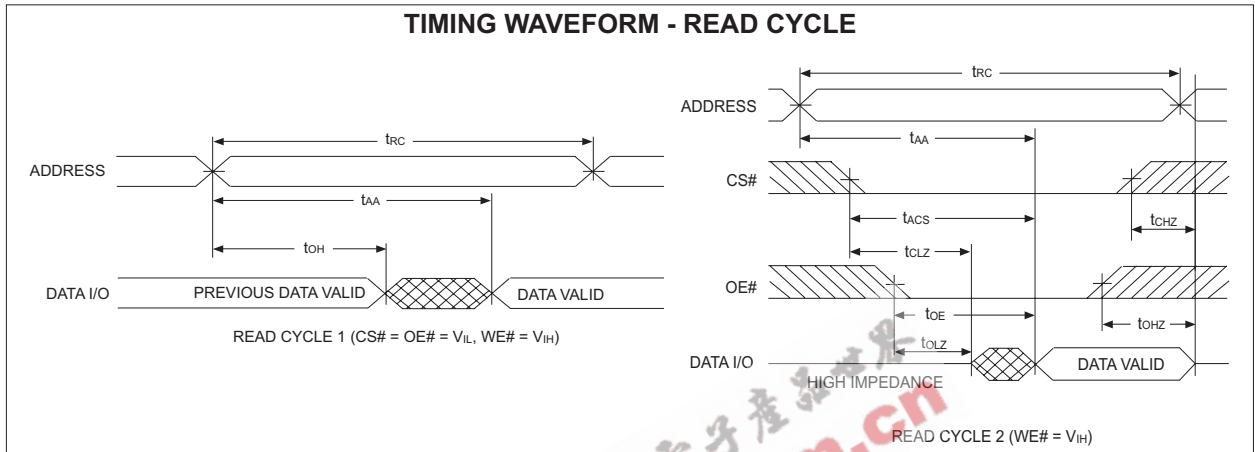
**AC TEST CIRCUIT**



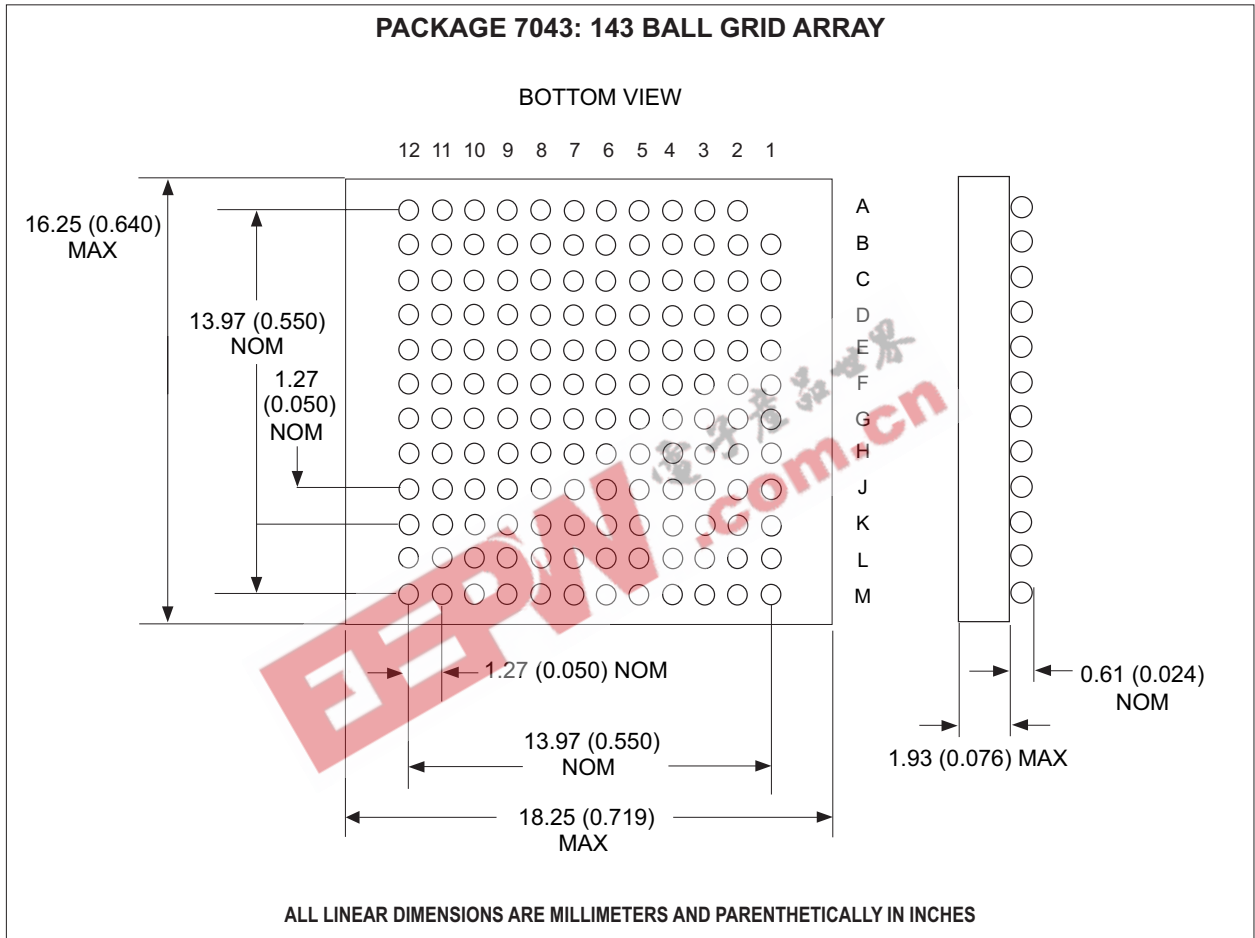
**AC TEST CONDITIONS**

Parameter	Typ	Unit
Input Pulse Levels	V <sub>IL</sub> = 0, V <sub>IH</sub> = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:  
 V<sub>Z</sub> is programmable from -2V to +7V.  
 I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.  
 Tester Impedance Z<sub>0</sub> = 75 Ω.  
 V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.  
 I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.  
 ATE tester includes jig capacitance.

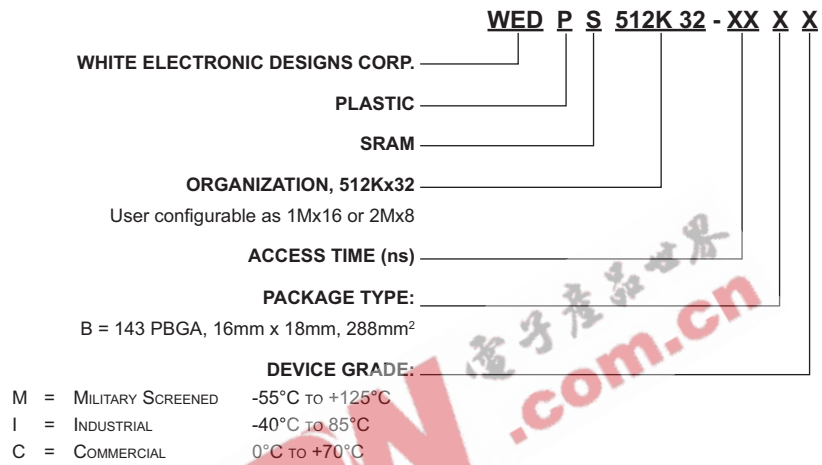


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**ORDERING INFORMATION**



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<b>Document Title</b>			
512K x 32 SRAM Multi-Chip Package			
<b>Revision History</b>			
<b>Rev #</b>	<b>History</b>	<b>ReleaseDate</b>	<b>Status</b>
Rev 0	Initial Release	March 2002	Advanced
Rev 1	Switch Rows and Columns header position (Pg. 1)	March 2002	Advanced
Rev 2	Switch Rows and Columns header position (Pg. 1)	May 2002	Advanced
Rev 3	Change mechanical outline to more accurate design (Pg. 1, 5)	May 2002	Advanced
Rev 4	Remove references to 25-55ns speed grades (Pg. 1, 2, 3)	August 2002	Advanced
Rev 5	Changes (Pg. 1, 2) 1.1 Add Thermal Resistance Table 1.2 Change product status to Final	January 2003	Final
Rev 6	Changes (Pg. 1, 5, 7) 1.1 Change package body height to 1.93mm Max 1.2 Add ball pitch (1.27mm) to package dimension	November 2003	Final