512Kx32 5V FLASH MODULE, SMD 5962-94612

FEATURES

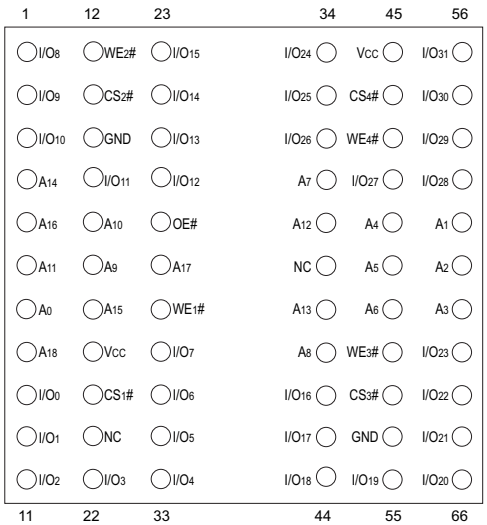
- Access Times of 60, 70, 90, 120, 150ns
- Packaging
  - 66 pin, PGA Type, 1.075" square, Hermetic Ceramic HIP (Package 400(1)).
  - 68 lead, 40mm, Low Capacitance Hermetic CQFP (Package 501)[1]
  - 68 lead, 40mm, Low Profile 3.5mm (0.140"), CQFP (Package 502)[1]
  - 68 lead, 22.4mm (0.880") Low Profile CQFP (G2U) 3.5mm (0.140") high, (Package 510)[1]
  - 68 lead, 22.4mm (0.880") CQFP (G2L) 5.08mm (0.200") high, Package (528)
- 1,000,000 Erase/Program Cycles Minimum
- Sector Architecture
  - 8 equal size sectors of 64KBytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 512Kx32
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Programming. 5V ± 10% Supply.
- Low Power CMOS, 6.5mA Standby
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Built-in Decoupling Caps for Low Noise Operation
- Page Program Operation and Internal Program Control Time
- Weight

  WF512K32 - XG2UX5 - 8 grams typical
  WF512K32N - XH1X5 - 13 grams typical
  WF512K32 - XG4TX5[1] - 20 grams typical
  WF512K32-XG2LX5 - 8 grams typical

* This product is subject to change without notice.
Note 1: Package Not Recommended for New Design
See Flash Programming Application Note 4M5 for algorithms.

FIGURE 1 – PIN CONFIGURATION FOR WF512K32N-XH1X5

Top View



Pin Description

I/O_{0-31}	Data Inputs/Outputs
A_{0-18}	Address Inputs
WE_{1-4}#	Write Enables
CS_{1-4}#	Chip Selects
OE#	Output Enable
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

Block Diagram

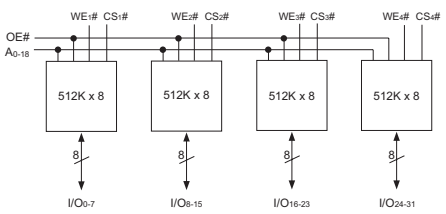
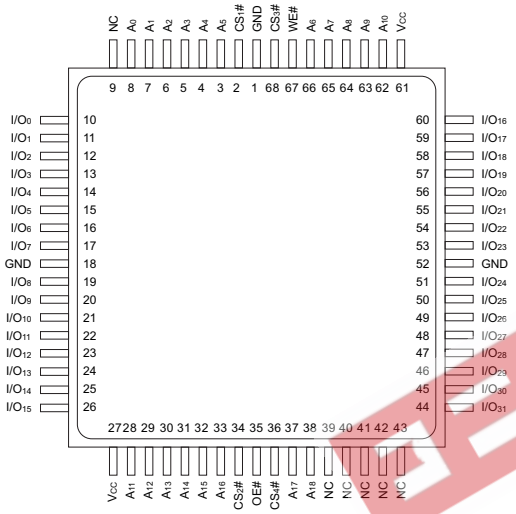


FIGURE 2 – PIN CONFIGURATION FOR WF512K32-XG4TX5[1]

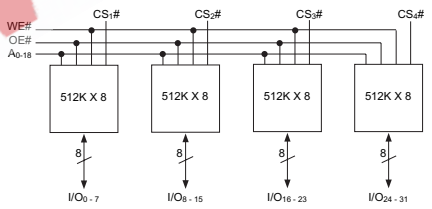
Top View



Pin Description

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
WE#	Write Enables
CS1-4#	Chip Selects
OE#	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

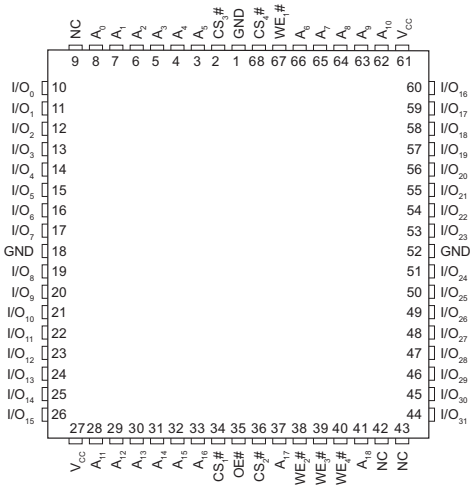
Block Diagram



Note 1: Package not recommended for new designs

FIGURE 3 – PIN CONFIGURATION FOR WF512K32-XG2UX5 AND WF512K32-XG2LX5

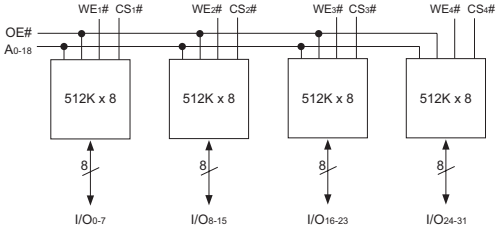
Top View



Pin Description

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
WE1-4#	Write Enables
CS1-4#	Chip Selects
OE#	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

Block Diagram



Absolute Maximum Ratings (1)

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage Range (V_{CC})	-2.0 to +7.0	V
Signal voltage range (any pin except A9) (2)	-2.0 to +7.0	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Data Retention (Mil Temp)	20 years	
Endurance - write/erase cycles (Mil Temp)	1,000,000 cycles min.	
A9 Voltage for sector protect (V_{ID}) (3)	-2.0 to +14.0	V

NOTES:
1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions,inputs may overshoot Vss to -2.0 V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is Vcc + 0.5V. During voltage transitions, outputs may overshoot to Vcc + 2.0 V for periods of up to 20ns.
3. Minimum DC input voltage on A9 pin is -0.5V. During voltage transitions, A9 may overshoot Vss to -2V for periods of up to 20ns. Maximum DC input voltage on A9 is +13.5V which may overshoot to 14.0 V for periods up to 20ns.

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C_{OE}	V_{IN} = 0V, f = 1.0 MHz	50	pF
WE_{1-4}# capacitance	C_{WE}	V_{IN} = 0V, f = 1.0 MHz		pF
HIP (PGA)			20	
CQFP G4T			50	
CQFP G2U/G2L			15	
CS_{1-4}# capacitance	C_{CS}	V_{IN} = 0V, f = 1.0 MHz	20	pF
Data# I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C
A_9 Voltage for Sector Protect	V_{ID}	11.5	12.5	V

DC CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LOx32}	CS# = V_{IH}, OE# = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
V_{CC} Active Current for Read (1)	I_{CC1}	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		190	mA
V_{CC} Active Current for Program or Erase (2)	I_{CC2}	CS# = V_{IH}, OE# = V_{IH}		240	mA
V_{CC} Standby Current	I_{CC4}	V_{CC} = 5.5, CS = V_{IH}, f = 5MHz		6.5	mA
V_{CC} Static Current	I_{CC3}	V_{CC} = 5.5, CS = V_{IH}		0.6	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA, V_{CC} = 4.5		0.45	V
Output High Voltage	V_{OH1}	I_{OH} = 2.5mA, V_{CC} = 4.5	0.85 x V_{CC}		V
Low V_{CC} Lock-Out Voltage	V_{LKO}		3.2	4.2	V

DC test conditions: VIL = 0.3V, VIH = VCC - 0.3V

NOTES:
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with OE at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.

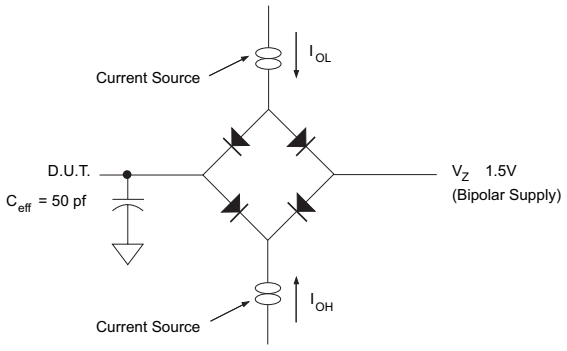
AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS,CS# CONTROLLED

V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-60 Min	-60 Max	-70 Min	-70 Max	-90 Min	-90 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
Write Cycle Time	t_{AVAV}	t_{WC}	60		70		90		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	40		45		45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	40		45		45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	40		45		45		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300		300		300	µs
Sector Erase Time (2)	t_{WHWH2}			15		15		15		15		15	sec
Read Recovery Time	t_{GHEL}		0		0		0		0		0		ns
Chip Programming Time				11		11		11		11		11	sec
Chip Erase Time (3)				64		64		64		64		64	sec

NOTES:
1. Typical value for t_{WHWH1} is 7µs.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 8sec.

FIGURE. 4 – AC TEST CIRCUIT



AC Test Conditions

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS,WE# CONTROLLED

V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-60 Min	-60 Max	-70 Min	-70 Max	-90 Min	-90 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
Write Cycle Time	t_{AVAV}	t_{WC}	60		70		90		120		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	40		45		45		50		50		ns
Address Setup Time	t_{AVWH}	t_{AS}	0		0		0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	40		45		45		50		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		0		0		ns
Address Hold Time	t_{WHAX}	t_{AH}	40		45		45		50		50		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300		300		300	µs
Sector Erase Time (2)	t_{WHWH2}			15		15		15		15		15	sec
Read Recovery Time before Write	t_{GHWL}		0		0		0		0		0		ns
VCC Set-up Time		t_{VCS}	50		50		50		50		50		µs
Chip Programming Time				11		11		11		11		11	sec
Output Enable Setup Time		t_{OES}	0		0		0		0		0		ns
Output Enable Hold Time (4)		t_{OEH}	10		10		10		10		10		ns
Chip Erase Time (3)				64		64		64		64		64	sec

NOTES:
1. Typical value for t_{WHWH1} is 7µs.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 8sec.
4. For Toggle and Data Polling.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS,WE# CONTROLLED

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-60 Min	-60 Max	-70 Min	-70 Max	-90 Min	-90 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
Read Cycle Time	t_{AVAV}	t_{RC}	60		70		90		120		150		ns
Address Access Time	t_{AVQV}	t_{ACC}		60		70		90		120		150	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		60		70		90		120		150	ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		30		35		35		50		55	ns
Chip Select to Output High Z (1)	t_{EHQZ}	t_{DF}		20		20		20		30		35	ns
Output Enable High to Output High Z (1)	t_{GHQZ}	t_{DF}		20		20		20		30		35	ns
Output Hold from Address, CS# or OE# Change, whichever is First	t_{AXQX}	t_{OH}	0		0		0		0		0		ns

1. Guaranteed by design, but not tested

FIGURE 5 – AC WAVEFORMS FOR READ OPERATIONS

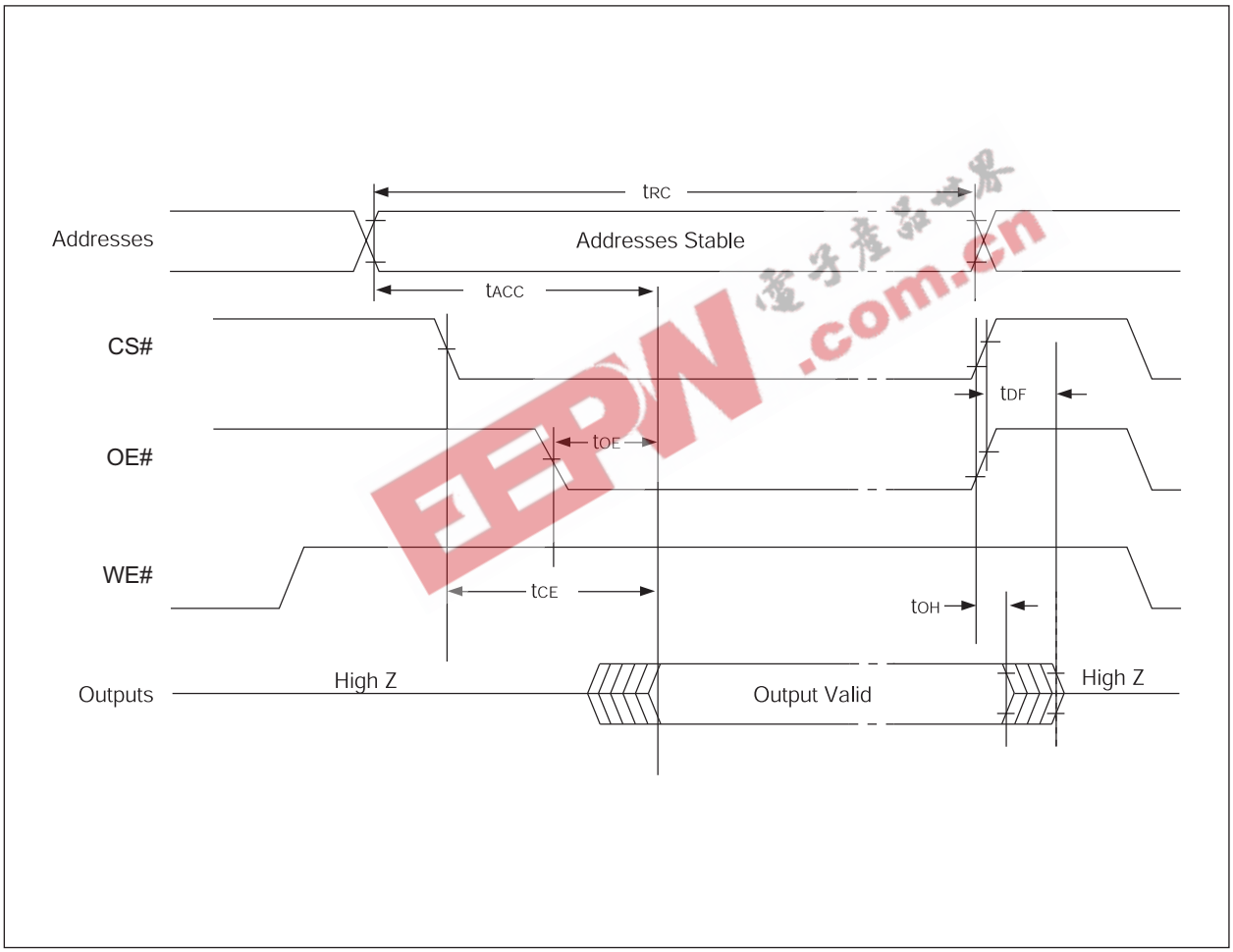
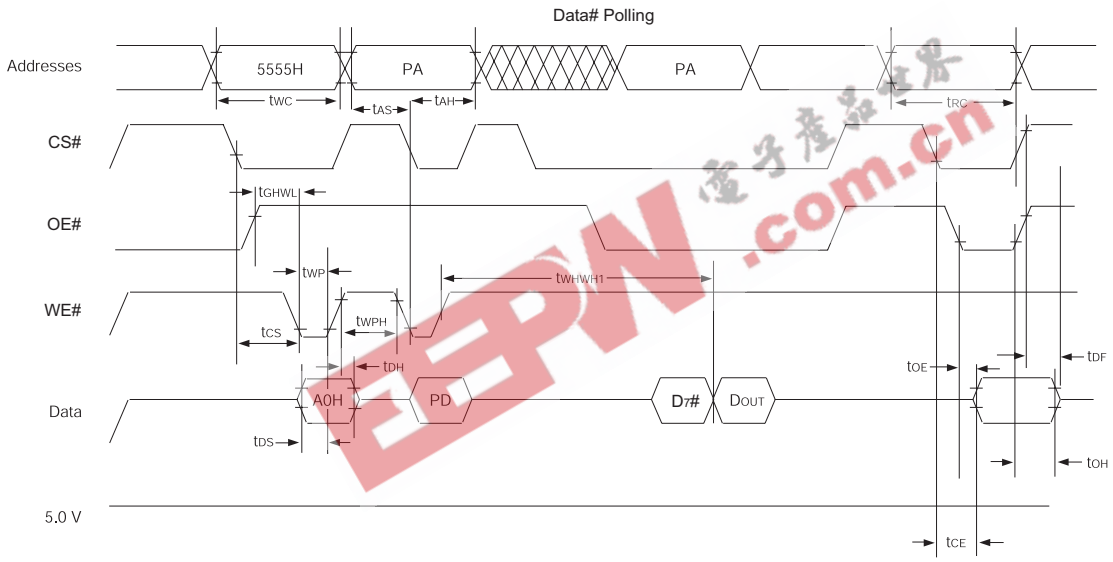
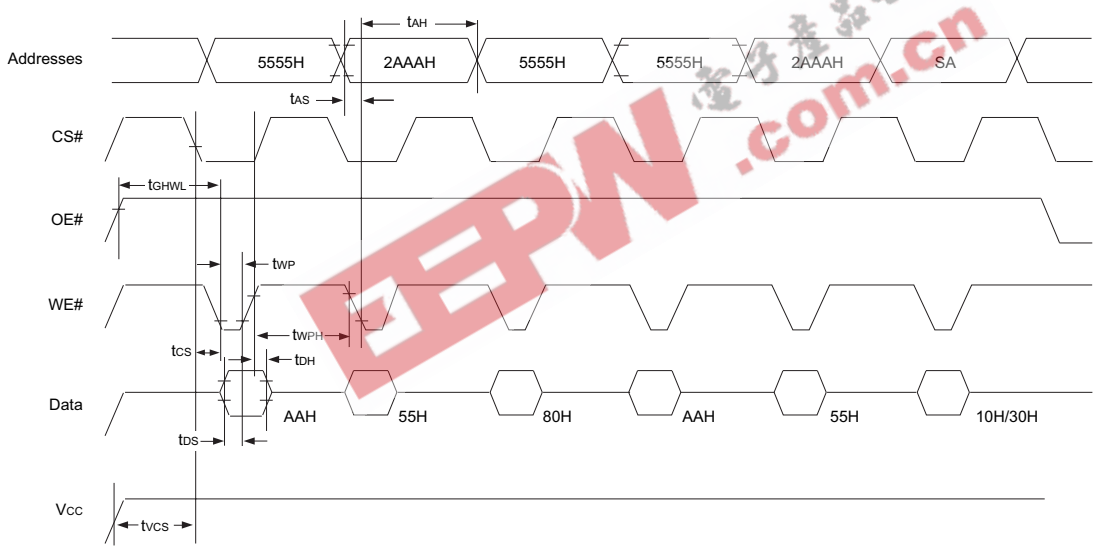


FIGURE 6 – WRITE/ERASE/PROGRAM OPERATION, WE# CONTROLLED



NOTES:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to the device (for each chip).
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

FIGURE 7 – AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



NOTE:
1. SA is the sector address for Sector Erase.

FIGURE 8 – AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS

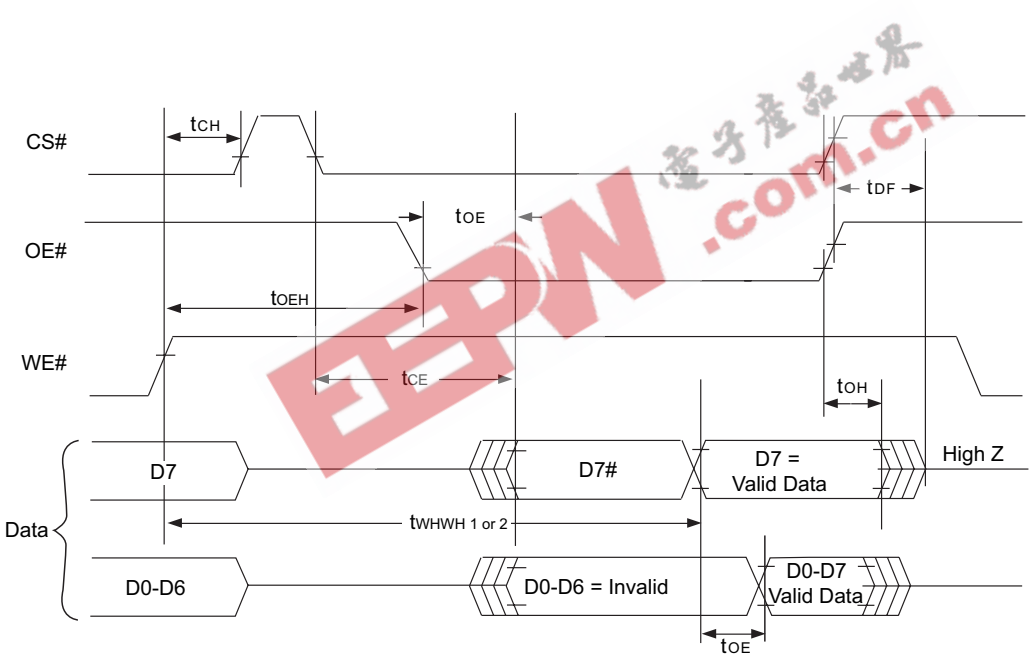
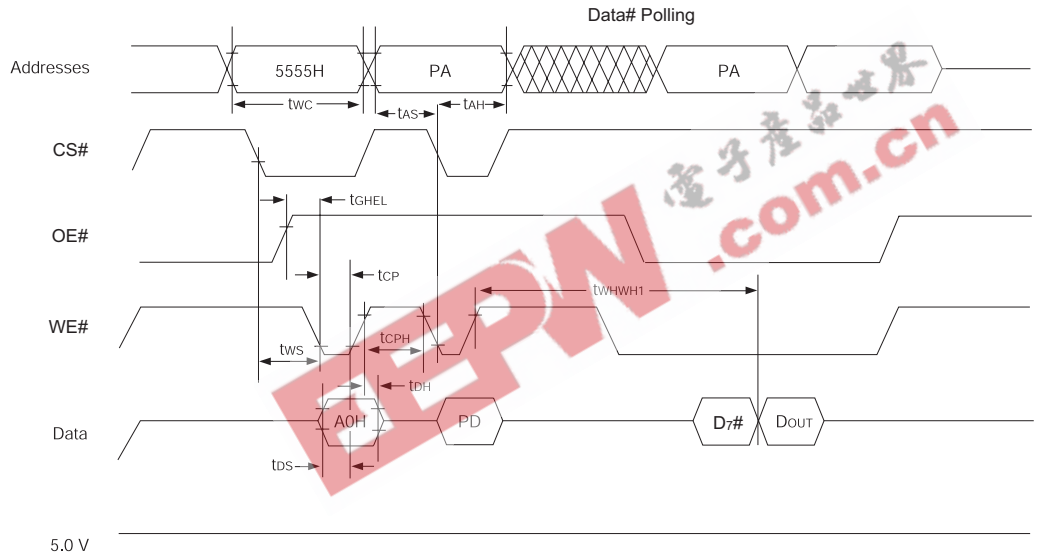
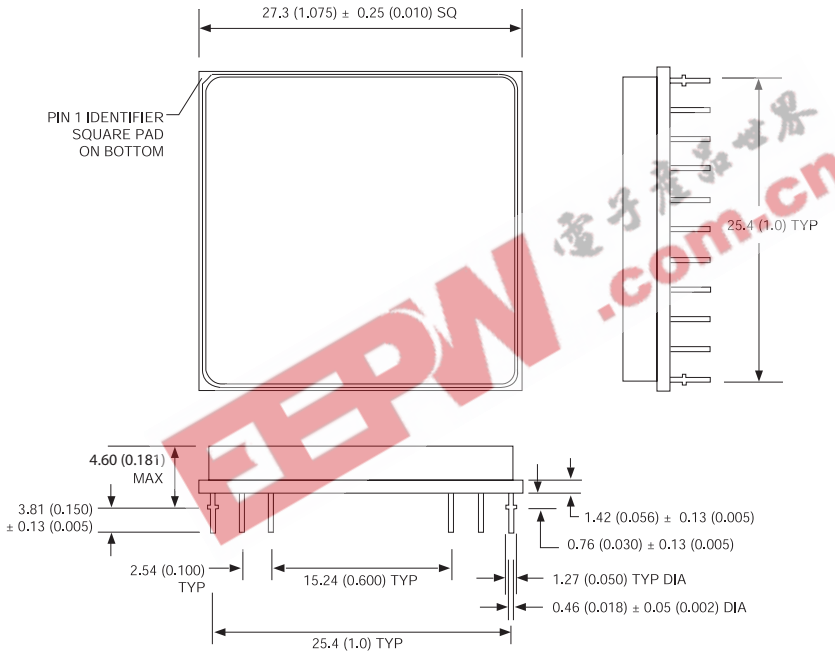


FIGURE 9 – ALTERNATE CS# CONTROLLED PROGRAMMING OPERATION TIMINGS



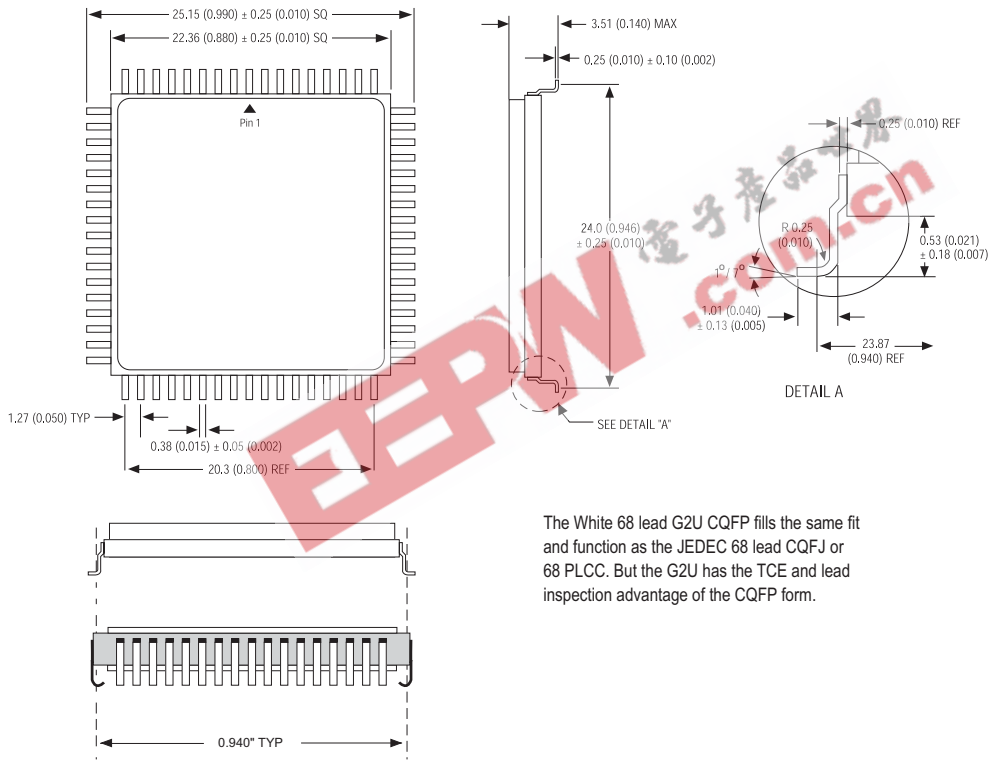
Notes:
1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to the device (for each chip).
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

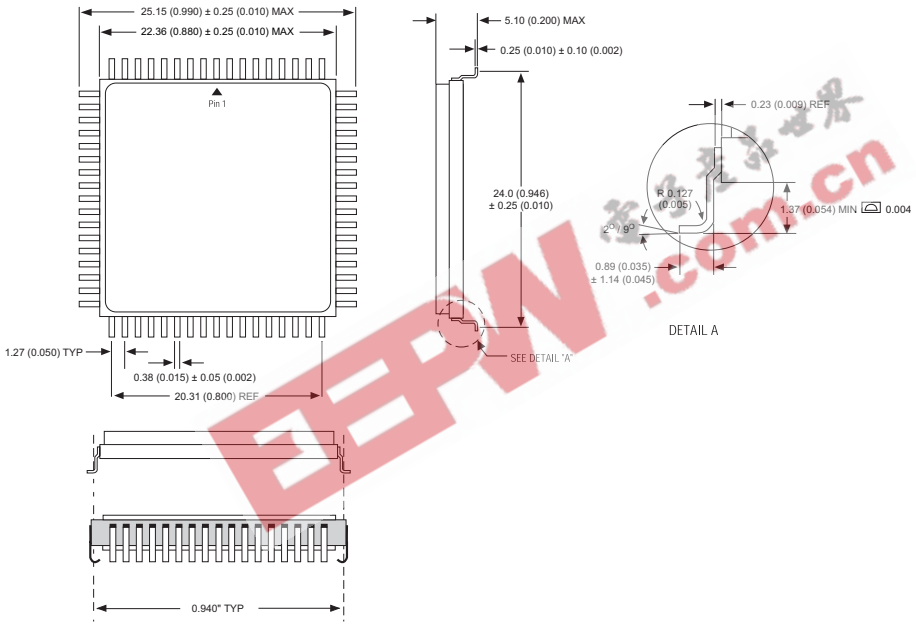
PACKAGE 510: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2U)



The White 68 lead G2U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2U has the TCE and lead inspection advantage of the CQFP form.

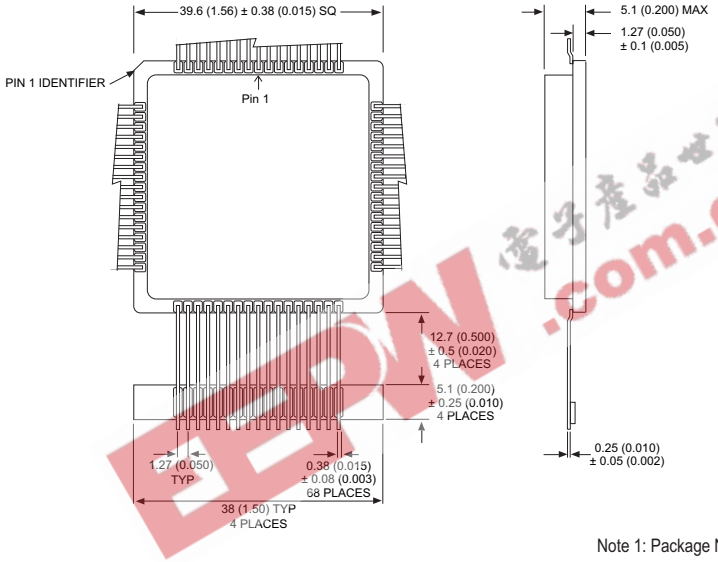
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 528: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2L)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)[1]



Note 1: Package Not Recommended for New Design

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W F 512K32 X - XXX X X 5 X

LEAD FINISH:
- Blank = Gold plated leads
- A = Solder dip leads

V_{PP} PROGRAMMING VOLTAGE
- 5 = 5 V

DEVICE GRADE:
- Q = MIL-STD-883 Compliant
- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE TYPE:
- H1 = 1.075" sq. Ceramic Hex In Line Package, HIP (Package 400*)
- G2U = 22.4mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 510)
- G2L = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 528)
- G4T[1] = 40mm Low Profile CQFP (Package 502)

ACCESS TIME (ns)

IMPROVEMENT MARK
- N = No Connect at pins 21 and 39 in HIP for Upgrade

ORGANIZATION, 512K x 32
- User configurable as 1M x 16 or 2M x 8

FLASH

WHITE ELECTRONIC DESIGNS CORP.

Note 1: Package Not Recommended for New Design

DEVICE TYPE	SPEED	PACKAGE	SMD NO.
512K x 32 Flash Module	150ns	66 pin HIP (H1) 1.075" sq.	5962-94612 01H4X
512K x 32 Flash Module	120ns	66 pin HIP (H1) 1.075" sq.	5962-94612 02H4X
512K x 32 Flash Module	90ns	66 pin HIP (H1) 1.075" sq.	5962-94612 03H4X
512K x 32 Flash Module	70ns	66 pin HIP (H1) 1.075" sq.	5962-94612 04H4X
512K x 32 Flash Module	150ns	68 lead CQFP Low Profile (G4T)[1]	5962-94612 01HTX[1]
512K x 32 Flash Module	120ns	68 lead CQFP Low Profile (G4T)[1]	5962-94612 02HTX[1]
512K x 32 Flash Module	90ns	68 lead CQFP Low Profile (G4T)[1]	5962-94612 03HTX[1]
512K x 32 Flash Module	70ns	68 lead CQFP Low Profile (G4T)[1]	5962-94612 04HTX[1]
512K x 32 Flash Module	150ns	68 lead CQFP/J (G2U)	5962-94612 01HZX
512K x 32 Flash Module	120ns	68 lead CQFP/J (G2U)	5962-94612 02HZX
512K x 32 Flash Module	90ns	68 lead CQFP/J (G2U)	5962-94612 03HZX
512K x 32 Flash Module	70ns	68 lead CQFP/J (G2U)	5962-94612 04HZX
512K x 32 Flash Module	150ns	68 lead CQFP (G2L)	5962-94612 01HAX
512K x 32 Flash Module	120ns	68 lead CQFP (G2L)	5962-94612 02HAX
512K x 32 Flash Module	90ns	68 lead CQFP (G2L)	5962-94612 03HAX
512K x 32 Flash Module	70ns	68 lead CQFP (G2L)	5962-94612 04HAX