



## 128Kx32 SSRAM/4Mx32 SDRAM

Advanced\*

### External Memory Solution for Texas Instruments TMS320C6000 DSP



#### FEATURES

- Clock speeds:
  - SSRAM: 200, 166, 150, and 133 MHz
  - SDRAMs: 125 and 100 MHz
- DSP Memory Solution
  - Texas Instruments TMS320C6201
  - Texas Instruments TMS320C6701
- Packaging:
  - 153 pin BGA, JEDEC MO-163
- 3.3V Operating supply voltage
- Direct control interface to both the SSRAM and SDRAM ports on the "C6x"
- Common address and databus
- 65% space savings vs. monolithic solution
- Reduced system inductance and capacitance

#### DESCRIPTION

The WED9LC6416VxxBC is a 3.3V, 128K x 32 Synchronous Pipeline SRAM and a 4Mx32 Synchronous DRAM array constructed with one 128K x 32 SBSRAM and two 4Mx16 SDRAM die mounted on a multilayer laminate substrate. The device is packaged in a 153 lead, 14mm by 22mm, BGA.

The WED9LC6416VxxBC provides a total memory solution for the Texas Instruments TMS320C6201 and the TMS320C6701 DSPs

The Synchronous Pipeline SRAM is available with clock speeds of 200, 166, 150, and 133 MHz, allowing the user to develop a fast external memory for the SSRAM interface port.

The SDRAM is available in clock speeds of 125 and 100 MHz, allowing the user to develop a fast external memory for the SDRAM interface port.

The WED9LC6416V is available in both commercial and industrial temperature ranges.

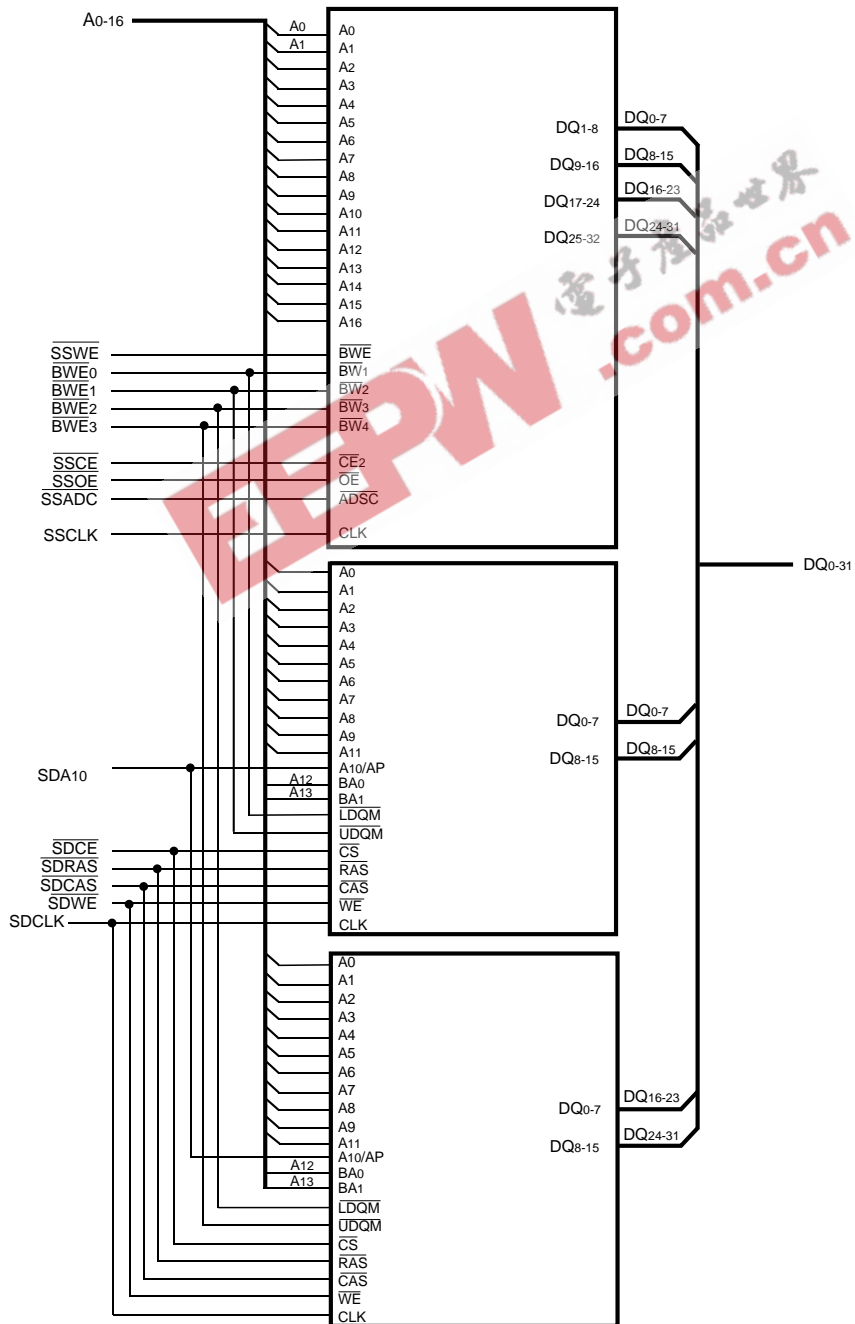
\* This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.

FIG. 1 PIN CONFIGURATION

TOP VIEW										PIN DESCRIPTION		
	1	2	3	4	5	6	7	8	9			
A	DQ19	DQ23	Vcc	Vss	Vss	Vss	Vcc	DQ24	DQ28	A	A0-16	Address Bus
B	DQ18	DQ22	Vcc	Vss	SDCE	Vss	Vcc	DQ25	DQ29	B	DQ0-31	Data Bus
C	Vcc0	Vcc0	Vcc	SDWE	SDA10	NC	Vcc	Vcc0	Vcc0	C	SSCLK	SSRAM Clock
D	DQ17	DQ21	Vcc	Vss	Vss	Vss	Vcc	DQ26	DQ30	D	SSADC	SSRAM Address Status Control
E	DQ16	DQ20	Vcc	Vss	SDCLK	Vss	Vcc	DQ27	DQ31	E	SSWE	SSRAM Write Enable
F	Vcc0	Vcc0	Vcc	Vss	Vss	Vss	Vcc	Vcc0	Vcc0	F	SSOE	SSRAM Output Enable
G	NC	NC	NC	SDRAS	SDCAS	Vss	A2	A4	A5	G	SDCLK	SDRAM Clock
H	NC	NC	A8	Vss	Vss	NC	A1	A3	A10	H	SDRAS	SDRAM Row Address Strobe
J	A6	A7	A9	Vss	Vss	NC	A0	A11	A12	J	SDCAS	SDRAM Column Address Strobe
K	NC / A17	NC / A18	NC / A19	Vss	Vss	NC	NC	A13	A14	K	SDWE	SDRAM Write Enable
L	NC	NC	NC	BWE2	BWE3	NC	NC	A15	A16	L	SDA10	SDRAM Address 10/auto precharge
M	Vcc0	Vcc0	Vcc	BWE0	BWE1	NC	Vcc	Vcc0	Vcc0	M	BWE0-3	SSRAM Byte Write Enables SDRAM SDQM 0 - 3
N	DQ12	DQ11	Vcc	Vss	Vss	Vss	Vcc	DQ4	DQ0	N	SSCE	Chip Enable SSRAM Device
P	DQ13	DQ10	Vcc	Vss	SSCLK	Vss	Vcc	DQ5	DQ1	P	SDCE	Chip Enable SDRAM Device
R	Vcc0	Vcc0	Vcc	Vss	Vss	Vss	Vcc	Vcc0	Vcc0	R	Vcc	Power Supply pins, 3.3V
T	DQ14	DQ9	Vcc	SSADC	SSWE	NC	Vcc	DQ6	DQ2	T	Vcc0	Data Bus Power Supply pins, 3.3V (2.5V future)
U	DQ15	DQ8	Vcc	SSOE	SSCE	NC	Vcc	DQ7	DQ3	U	Vss	Ground
	1	2	3	4	5	6	7	8	9		NC	No Connect



FIG. 2 BLOCK DIAGRAM





## OUTPUT FUNCTIONAL DESCRIPTIONS

Symbol	Type	Signal	Polarity	Function
SSCLK	Input	Pulse	Positive Edge	The system clock input. All of the SSRAM inputs are sampled on the rising edge of the clock.
$\overline{SSADS}$ $\overline{SSOE}$ $\overline{SSWE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{SSADS}$ , $\overline{SSOE}$ , and $\overline{SSWE}$ define the operation to be executed by the SSRAM.
$\overline{SSCE}$	Input	Pulse	Active Low	$\overline{SSCE}$ disable or enable SSRAM device operation.
SDCLK	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
SDCE	Input	Pulse	Active Low	SDCE disable or enable device operation by masking or enabling all inputs except SDCLK and BWE <sub>0-3</sub> .
$\overline{SDRAS}$ $\overline{SDCAS}$ $\overline{SDWE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{SDRAS}$ , $\overline{SDCAS}$ , and $\overline{SDWE}$ define the operation to be executed by the SDRAM.
A <sub>0-16</sub> , SDA <sub>10</sub>	Input	Level	—	Address bus for SSRAM and SDRAM. A <sub>0</sub> and A <sub>1</sub> are the burst address inputs for the SSRAM. During a Bank Active command cycle, A <sub>0-11</sub> , SDA <sub>10</sub> defines the row address (RA <sub>0-10</sub> ) when sampled at the rising clock edge. During a Read or Write command cycle, A <sub>0-7</sub> defines the column address (CA <sub>0-7</sub> ) when sampled at the rising clock edge. In addition to the row address, SDA <sub>10</sub> is used to invoke Autoprecharge operation at the end of the Burst Read or Write Cycle. If SDA <sub>10</sub> is high, autoprecharge is selected and A <sub>12</sub> and A <sub>13</sub> define the bank to be precharged. If SDA <sub>10</sub> is low, autoprecharge is disabled. During a Precharge command cycle, SDA <sub>10</sub> is used in conjunction with A <sub>12</sub> and A <sub>13</sub> to control which bank(s) to precharge. If SDA <sub>10</sub> is high, all banks will be precharged regardless of the state of A <sub>12</sub> and A <sub>13</sub> . If SDA <sub>10</sub> is low, then A <sub>12</sub> and A <sub>13</sub> are used to define which bank to precharge.
DQ <sub>0-31</sub>	Input Output	Level	—	Data Input/Output are multiplexed on the same pins.
BWE <sub>0-3</sub>	Input	Pulse		BWE <sub>0-3</sub> perform the byte write enable function for the SSRAM and DQM function for the SDRAM. BWE <sub>0</sub> is associated with DQ <sub>0-7</sub> , BWE <sub>1</sub> with DQ <sub>8-15</sub> , BWE <sub>2</sub> with DQ <sub>16-23</sub> and BWE <sub>3</sub> with DQ <sub>24-31</sub> .
V <sub>cc</sub> , V <sub>ss</sub>	Supply			Power and ground for the input buffers and the core logic.
V <sub>cco</sub>	Supply			Data base power supply pins, 3.3V (2.5V future).

**ABSOLUTE MAXIMUM RATINGS**

Voltage on Vcc Relative to Vss	-0.5V to +4.6V
V <sub>IN</sub> (DOx)	-0.5V to V <sub>CC</sub> +0.5V
Storage Temperature (BGA)	-55°C to +125°C
Junction Temperature	+175°C
Short Circuit Output Current	100 mA

\*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(V<sub>CC</sub> = 3.3V -5% / +10% unless otherwise noted;

0°C ≤ T<sub>A</sub> ≤ 70°C, Commercial; -40°C ≤ T<sub>A</sub> ≤ 85°C, Industrial)

Parameter	Symbol	Min	Max	Units
Supply Voltage (1)	V <sub>CC</sub>	3.135	3.6	V
Input High Voltage (1,2)	V <sub>IH</sub>	2.0	V <sub>CC</sub> +0.3	V
Input Low Voltage (1,2)	V <sub>IL</sub>	-0.3	0.8	V
Input Leakage Current 0 ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	I <sub>LI</sub>	-10	10	μA
Output Leakage (Output Disabled) 0 ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	I <sub>LO</sub>	-10	10	μA
Output High (I <sub>OH</sub> = -4mA) (1)	V <sub>OH</sub>	2.4	—	V
Output Low (I <sub>OL</sub> = 8mA) (1)	V <sub>OL</sub>	—	0.4	V

**NOTES:**

- All voltages referenced to V<sub>SS</sub> (GND).
- Overshoot: V<sub>IH</sub> ≤ +6.0V for t ≤ t<sub>tc</sub>/2  
Undershoot: V<sub>IL</sub> ≥ -2.0V for t ≤ t<sub>tc</sub>/2

**DC ELECTRICAL CHARACTERISTICS**

(V<sub>CC</sub> = 3.3V -5% / +10% unless otherwise noted; 0°C ≤ T<sub>A</sub> ≤ 70°C, Commercial; -40°C ≤ T<sub>A</sub> ≤ 85°C, Industrial)

Description	Conditions	Symbol	Frequency	Typ	Max	Units
Power Supply Current: Operating (1,2,3)	SSRAM Active / DRAM Auto Refresh	I <sub>CC1</sub>	133MHz	400	550	mA
			150MHz	450	580	
			166MHz	500	625	
			200MHz	550	700	
Power Supply Current Operating (1,2,3)	SSRAM Active / DRAM Idle	I <sub>CC2</sub>	133MHz	300	450	mA
			150MHz	350	480	
			166MHz	400	525	
			200MHz	450	585	
Power Supply Current Operating (1,2,3)	SDRAM Active / SSRAM Idle	I <sub>CC3</sub>	83MHz	220	240	mA
			100MHz	235	250	
			125MHz	255	280	
CMOS Standby	SSCE and SDCE ≤ V <sub>CC</sub> -0.2V, All other inputs at V <sub>SS</sub> +0.2 ≤ V <sub>IN</sub> or V <sub>IN</sub> ≤ V <sub>CC</sub> -0.2V, Clk frequency = 0	I <sub>SB1</sub>		20.0	40.0	mA
TTL Standby	SSCE and SDCE ≤ V <sub>IH</sub> min All other inputs at V <sub>IL</sub> max ≤ V <sub>IN</sub> or V <sub>IN</sub> ≤ V <sub>CC</sub> -0.2V, Clk frequency = 0	I <sub>SB2</sub>		30.0	55.0	mA
Auto Refresh		I <sub>CC5</sub>		190	250	mA

**NOTES:**

- I<sub>CC</sub> (operating) is specified with no output current. I<sub>CC</sub> (operating) increases with faster cycle times and greater output loading.
- "Device idle" means device is deselected (CE ≥ V<sub>IH</sub>) Clock is running at max frequency and Addresses are switching each cycle.
- Typical values are measured at 3.3V, 25°C. I<sub>CC</sub> (operating) is specified at specified frequency.

**BGA CAPACITANCE**

Description	Conditions	Symbol	Typ	Max	Units
Address Input Capacitance (1)	T <sub>A</sub> = 25°C; f = 1MHz	C <sub>I</sub>	5	8	pF
Input/Output Capacitance (DO) (1)	T <sub>A</sub> = 25°C; f = 1MHz	C <sub>O</sub>	8	10	pF
Control Input Capacitance (1)	T <sub>A</sub> = 25°C; f = 1MHz	C <sub>A</sub>	5	8	pF
Clock Input Capacitance (1)	T <sub>A</sub> = 25°C; f = 1MHz	C <sub>CK</sub>	4	6	pF

**NOTE:**

- This parameter is sampled.

**SSRAM AC CHARACTERISTICS**(V<sub>CC</sub> = 3.3V -5% / +10% unless otherwise noted: 0°C ≤ T<sub>A</sub> ≤ 70°C, Commercial; -40°C ≤ T<sub>A</sub> ≤ 85°C, Industrial)

Parameter	Symbol	200MHz		166MHz		150MHz		133MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock Cycle Time	t <sub>KHKH</sub>	5		6		7		8		ns
Clock HIGH Time	t <sub>KLKH</sub>	1.6		2.4		2.6		2.8		ns
Clock LOW Time	t <sub>KHKL</sub>	1.6		2.4		2.6		2.8		ns
Clock to output valid	t <sub>KHOV</sub>		2.5		3.5		3.8		4.0	ns
Clock to output invalid	t <sub>KHOX</sub>	1.5		1.5		1.5		1.5		ns
Clock to output on Low-Z	t <sub>KQLZ</sub>	0		0		0		0		ns
Clock to output in High-Z	t <sub>KOHZ</sub>	1.5	3	1.5	3.5	1.5	3.8	1.5	4.0	ns
Output Enable to output valid	t <sub>OELQV</sub>		2.5		3.5		3.8		4.0	ns
Output Enable to output in Low-Z	t <sub>OELZ</sub>	0		0		0		0		ns
Output Enable to output in High-Z	t <sub>OEHZ</sub>		3.0		3.5		3.5		3.8	ns
Address, Control, Data-in Setup Time to Clock	t <sub>s</sub>	1.5		1.5		1.5		1.5		ns
Address, Control, Data-in Hold Time to Clock	t <sub>h</sub>	0.5		0.5		0.5		0.5		ns



## SSRAM OPERATION TRUTH TABLE

Operation	Address Used	$\overline{SSCE}$	$\overline{SSADS}$	$\overline{SSWE}$	$\overline{SSOE}$	DQ
Deselected Cycle, Power Down	None	H	L	X	X	High-Z
WRITE Cycle, Begin Burst	External	L	L	L	X	D
READ Cycle, Begin Burst	External	L	L	H	L	Q
READ Cycle, Begin Burst	External	L	L	H	H	High-Z
READ Cycle, Suspend Burst	Current	X	H	H	L	Q
READ Cycle, Suspend Burst	Current	X	H	H	H	High-Z
READ Cycle, Suspend Burst	Current	H	H	H	L	Q
READ Cycle, Suspend Burst	Current	H	H	H	H	High-Z
WRITE Cycle, Suspend Burst	Current	X	H	L	X	D
WRITE Cycle, Suspend Burst	Current	H	H	L	X	D

## NOTE:

1. X means "don't care", H means logic HIGH. L means logic LOW.
2. All inputs except  $\overline{SSOE}$  must meet setup and hold times around the rising edge (LOW to HIGH) of  $\overline{SSCLK}$ .
3. Suspending burst generates wait cycle
4. For a write operation following a read operation,  $\overline{SSOE}$  must be HIGH before the input data required setup time plus High-Z time for  $\overline{SSOE}$  and staying HIGH through out the input data hold time.
5. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.

## SSRAM PARTIAL TRUTH TABLE

Function	$\overline{SSWE}$	$\overline{BWE0}$	$\overline{BWE1}$	$\overline{BWE2}$	$\overline{BWE3}$
READ	H	X	X	X	X
WRITE one Byte (DQ0-7)	L	L	H	H	H
WRITE all Bytes	L	L	L	L	L



FIG. 3 SSRAM READ TIMING

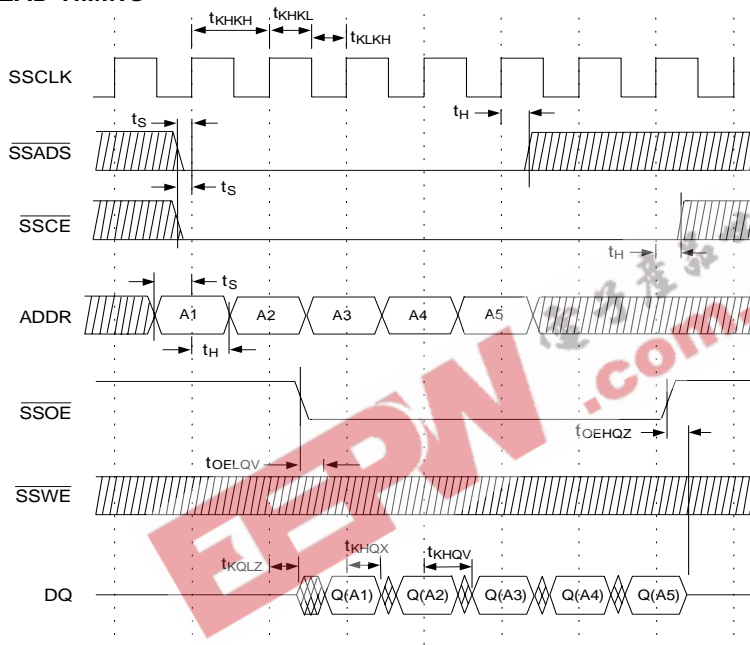
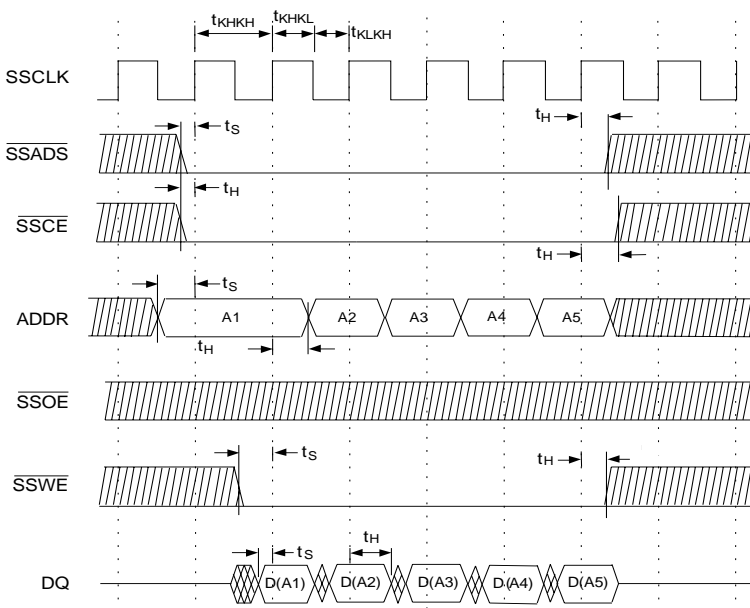


FIG. 4 SSRAM WRITE TIMING





## SDRAM AC CHARACTERISTICS

(V<sub>CC</sub> = 3.3V -5% / +10% unless otherwise noted; 0°C ≤ T<sub>A</sub> ≤ 70°C, Commercial; -40°C ≤ T<sub>A</sub> ≤ 85°C, Industrial)

Parameter	Symbol	125MHz		100MHz		83MHz		Units	
		Min	Max	Min	Max	Min	Max		
Clock Cycle Time (1)	CL = 3	tcc	8	1000	10	1000	12	1000	ns
	CL = 2	tcc	10	1000	12	1000	15	1000	
Clock to valid Output delay (1,2)		tsac		6		7		8	ns
Output Data Hold Time (2)		toH	3		3		3		ns
Clock HIGH Pulse Width (3)		tch	3		3		3		ns
Clock LOW Pulse Width (3)		tcl	3		3		3		ns
Input Setup Time (3)		tss	2		2		2		ns
Input Hold Time (3)		tsh	1		1		1		ns
CLK to Output Low-Z (2)		tslz	2		2		2		ns
CLK to Output High-Z		tshz		7		7		8	ns
Row Active to Row Active Delay (4)		trrd	20		20		24		ns
RAS\ to CAS\ Delay (4)		trcd	20		20		24		ns
Row Precharge Time (4)		trp	20		20		24		ns
Row Active Time (4)		trAs	50	10,000	50	10,000	60	10,000	ns
Row Cycle Time - Operation (4)		trc	70		80		90		ns
Row Cycle Time - Auto Refresh (4,8)		trfc	70		80		90		ns
Last Data in to New Column Address Delay (5)		tcDL	1		1		1		CLK
Last Data in to Row Precharge (5)		trDL	1		1		1		CLK
Last Data in to Burst Stop (5)		tbDL	1		1		1		CLK
Column Address to Column Address Delay (6)		tccD	1.5		1.5		1.5		CLK
Number of Valid Output Data (7)			2		2		2		ea
			1		2		1		

## NOTES:

- Parameters depend on programmed CAS latency.
- If clock rise time is longer than 1ns (tr<sub>rise</sub>/2 - 0.5)ns should be added to the parameter.
- Assumed input rise and fall time = 1ns. If tr<sub>rise</sub> or tr<sub>fall</sub> are longer than 1ns. [(tr<sub>rise</sub> = tr<sub>fall</sub>)/2] - 1ns should be added to the parameter.
- The minimum number of clock cycles required is determined by dividing the minimum time required by the clock cycle time and then rounding up to the next higher integer.
- Minimum delay is required to complete write.
- All devices allow every cycle column address changes.
- In case of row precharge interrupt, auto precharge and read burst stop.
- A new command may be given tr<sub>fc</sub> after self-refresh exit.





### CLOCK FREQUENCY AND LATENCY PARAMETERS - 125MHz SDRAM

(Unit = number of clock)

Frequency	CAS Latency	t <sub>RC</sub>	t <sub>RAS</sub>	t <sub>RP</sub>	t <sub>RRD</sub>	t <sub>RCD</sub>	t <sub>CCD</sub>	t <sub>CDL</sub>	t <sub>RDL</sub>
		70ns	50ns	20ns	20ns	20ns	10ns	10ns	10ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1

### CLOCK FREQUENCY AND LATENCY PARAMETERS - 100MHz SDRAM

(Unit = number of clock)

Frequency	CAS Latency	t <sub>RC</sub>	t <sub>RAS</sub>	t <sub>RP</sub>	t <sub>RRD</sub>	t <sub>RCD</sub>	t <sub>CCD</sub>	t <sub>CDL</sub>	t <sub>RDL</sub>
		70ns	50ns	20ns	20ns	20ns	10ns	10ns	10ns
100MHz (12.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	5	2	2	2	1	1	1

### REFRESH CYCLE PARAMETERS

Parameter	Symbol	-10		-12		Units
		Min	Max	Min	Max	
Refresh Period (1,2)	t <sub>REF</sub>	—	64	—	64	ms

#### NOTES:

- 4096 cycles
- Any time that the Refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to "wake-up" the device.

### SDRAM COMMAND TRUTH TABLE

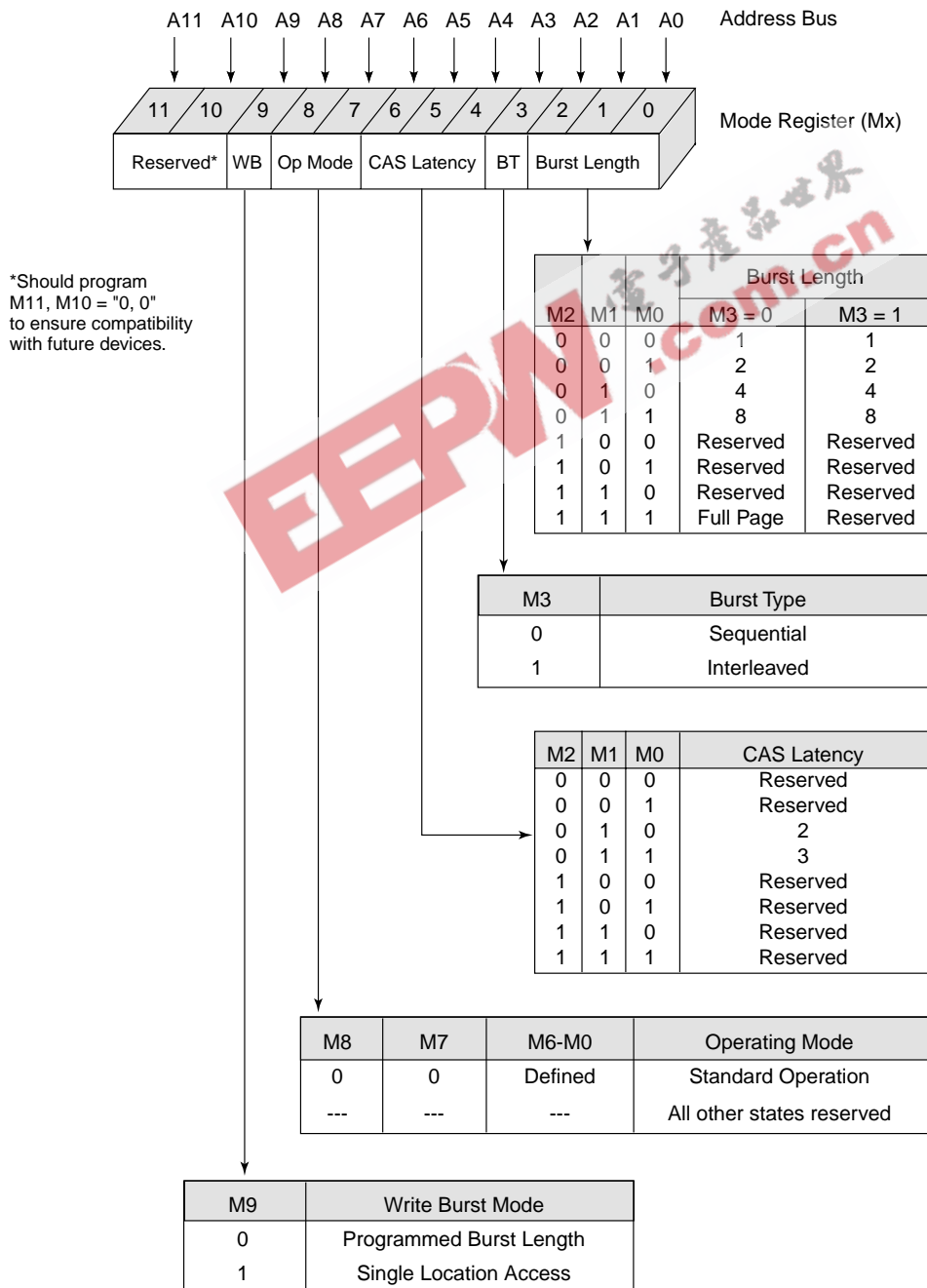
Function	SDCE	SDRAS	SDCAS	SDWE	BWE	A <sub>12</sub> , A <sub>13</sub>	SDA <sub>10</sub> A <sub>11-0</sub>	Notes	
Mode Register Set	L	L	L	L	X	OP CODE			
Auto Refresh (CBR)	L	L	L	H	X	X	X		
Precharge	Single Bank	L	L	H	L	X	BA	L	2
	Precharge all Banks	L	L	H	L	X	X	H	
Bank Activate	L	L	H	H	X	BA	Row Address	2	
Write	L	H	L	L	X	BA	L	2	
Write with Auto Precharge	L	H	L	L	X	BA	H	2	
Read	L	H	L	L	X	BA	L	2	
Read with Auto Precharge	L	H	L	H	X	BA	H	2	
Burst Termination	L	H	H	L	X	X	X	3	
No Operation	L	H	H	H	X	X	X		
Device Deselect	H	X	X	X	X	X	X		
Data Write/Output Disable	X	X	X	X	L	X	X	4	
Data Mask/Output Disable	X	X	X	X	H	X	X	4	

#### NOTES:

- All of the SDRAM operations are defined by states of SDCE\, SDWE\, SDRAS\, SDCAS\, and BWE<sub>0-3</sub> at the positive rising edge of the clock.
- Bank Select (BA), if A<sub>12</sub> (BA<sub>0</sub>) and A<sub>13</sub> (BA<sub>1</sub>) select between different banks.
- During a Burst Write cycle there is a zero clock delay, for a Burst Read cycle the delay is equal to the CAS latency.
- The BWE has two functions for the data DQ Read and Write operations. During a Read cycle, when BWE goes high at a clock timing the data outputs are disabled and become high impedance after a two clock delay. BWE also provides a data mask function for Write cycles. When it activates, the Write operation at the clock is prohibited (zero clock latency).



MODE REGISTER SET TABLE





SDRAM CURRENT STATE TRUTH TABLE

Current State	Command						Description	Action	Notes
	$\overline{\text{SDCE}}$	$\overline{\text{SDRAS}}$	$\overline{\text{SDCAS}}$	$\overline{\text{SDWE}}$	A <sub>12</sub> & A <sub>13</sub> (BA)	A <sub>11</sub> -A <sub>0</sub>			
Idle	L	L	L	L	OP Code		Mode Register Set	Set the Mode Register	1
	L	L	L	H	X	X	Auto or Self Refresh	Start Auto	1
	L	L	H	L	X	X	Precharge	No Operation	
	L	L	H	H	BA	Row Address	Bank Activate	Activate the specified bank and row	
	L	H	L	L	BA	Column	Write w/o Precharge	ILLEGAL	2
	L	H	L	H	BA	Column	Read w/o Precharge	ILLEGAL	1
	L	H	H	L	X	X	Burst Termination	No Operation	1
	L	H	H	H	X	X	No Operation	No Operation	
Row Active	H	X	X	X	X	X	Device Deselect	No Operation	
	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Precharge	3
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	1
	L	H	L	L	BA	Column	Write	Start Write; Determine if Auto Precharge	4,5
	L	H	L	H	BA	Column	Read	Start Read; Determine if Auto Precharge	4,5
	L	H	H	L	X	X	Burst Termination	No Operation	
Read	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation	
	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Terminate Burst; Start the Precharge	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	L	H	L	L	BA	Column	Write	Terminate Burst; Start the Write cycle	5,6
	L	H	L	H	BA	Column	Read	Terminate Burst; Start a new Read cycle	5,6
Write	L	H	H	L	X	X	Burst Termination	Terminate the Burst	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Terminate Burst; Start the Precharge	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	L	H	L	L	BA	Column	Write	Terminate Burst; Start a new Write cycle	5,6
Read with Auto Precharge	L	H	L	H	BA	Column	Read	Terminate Burst; Start the Read cycle	5,6
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	2
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2



SDRAM CURRENT STATE TRUTH TABLE (cont.)

Current State	Command						Description	Action	Notes
	$\overline{\text{SDCE}}$	$\overline{\text{SDRAS}}$	$\overline{\text{SDCAS}}$	$\overline{\text{SDWE}}$	A <sub>12</sub> & A <sub>13</sub> (BA)	A <sub>11</sub> -A <sub>0</sub>			
Write with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	2
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	Continue the Burst	
Precharging	H	X	X	X	X	X	Device Deselect	Continue the Burst	
	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	No Operation; Bank(s) idle after tRP	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	L	H	L	L	BA	Column	Write w/o Precharge	ILLEGAL	2
	L	H	L	H	BA	Column	Read w/o Precharge	ILLEGAL	20
	L	H	H	L	X	X	Burst Termination	No Operation; Bank(s) idle after tRP	
Row Activating	L	H	H	H	X	X	No Operation	No Operation; Bank(s) idle after tRP	
	H	X	X	X	X	X	Device Deselect	No Operation; Bank(s) idle after tRP	
	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	2
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	L	H	L	L	BA	Column	Write	ILLEGAL	2
	L	H	L	H	BA	Column	Read	ILLEGAL	2
Write Recovering	L	H	H	L	X	X	Burst Termination	No Operation; Row active after tRCD	
	L	H	H	H	X	X	No Operation	No Operation; Row active after tRCD	
	H	X	X	X	X	X	Device Deselect	No Operation; Row active after tRCD	
	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	2
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	L	H	L	L	BA	Column	Write	Start Write; Determine if Auto Precharge	6
Write Recovering with Auto Precharge	L	H	L	H	BA	Column	Read	Start Read; Determine if Auto Precharge	6
	L	H	H	L	X	X	Burst Termination	No Operation; Row active after tDPL	
	L	H	H	H	X	X	No Operation	No Operation; Row active after tDPL	
	H	X	X	X	X	X	Device Deselect	No Operation; Row active after tDPL	
	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	2
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
Write Recovering with Auto Precharge	L	H	L	L	BA	Column	Write	ILLEGAL	2,6
	L	H	L	H	BA	Column	Read	ILLEGAL	2,6
	L	H	H	L	X	X	Burst Termination	No Operation; Precharge after tDPL	
	L	H	H	H	X	X	No Operation	No Operation; Precharge after tDPL	
	H	X	X	X	X	X	Device Deselect	No Operation; Precharge after tDPL	



SDRAM CURRENT STATE TRUTH TABLE (cont.)

Current State	Command						Description	Action	Notes
	$\overline{\text{SDCE}}$	$\overline{\text{SDRAS}}$	$\overline{\text{SDCAS}}$	$\overline{\text{SDWE}}$	A <sub>12</sub> & A <sub>13</sub> (BA)	A <sub>11</sub> -A <sub>0</sub>			
Refreshing	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	No Operation; Idle after t <sub>rc</sub>	
	L	H	H	H	X	X	No Operation	No Operation; Idle after t <sub>rc</sub>	
Mode Register Accessing	H	X	X	X	X	X	Device Deselect	No Operation; Idle after t <sub>rc</sub>	
	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	No Operation; Idle after two clock cycles	
	H	X	X	X	X	X	Device Deselect	No Operation; Idle after two clock cycles	

**NOTES:**

- Both Banks must be idle otherwise it is an illegal action.
- The Current State refers only refers to one of the banks, if BA selects this bank then the action is illegal. If BA selects the bank not being referenced by the Current State then the action may be legal depending on the state of that bank.
- The minimum and maximum Active time (t<sub>ras</sub>) must be satisfied.
- The  $\overline{\text{RAS}}$  to  $\overline{\text{CAS}}$  Delay (t<sub>rcd</sub>) must occur before the command is given.
- Address SDA<sub>10</sub> is used to determine if the Auto Precharge function is activated.
- The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.

The command is illegal if the minimum bank to bank delay time (t<sub>rrd</sub>) is not satisfied.



**FIG. 5 SDRAM SINGLE BIT READ-WRITE-READ CYCLE (SAME PAGE) @ CAS LATENCY = 3, BURST LENGTH = 1**

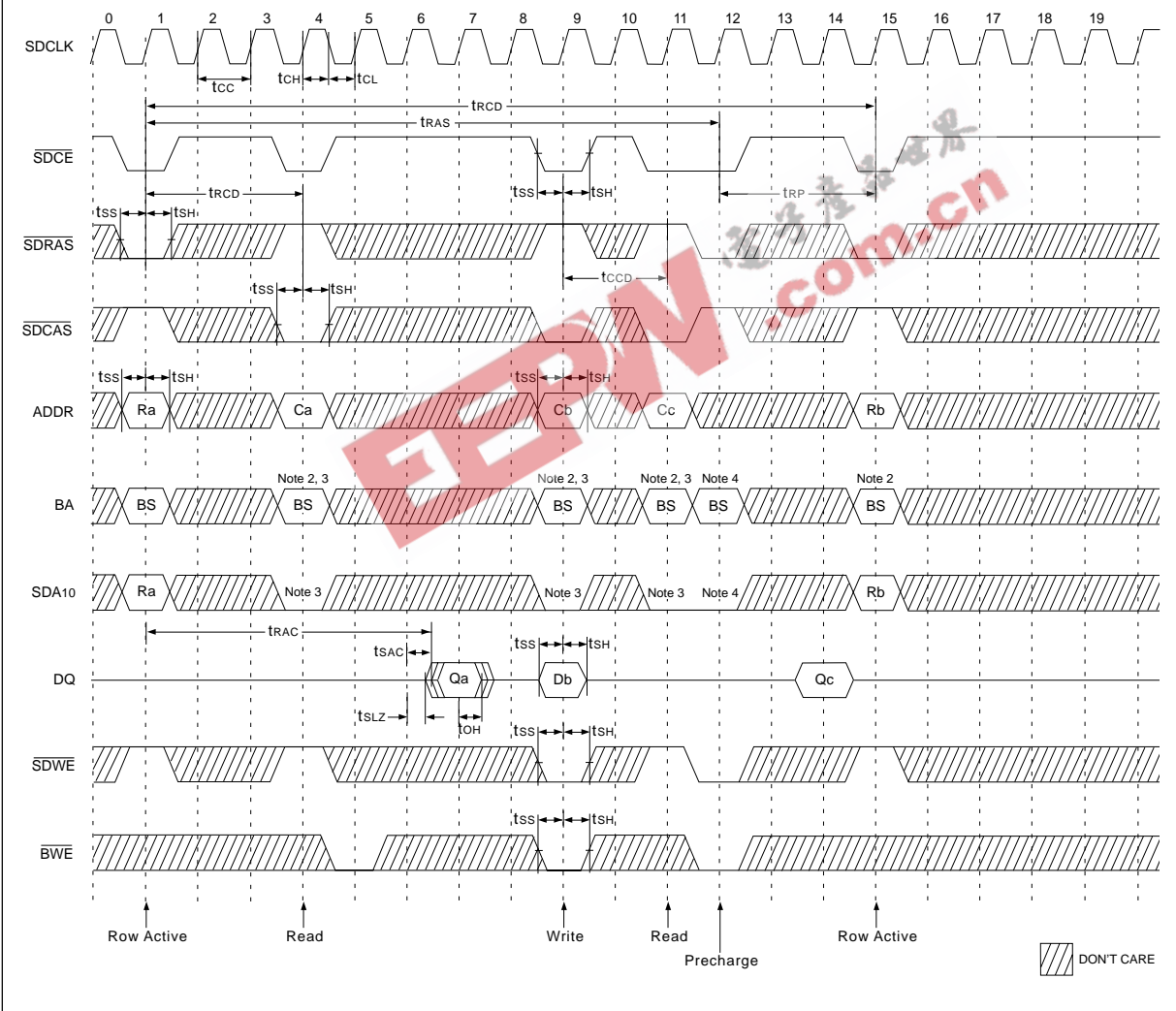




FIG. 6 SDRAM POWER UP SEQUENCE

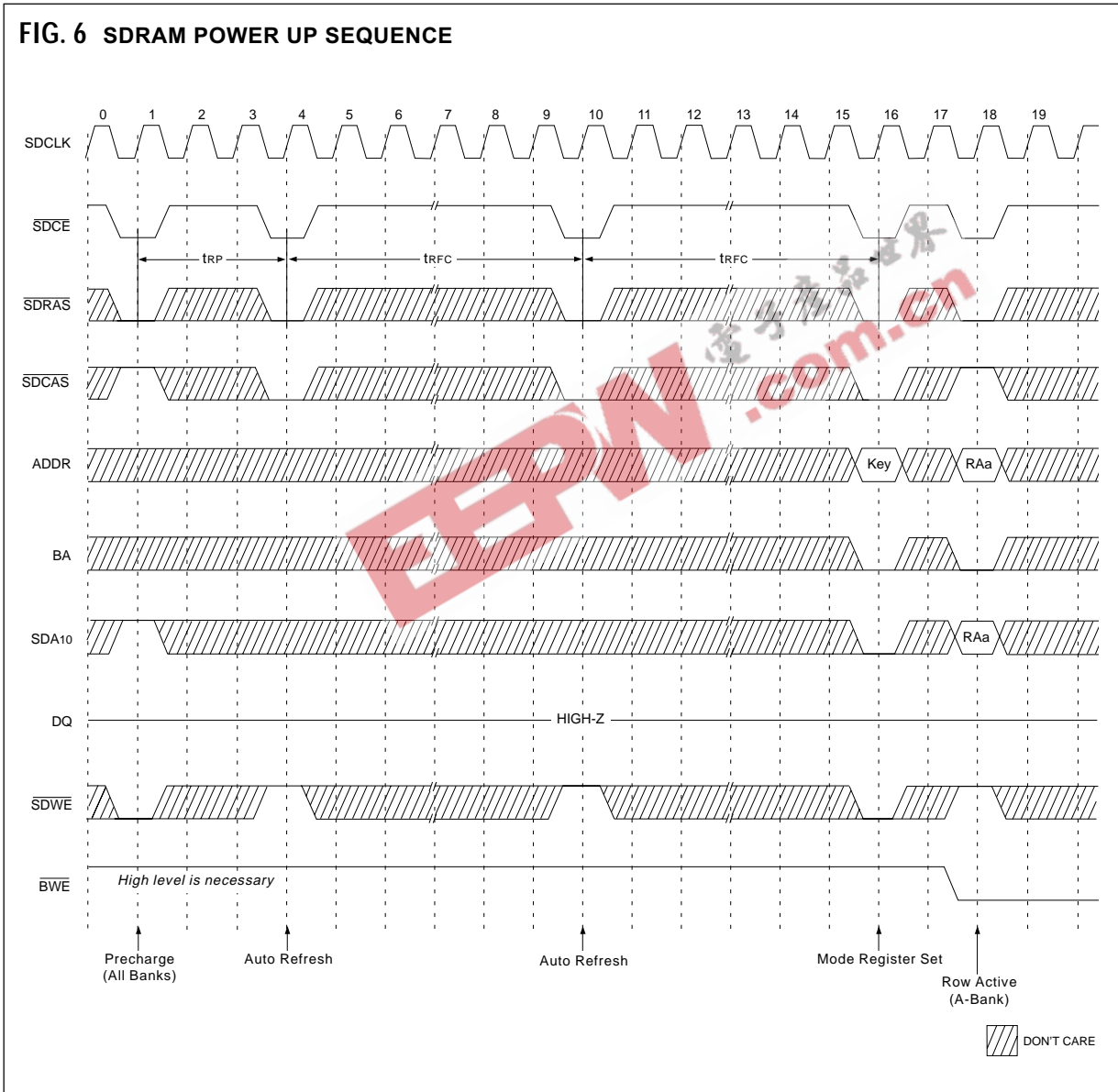
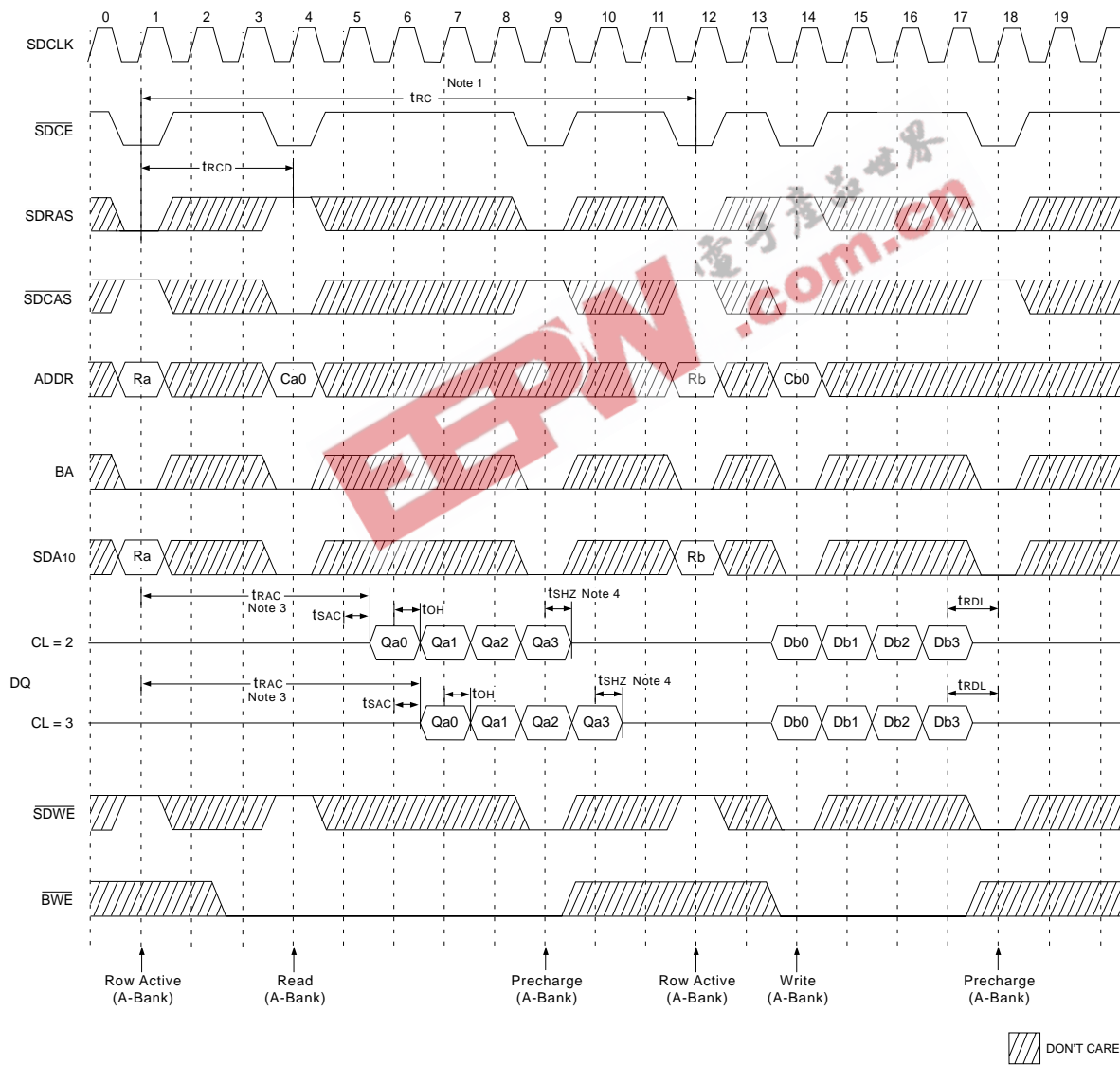




FIG. 7 SDRAM READ & WRITE CYCLE AT SAME BANK @ BURST LENGTH = 4



NOTES:

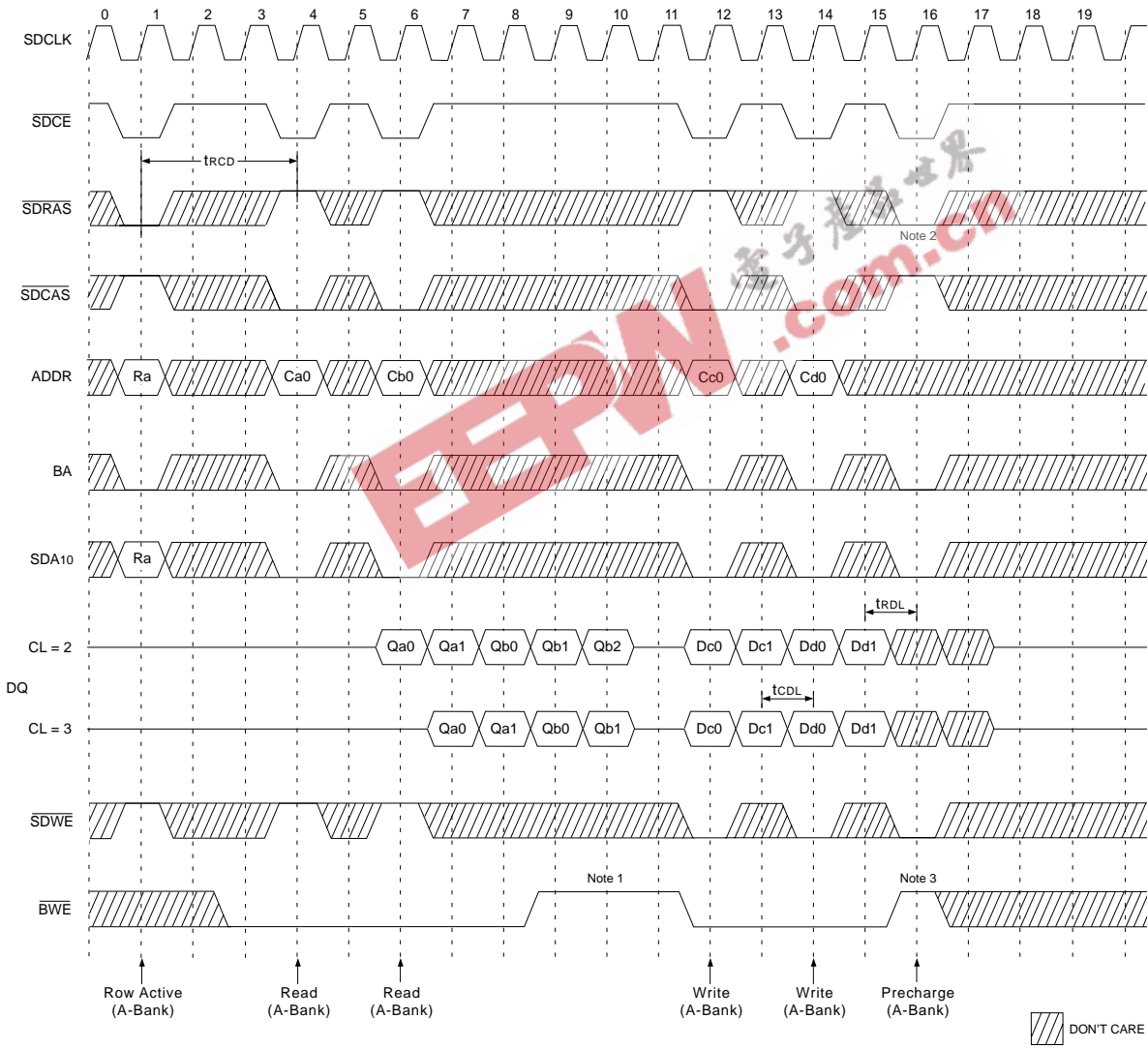
1. Minimum row cycle times are required to complete internal DRAM operation.
2. Row precharge can interrupt burst on any cycle. (CAS Latency - 1) number of valid output data is available after Row precharge. Last valid output will be Hi-Z ( $t_{SHZ}$ ) after the clock.
3. Access time from Row active command.  $t_{trc} * (t_{trCD} + \text{CAS Latency} - 1) + t_{tsAC}$ .
4. Output will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)

DONT CARE





FIG. 8 SDRAM PAGE READ & WRITE CYCLE AT SAME BANK @ BURST LENGTH = 4

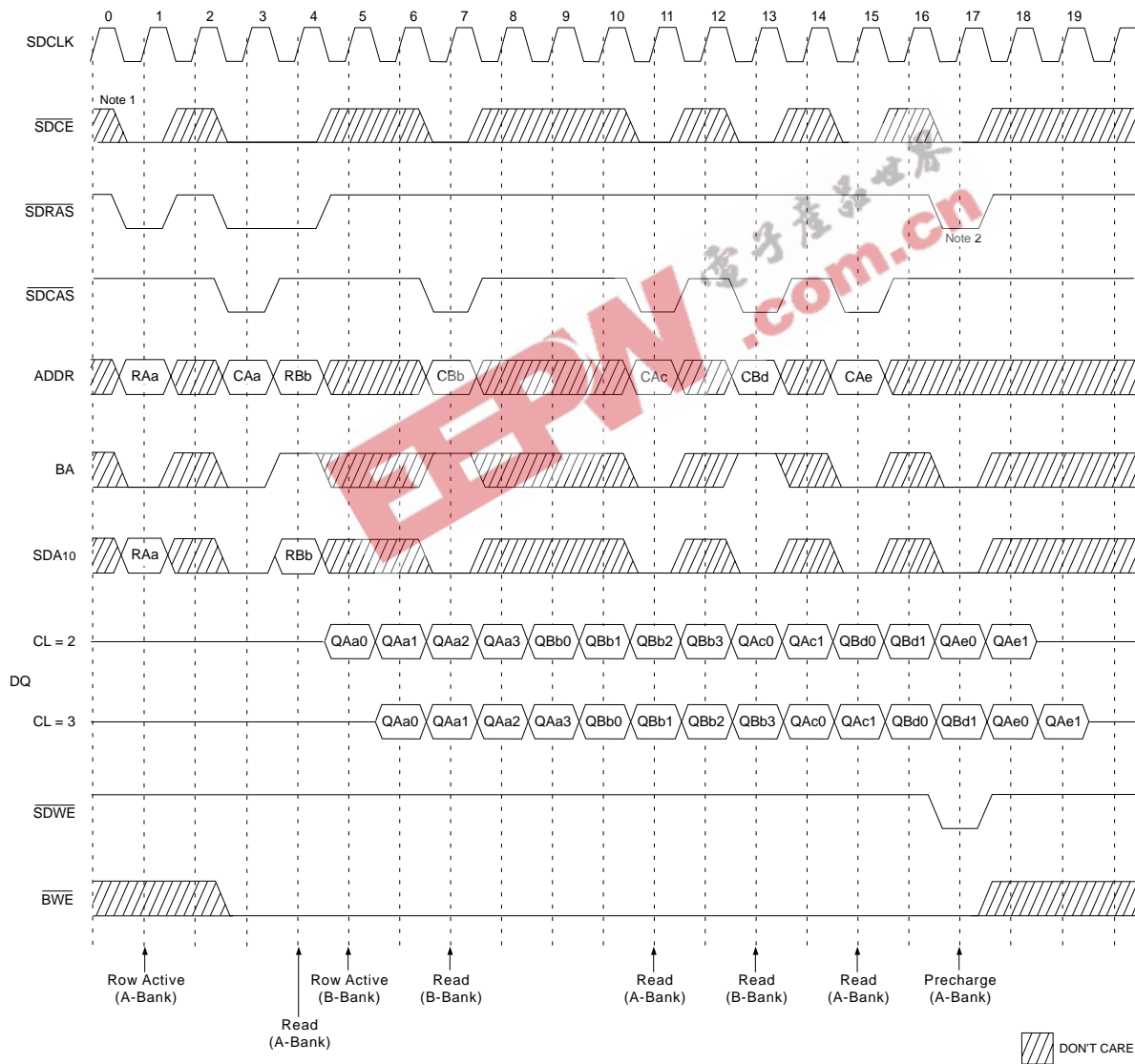


NOTES:

1. To write data before burst read ends,  $\overline{BWE}$  should be asserted three cycle prior to write command to avoid bus contention.
2. Row precharge will interrupt writing. Last data input,  $t_{rdL}$  before Row precharge will be written.
3.  $\overline{BWE}$  should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.



FIG. 9 SDRAM PAGE READ CYCLE AT DIFFERENT BANK @ BURST LENGTH = 4

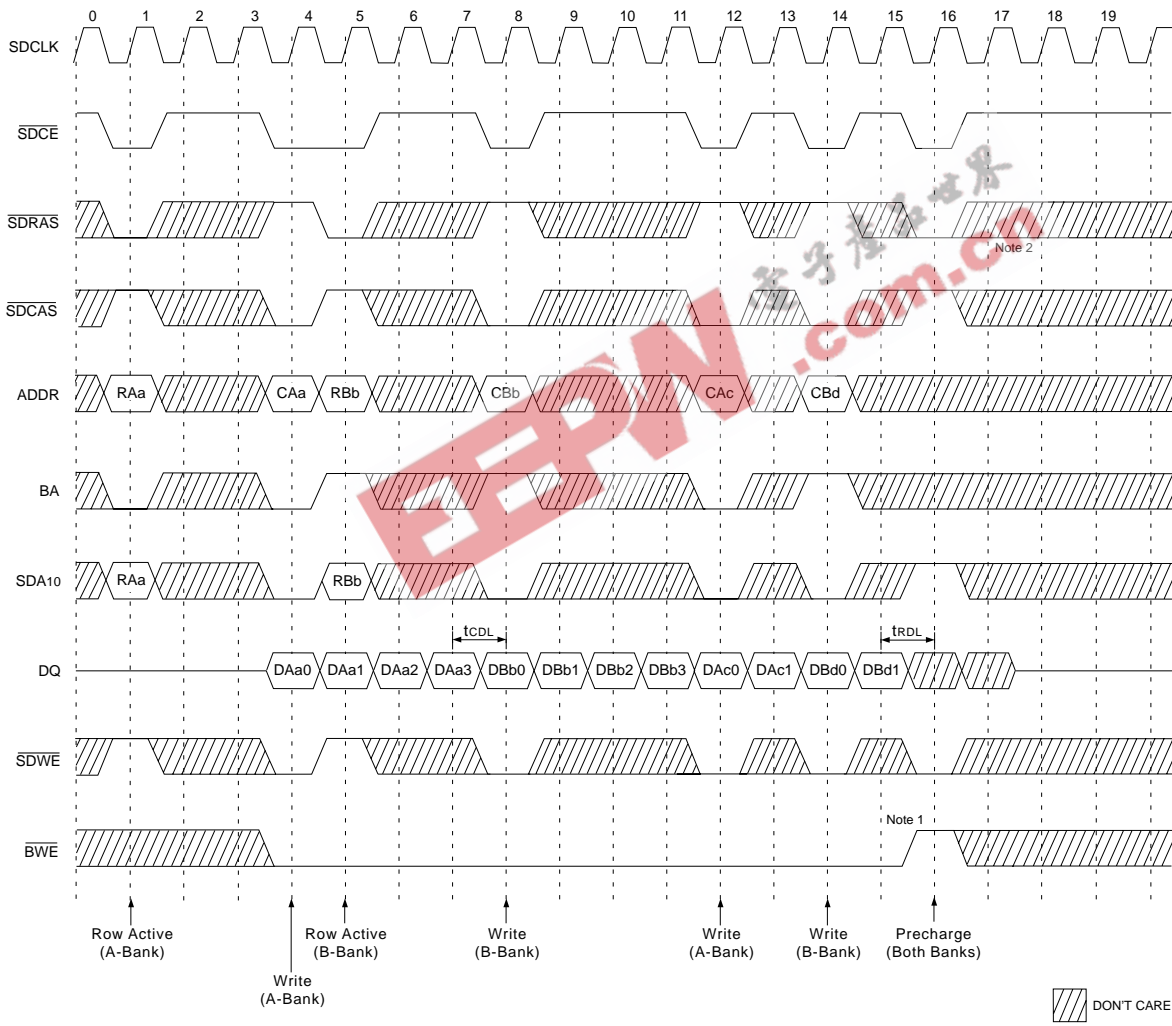


NOTES:

- SDCE can be "don't care" when SDRAS, SDCAS and SDWE are high at the clock going high edge.
- To interrupt a burst read by Row precharge, both the read and the precharge banks must be the same.



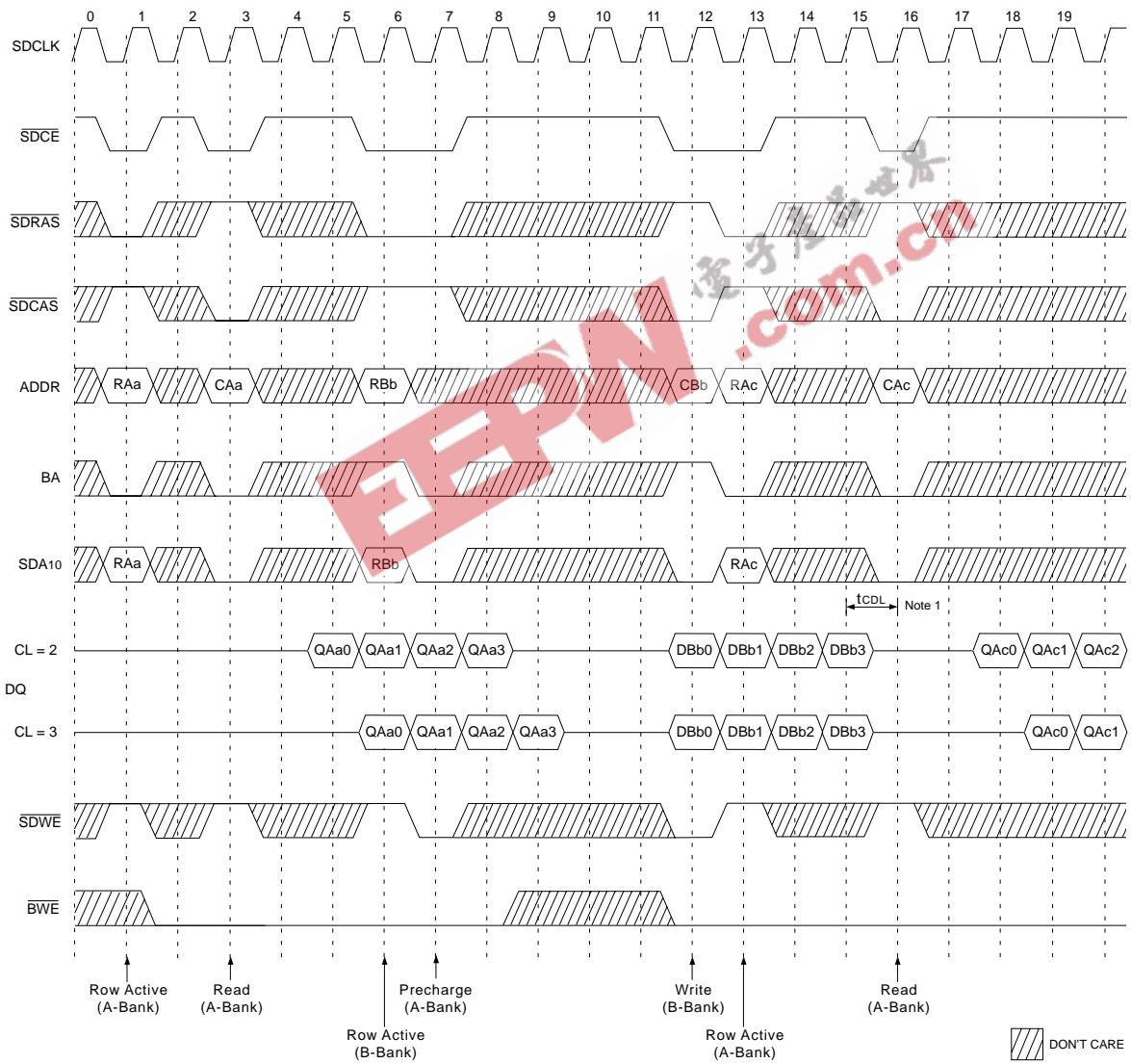
FIG. 10 SDRAM PAGE WRITE CYCLE AT DIFFERENT BANK @ BURST LENGTH = 4



- NOTES:**
1. To interrupt burst write by Row precharge, BWE should be asserted to mask invalid input data.
  2. To interrupt a burst read by Row precharge, both the read and the precharge banks must be the same.



FIG. 11 SDRAM READ & WRITE CYCLE AT DIFFERENT BANK @ BURST LENGTH = 4

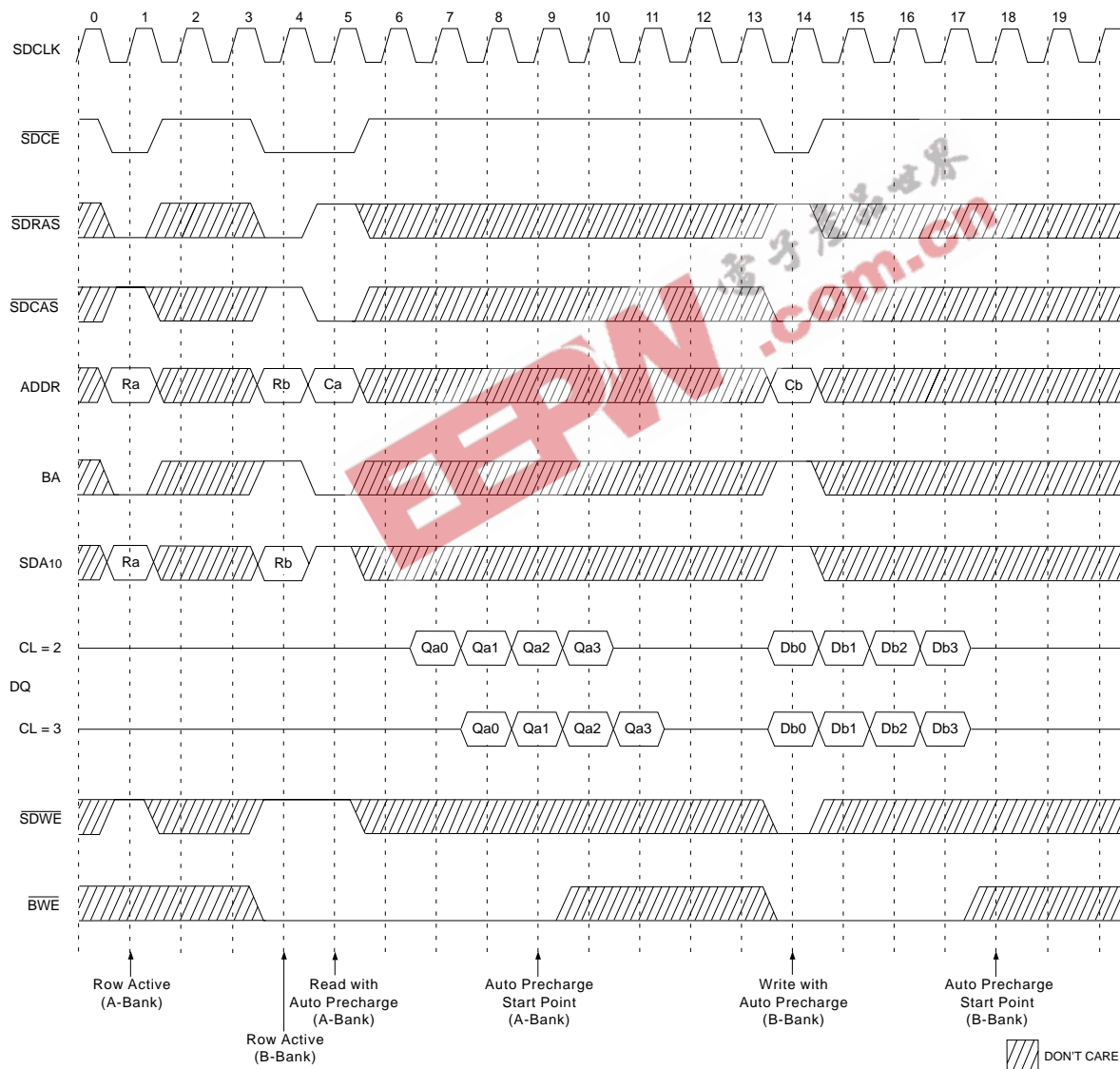


NOTES:

1. tCDL should be met to complete write.



FIG. 12 SDRAM READ & WRITE CYCLE WITH AUTO PRECHARGE @ BURST LENGTH = 4

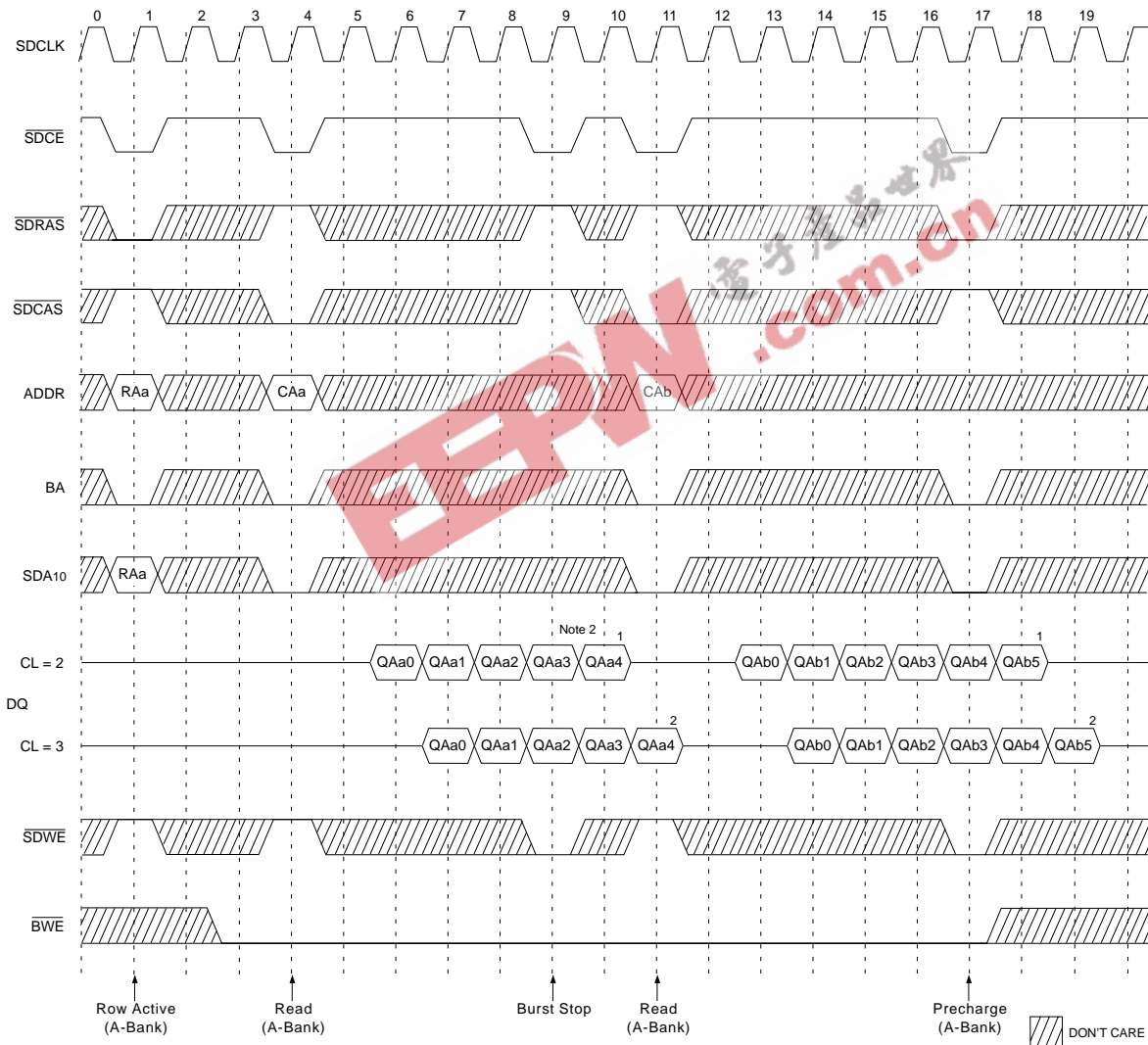


NOTES:

1. t<sub>CDL</sub> should be controlled to meet minimum t<sub>RAS</sub> before internal precharge start. (In the case of Burst Length = 1 & 2 and BRSW mode)



**FIG. 13 SDRAM READ INTERRUPTED BY PRECHARGE COMMAND & READ BURST STOP @ BURST LENGTH = FULL PAGE**

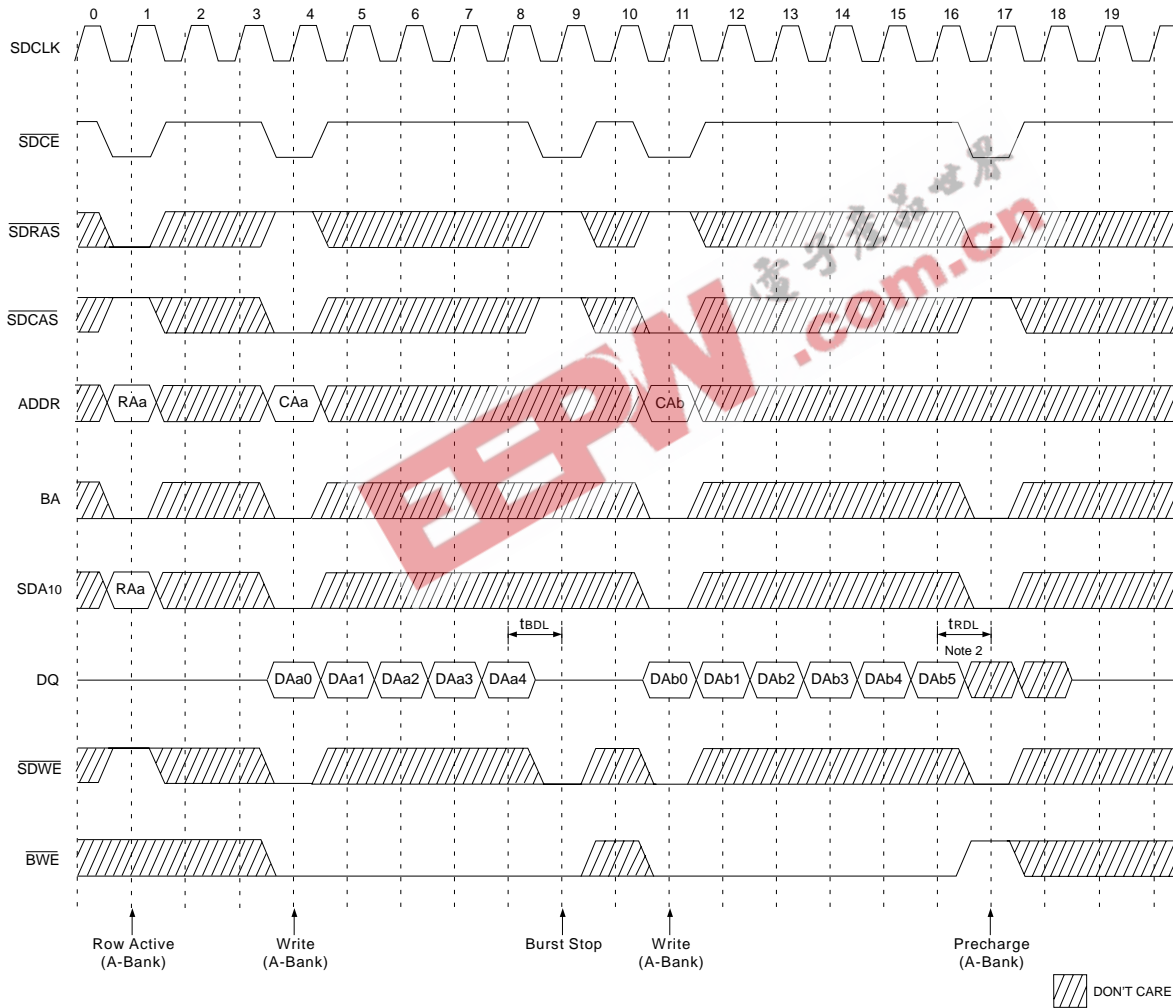


**NOTES:**

1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
2. About the valid DQs after burst stop, it is the same as the case of SDRAS interrupt. Both cases are illustrated in the above timing diagram. See the label 1, 2 on each of them. But at burst write, burst stop and SDRAS interrupt should be compared carefully. Refer to the timing diagram of "Full page write burst stop cycle".
3. Burst stop is valid at every burst length.



**FIG. 14 SDRAM WRITE INTERRUPTED BY PRECHARGE COMMAND & WRITE BURST STOP @ BURST LENGTH = FULL PAGE**

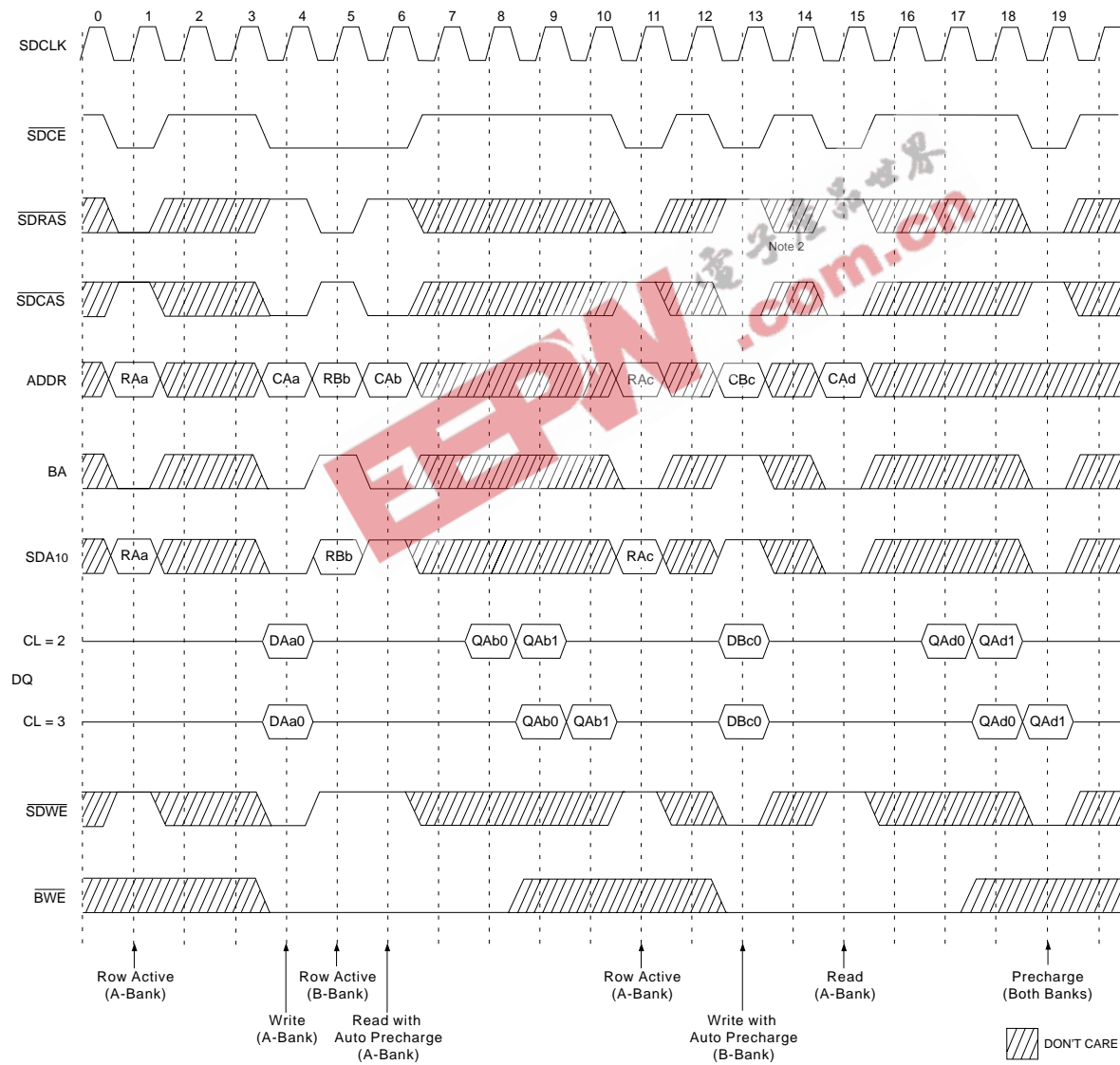


**NOTES:**

1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of  $t_{rDL}$ .  
**BWE** at write interrupt by precharge command is needed to prevent invalid write.  
**BWE** should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
3. Burst stop is valid at every burst length.



FIG. 15 SDRAM BURST READ SINGLE BIT WRITE CYCLE @ BURST LENGTH = 2



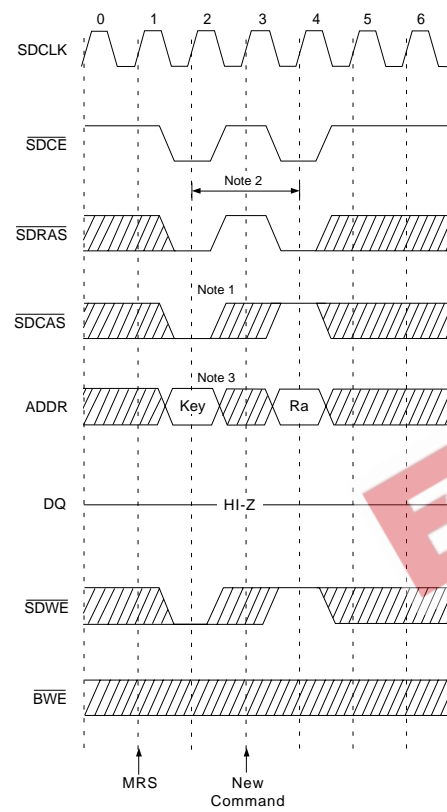
NOTES:

1. BRSW modes enabled by setting A9 "High" at MRS (Mode Register Set).  
At the BRSW Mode, the burst length at Write is fixed to "1" regardless of programmed burst length.
2. When BRSW write command with auto precharge is executed, keep it in mind that  $t_{RAS}$  should not be violated. Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command, the next cycle starts the precharge.

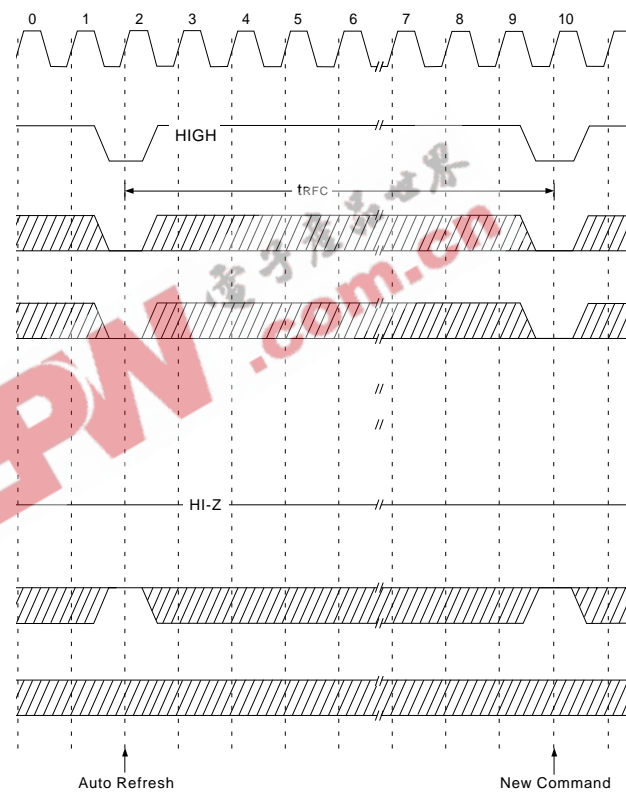




**FIG. 16**  
**SDRAM MODE REGISTER SET CYCLE**



**SDRAM AUTO REFRESH CYCLE**



\*Both banks precharge should be completed before Mode Register Set cycle and Auto refresh cycle.

**NOTES:**

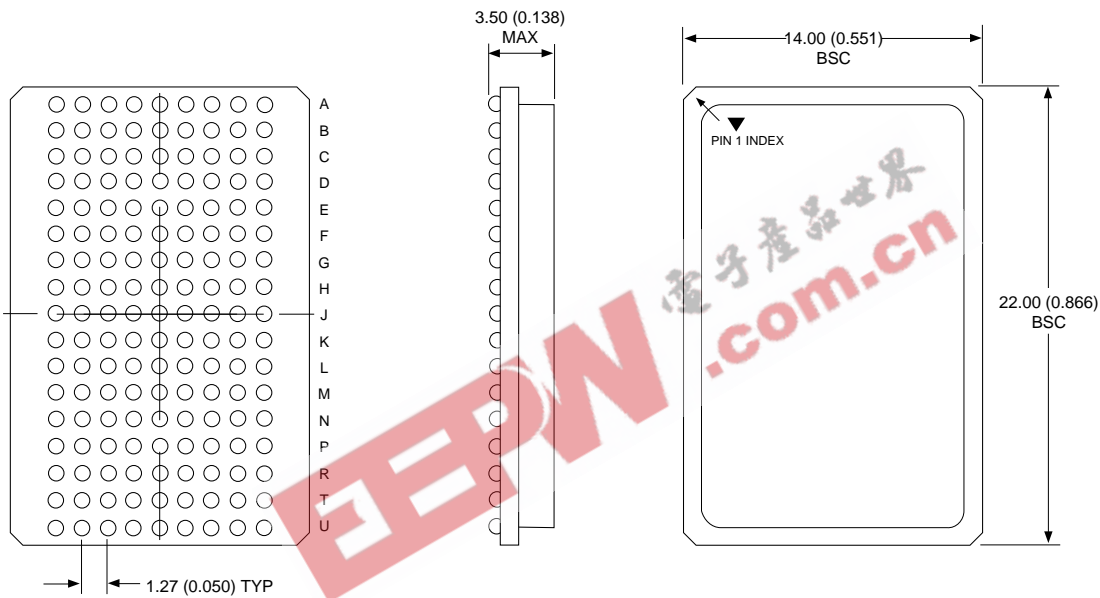
**MODE REGISTER SET CYCLE**

1. SDCE, SDRAS, SDCAS & SDWE activation at the same clock cycle with address key will set internal mode register.
2. Minimum 2 clock cycles should be met before new SDRAS activation.
3. Please refer to Mode Register Set Table.

DONT CARE



**PACKAGE DESCRIPTION: 153 LEAD BGA (17 x 9 BALL ARRAY)  
JEDEC MO-163**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

**ORDERING INFORMATION**

**COMMERCIAL (0°C ≤ T<sub>A</sub> ≤ 70°C)**

Part Number	SSRAM Access	SDRAM Access
WED9LC6416V2012BC	200MHz	125MHz
WED9LC6416V2010BC	200MHz	100MHz
WED9LC6416V1612BC	166MHz	125MHz
WED9LC6416V1610BC	166MHz	100MHz
WED9LC6416V1512BC	150MHz	125MHz
WED9LC6416V1510BC	150MHz	100MHz
WED9LC6416V1312BC	133MHz	125MHz
WED9LC6416V1310BC	133MHz	100MHz

**INDUSTRIAL (-40°C ≤ T<sub>A</sub> ≤ 85°C)**

Part Number	SSRAM Access	SDRAM Access
WED9LC6416V2012BI	200MHz	125MHz
WED9LC6416V2010BI	200MHz	100MHz
WED9LC6416V1612BI	166MHz	125MHz
WED9LC6416V1610BI	166MHz	100MHz
WED9LC6416V1512BI	150MHz	125MHz
WED9LC6416V1510BI	150MHz	100MHz
WED9LC6416V1312BI	133MHz	125MHz
WED9LC6416V1310BI	133MHz	100MHz



**FIG. 17**  
**INTERFACING THE TEXAS INSTRUMENTS TMS320C6x WITH**  
**THE WED9LC6416V (128Kx32 SSRAM/4Mx32 SDRAM)**

