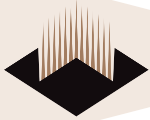

WHITE ELECTRONIC DESIGNS

**W3H32M64E-XSBX**

*ADVANCED**

# 32M x 64 DDR2 SDRAM 208 PBGA Multi-Chip Package

## FEATURES

- Data rate = 667*, 533, 400
- Package:
  - 208 Plastic Ball Grid Array (PBGA), 16 x 20mm
  - 1.0mm pitch
- DDR2 Data Rate = 667*, 533, 400
- Supply Voltage = 1.8V ± 0.1V
- Differential data strobe (DQS, DQS#) per byte
- Internal, pipelined, double data rate architecture
- 4-bit prefetch architecture
- DLL for alignment of DQ and DQS transitions with clock signal
- Four internal banks for concurrent operation (Per DDR2 SDRAM Die)
- Programmable Burst lengths: 4 or 8
- Auto Refresh and Self Refresh Modes
- On Die Termination (ODT)
- Adjustable data – output drive strength
- Programmable CAS latency: 3, 4 or 5
- Posted CAS additive latency: 0, 1, 2, 3 or 4
- Write latency = Read latency - 1* tCK
- Commercial, Industrial and Military Temperature Ranges
- Organized as 32M x 64, user configurable as 2 x 32M x 32
- Weight: W3H32M64E-XSBX - 2.5 grams typical

## BENEFITS

- 62% SPACE SAVINGS vs. FPBGA
- Reduced part count
- 42% I/O reduction vs FPBGA
- Reduced trace lengths for lower parasitic capacitance
- Suitable for hi-reliability applications
- Upgradeable to 64M x 64 density (contact factory for information)

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

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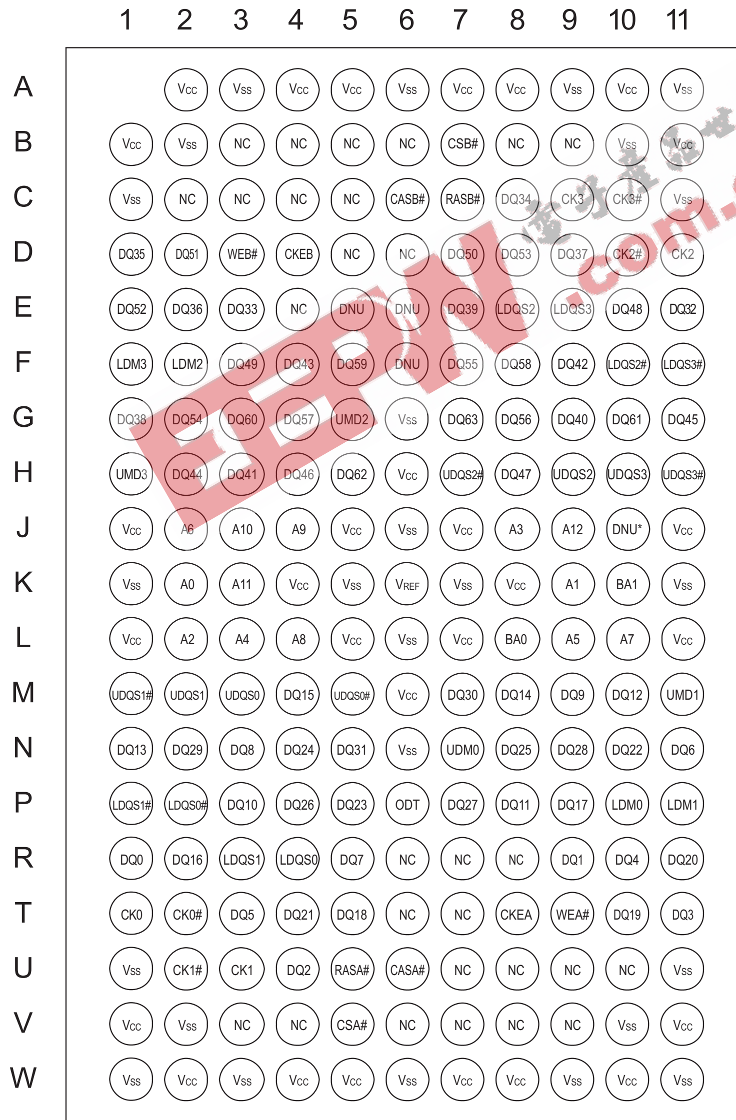
**FIGURE 1 – DENSITY COMPARISONS**

| | CSP Approach (mm) | Actual Size W3H32M64E-XSBX | SAVINGS |
|---|---|---|---|
| | 11.0 / 11.0 / 11.0 / 11.0; 19.0; 90 FBGA, 90 FBGA, 90 FBGA, 90 FBGA | 20; 16 | |
| **Area** | **4 x 209mm² = 836mm²** | **320mm²** | **62%** |
| **I/O Count** | **4 x 90 balls = 360 balls** | **208 Balls** | **42%** |

White Electronic Designs Corp. reserves the right to change products or specifications without notice.

## FIGURE 2 – FUNCTIONAL BLOCK DIAGRAM

## FIGURE 1 - PIN CONFIGURATION

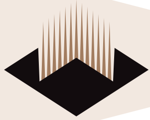



* Pin J10 is reserved for signal A13 on future upgrades.

## PACKAGE DIMENSION: 208 PLASTIC BALL GRID ARRAY (PBGA)



All linear dimensions are millimeters and parenthetically in inches





## ORDERING INFORMATION

**W 3H 32M 64 E - XXX SB X**

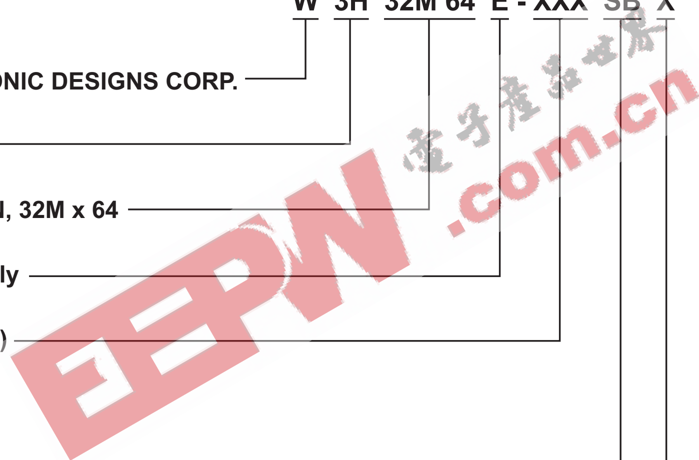
**WHITE ELECTRONIC DESIGNS CORP.** — W

**DDR2 SDRAM** — 3H

**CONFIGURATION, 32M x 64** — 32M 64

**1.8V Power Supply** — E

**DATA RATE (Mbs)** — XXX
400 = 400Mbs
533 = 533Mbs
667 = 667Mbs
Blank = No datarate specified for ES product [1]



**PACKAGE:** — SB
ES = Non Qualified Product [1]
SB = 208 Plastic Ball Grid Array (PBGA)

**DEVICE GRADE:** — X

| | | |
|---|---|---|
| M = | Military | -55°C to +125°C |
| I = | Industrial | -40°C to +85°C |
| C = | Commercial | 0°C to +70°C |

Blank = No temperature specified for ES product [1]

Note 1: W3H32M64E-ESSB is the only available product until completion of qualification.

White Electronic Designs Corp. reserves the right to change products or specifications without notice.

## Document Title

32M x 64 DDR2 SDRAM 208 PBGA Multi-Chip Package

## Revision History

| Rev # | History | Release Date | Status |
|---|---|---|---|
| Rev 0 | Initial Release | June 2005 | Advanced |
| Rev 1 | Changes (Pg. 1, 3, 5)<br>1.1 Change max package width to 16mm | August 2005 | Advanced |
| Rev 2 | Changes (pg. 1, 3, 6)<br>2.1 Pinout added | October 2005 | Advanced |
| Rev 3 | Changes (Pg. 1, 3, 6)<br>3.1 Change all $V_{CCQ}$ to $V_{CC}$ | October 2005 | Advanced |

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