



## 128Kx32 5V FLASH MODULE, SMD 5962-94716

### FEATURES

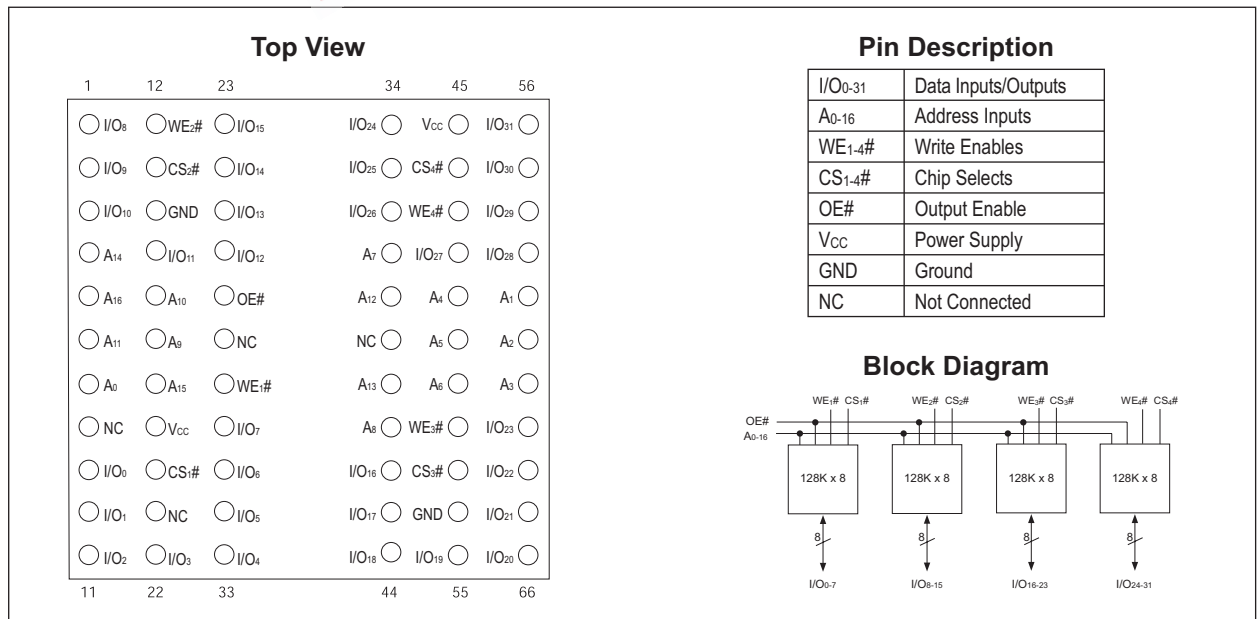
- Access Times of 50\*\*, 60, 70, 90, 120, 150ns
- Packaging:
  - 66 pin, PGA Type, 1.075 inch square, Hermetic Ceramic HIP (Package 400)
  - 68 lead, Hermetic CQFP (G2U), 22.4mm (0.880 inch) square, 3.56mm (0.140 inch) high (Package 510)
  - 68 lead, Hermetic CQFP (G2L), 22.4mm (0.880 inch) square, 4.06mm (0.160 inch) high (Package 528)
- Sector Architecture
  - 8 equal size sectors of 16KBytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- 100,000 Erase/Program Cycles Typical, 0°C to +70°C
- Organized as 128Kx32
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Programming. 5V ± 10% Supply
- Low Power CMOS, 1mA Standby Typical
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Page Program Operation and Internal Program Control Time
- Weight
  - WF128K32-XG2LX5 - 8 grams typical
  - WF128K32-XG2UX5 - 8 grams typical
  - WF128K32-XH1X5 - 13 grams typical

Note: For programming information refer to Flash Programming 1M5 Application Note.

\* This product is subject to change without notice.

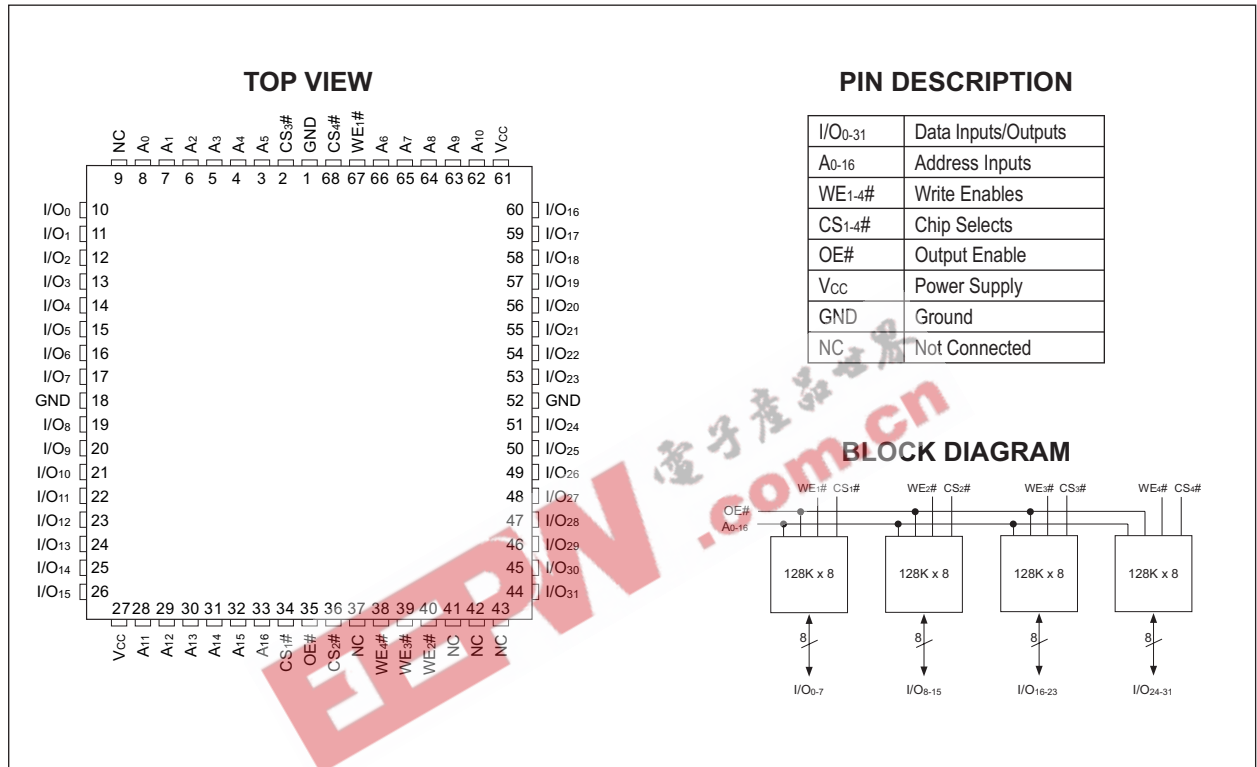
\*\* The access time of 50ns is available in Industrial and Commercial temperature ranges only.

**FIGURE 1 – PIN CONFIGURATION FOR WF128K32N-XH1X5**





**FIGURE 3 – PIN CONFIGURATION FOR WF128K32-XG2UX5 AND WF128K32-XG2LX5**





**ABSOLUTE MAXIMUM RATINGS (1)**

| Parameter  |                    | Unit |
|--|--------------------|------|
| Operating Temperature                                | -55 to +125        | °C   |
| Supply Voltage Range (V <sub>CC</sub> )              | -2.0 to +7.0       | V    |
| Signal voltage range (any pin except A9) (2)         | -2.0 to +7.0       | V    |
| Storage Temperature Range                            | -65 to +150        | °C   |
| Lead Temperature (soldering, 10 seconds)             | +300               | °C   |
| Data Retention Mil Temp                              | 10 years           |      |
| Endurance (write/erase cycles) Mil Temp              | 10,000 cycles min. |      |
| A9 Voltage for sector protect (V <sub>ID</sub> ) (3) | -2.0 to +14.0      | V    |

NOTES:

- Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot V<sub>SS</sub> to -2.0 V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is V<sub>CC</sub> + 0.5V. During voltage transitions, outputs may overshoot to V<sub>CC</sub> + 2.0 V for periods of up to 20ns.
- Minimum DC input voltage on A9 pin is -0.5V. During voltage transitions, A9 may overshoot V<sub>SS</sub> to -2V for periods of up to 20ns. Maximum DC input voltage on A9 is +13.5V which may overshoot to 14.0 V for periods up to 20ns.

**RECOMMENDED OPERATING CONDITIONS**

| Parameter                     | Symbol          | Min  | Max                   | Unit |
|-------------------------------|-----------------|------|-----------------------|------|
| Supply Voltage                | V <sub>CC</sub> | 4.5  | 5.5                   | V    |
| Input High Voltage            | V <sub>IH</sub> | 2.0  | V <sub>CC</sub> + 0.3 | V    |
| Input Low Voltage             | V <sub>IL</sub> | -0.5 | +0.8                  | V    |
| Operating Temp. (Mil.)        | T <sub>A</sub>  | -55  | +125                  | °C   |
| A9 Voltage for Sector Protect | V <sub>ID</sub> | 11.5 | 12.5                  | V    |

**CAPACITANCE**

T<sub>a</sub> = +25°C

| Parameter                 | Symbol           | Conditions                         | Max | Unit |
|---------------------------|------------------|------------------------------------|-----|------|
| OE# capacitance           | C <sub>OE</sub>  | V <sub>IN</sub> = 0V, f = 1.0 MHz  | 50  | pF   |
| WE1-4# capacitance        | C <sub>WE</sub>  | V <sub>IN</sub> = 0V, f = 1.0 MHz  | 20  | pF   |
| HIP (PGA) H1              |                  |                                    | 20  | pF   |
| CQFP G2U/G2L              |                  |                                    | 15  | pF   |
| CS1-4# capacitance        | C <sub>CS</sub>  | V <sub>IN</sub> = 0V, f = 1.0 MHz  | 20  | pF   |
| Data# I/O capacitance     | C <sub>I/O</sub> | V <sub>I/O</sub> = 0V, f = 1.0 MHz | 20  | pF   |
| Address input capacitance | C <sub>AD</sub>  | V <sub>IN</sub> = 0V, f = 1.0 MHz  | 50  | pF   |

This parameter is guaranteed by design but not tested.

**DC CHARACTERISTICS – CMOS COMPATIBLE**

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

| Parameter   | Symbol             | Conditions  | Min                    | Max  | Unit |
|---|--------------------|---|------------------------|------|------|
| Input Leakage Current                                   | I <sub>LI</sub>    | V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub> |                        | 10   | µA   |
| Output Leakage Current                                  | I <sub>LOx32</sub> | V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub> |                        | 10   | µA   |
| V <sub>CC</sub> Active Current for Read (1)             | I <sub>CC1</sub>   | CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub>                   |                        | 140  | mA   |
| V <sub>CC</sub> Active Current for Program or Erase (2) | I <sub>CC2</sub>   | CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub>                   |                        | 200  | mA   |
| V <sub>CC</sub> Standby Current                         | I <sub>CC3</sub>   | V <sub>CC</sub> = 5.5, CS# = V <sub>IH</sub> , f = 5MHz         |                        | 6.5  | mA   |
| V <sub>CC</sub> Static Current                          | I <sub>CC4</sub>   | V <sub>CC</sub> = 5.5, CS# = V <sub>IH</sub>                    |                        | 0.6  | mA   |
| Output Low Voltage                                      | V <sub>OL</sub>    | I <sub>OL</sub> = 8.0 mA, V <sub>CC</sub> = 4.5                 |                        | 0.45 | V    |
| Output High Voltage                                     | V <sub>OH1</sub>   | I <sub>OH</sub> = -2.5 mA, V <sub>CC</sub> = 4.5                | 0.85 x V <sub>CC</sub> |      | V    |
| Output High Voltage                                     | V <sub>OH2</sub>   | I <sub>OH</sub> = -100 µA, V <sub>CC</sub> = 4.5                | V <sub>CC</sub> - 0.4  |      | V    |
| Low V <sub>CC</sub> Lock Out Voltage                    | V <sub>LKO</sub>   |   | 3.2                    |      | V    |

NOTES:

- The I<sub>CC</sub> current listed includes both the DC operating current and the frequency dependent component (at 5 MHz).  
The frequency component typically is less than 2 mA/MHz, with OE# at V<sub>IH</sub>.
- I<sub>CC</sub> active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions: V<sub>IL</sub> = 0.3V, V<sub>IH</sub> = V<sub>CC</sub> - 0.3V

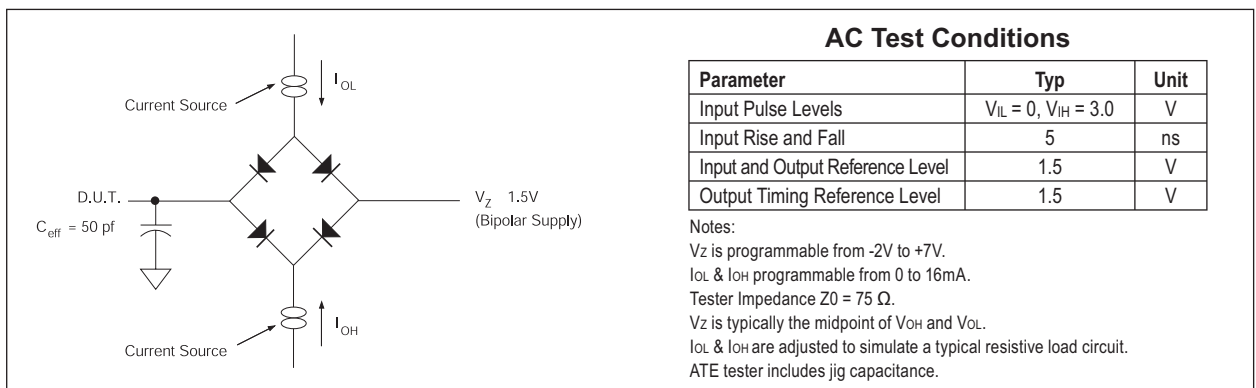


**AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, CS# CONTROLLED**

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

| Parameter                         | Symbol             |                  | -50 |      | -60 |      | -70 |      | -90 |      | -120 |      | -150 |      | Unit |
|-----------------------------------|--------------------|------------------|-----|------|-----|------|-----|------|-----|------|------|------|------|------|------|
|                                   | Min                | Max              | Min | Max  | Min | Max  | Min | Max  | Min | Max  | Min  | Max  | Min  | Max  |      |
| Write Cycle Time                  | t <sub>AVAV</sub>  | t <sub>WC</sub>  | 50  |      | 60  |      | 70  |      | 90  |      | 120  |      | 150  |      | ns   |
| WE# Setup Time                    | t <sub>WLEL</sub>  | t <sub>WS</sub>  | 0   |      | 0   |      | 0   |      | 0   |      | 0    |      | 0    |      | ns   |
| CS# Pulse Width                   | t <sub>LELH</sub>  | t <sub>CP</sub>  | 25  |      | 30  |      | 35  |      | 45  |      | 50   |      | 50   |      | ns   |
| Address Setup Time                | t <sub>AVEL</sub>  | t <sub>AS</sub>  | 0   |      | 0   |      | 0   |      | 0   |      | 0    |      | 0    |      | ns   |
| Data Setup Time                   | t <sub>DVEH</sub>  | t <sub>DS</sub>  | 25  |      | 30  |      | 30  |      | 45  |      | 50   |      | 50   |      | ns   |
| Data Hold Time                    | t <sub>EHDX</sub>  | t <sub>DH</sub>  | 0   |      | 0   |      | 0   |      | 0   |      | 0    |      | 0    |      | ns   |
| Address Hold Time                 | t <sub>ELAX</sub>  | t <sub>AH</sub>  | 40  |      | 45  |      | 45  |      | 45  |      | 50   |      | 50   |      | ns   |
| WE# Hold from WE# High            | t <sub>EHWH</sub>  | t <sub>WH</sub>  | 0   |      | 0   |      | 0   |      | 0   |      | 0    |      | 0    |      | ns   |
| CS# Pulse Width High              | t <sub>EHEL</sub>  | t <sub>CPH</sub> | 20  |      | 20  |      | 20  |      | 20  |      | 20   |      | 20   |      | ns   |
| Duration of Programming Operation | t <sub>WHWH1</sub> |                  | 14  |      | 14  |      | 14  |      | 14  |      | 14   |      | 14   |      | μs   |
| Duration of Erase Operation       | t <sub>WHWH2</sub> |                  | 2.2 | 60   | 2.2 | 60   | 2.2 | 60   | 2.2 | 60   | 2.2  | 60   | 2.2  | 60   | sec  |
| Read Recovery before Write        | t <sub>GHLEL</sub> |                  | 0   |      | 0   |      | 0   |      | 0   |      | 0    |      | 0    |      | ns   |
| Chip Programming Time             |                    |                  |     | 12.5 |     | 12.5 |     | 12.5 |     | 12.5 |      | 12.5 |      | 12.5 | sec  |

FIGURE 4 – AC TEST CIRCUIT





**AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, WE# CONTROLLED**

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

| Parameter                                    | Symbol             |                  | -50 |      | -60 |      | -70 |      | -90 |      | -120 |      | -150 |      | Unit |
|--|--------------------|------------------|-----|------|-----|------|-----|------|-----|------|------|------|------|------|------|
|  |                    |                  | Min | Max  | Min | Max  | Min | Max  | Min | Max  | Min  | Max  | Min  | Max  |      |
| Write Cycle Time                             | t <sub>AVAV</sub>  | t <sub>WC</sub>  | 50  |      | 60  |      | 70  |      | 90  |      | 120  |      | 150  |      | ns   |
| Chip Select Setup Time                       | t <sub>ELWL</sub>  | t <sub>CS</sub>  | 0   |      | 0   |      | 0   |      | 0   |      | 0    |      | 0    |      | ns   |
| Write Enable Pulse Width                     | t <sub>WLWH</sub>  | t <sub>WP</sub>  | 25  |      | 30  |      | 35  |      | 45  |      | 50   |      | 50   |      | ns   |
| Address Setup Time                           | t <sub>AVWL</sub>  | t <sub>AS</sub>  | 0   |      | 0   |      | 0   |      | 0   |      | 0    |      | 0    |      | ns   |
| Data Setup Time                              | t <sub>DVWH</sub>  | t <sub>DS</sub>  | 25  |      | 30  |      | 30  |      | 45  |      | 50   |      | 50   |      | ns   |
| Data Hold Time                               | t <sub>WHDX</sub>  | t <sub>DH</sub>  | 0   |      | 0   |      | 0   |      | 0   |      | 0    |      | 0    |      | ns   |
| Address Hold Time                            | t <sub>WLAX</sub>  | t <sub>AH</sub>  | 40  |      | 45  |      | 45  |      | 45  |      | 50   |      | 50   |      | ns   |
| Chip Select Hold Time                        | t <sub>WHEH</sub>  | t <sub>CH</sub>  | 0   |      | 0   |      | 0   |      | 0   |      | 0    |      | 0    |      | ns   |
| Write Enable Pulse Width High                | t <sub>WHWL</sub>  | t <sub>WPH</sub> | 20  |      | 20  |      | 20  |      | 20  |      | 20   |      | 20   |      | ns   |
| Duration of Byte Programming Operation (min) | t <sub>WHWH1</sub> |                  | 14  |      | 14  |      | 14  |      | 14  |      | 14   |      | 14   |      | μs   |
| Sector Erase Time                            | t <sub>WHWH2</sub> |                  | 2.2 | 60   | 2.2 | 60   | 2.2 | 60   | 2.2 | 60   | 2.2  | 60   | 2.2  | 60   | sec  |
| Read Recovery Time Before Write              | t <sub>GHWL</sub>  |                  | 0   |      | 0   |      | 0   |      | 0   |      | 0    |      | 0    |      | ns   |
| V <sub>CC</sub> Setup Time                   | t <sub>VCS</sub>   |                  | 50  |      | 50  |      | 50  |      | 50  |      | 50   |      | 50   |      | μs   |
| Chip Programming Time                        |                    |                  |     | 12.5 |     | 12.5 |     | 12.5 |     | 12.5 |      | 12.5 |      | 12.5 | sec  |
| Output Enable Setup Time                     | t <sub>OES</sub>   |                  | 0   |      | 0   |      | 0   |      | 0   |      | 0    |      | 0    |      | ns   |
| Output Enable Hold Time (1)                  | t <sub>OEH</sub>   |                  | 10  |      | 10  |      | 10  |      | 10  |      | 10   |      | 10   |      | ns   |

1. For Toggle and Data Polling.

**AC CHARACTERISTICS – READ ONLY OPERATIONS**

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

| Parameter   | Symbol            |                  | -50 |     | -60 |     | -70 |     | -90 |     | -120 |     | -150 |     | Unit |
|---|-------------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|------|-----|------|-----|------|
|   |                   |                  | Min | Max | Min | Max | Min | Max | Min | Max | Min  | Max | Min  | Max |      |
| Read Cycle Time   | t <sub>AVAV</sub> | t <sub>RC</sub>  | 50  |     | 60  |     | 70  |     | 90  |     | 120  |     | 150  |     | ns   |
| Address Access Time   | t <sub>AVQV</sub> | t <sub>ACC</sub> |     | 50  |     | 60  |     | 70  |     | 90  |      | 120 |      | 150 | ns   |
| Chip Select Access Time   | t <sub>ELQV</sub> | t <sub>CE</sub>  |     | 50  |     | 60  |     | 70  |     | 90  |      | 120 |      | 150 | ns   |
| OE# to Output Valid   | t <sub>GLQV</sub> | t <sub>OE</sub>  |     | 25  |     | 30  |     | 35  |     | 40  |      | 50  |      | 55  | ns   |
| Chip Select to Output High Z (1)                                | t <sub>EHQZ</sub> | t <sub>DF</sub>  |     | 20  |     | 20  |     | 20  |     | 25  |      | 30  |      | 35  | ns   |
| OE# High to Output High Z (1)                                   | t <sub>GHQZ</sub> | t <sub>DF</sub>  |     | 20  |     | 20  |     | 20  |     | 25  |      | 30  |      | 35  | ns   |
| Output Hold from Address, CS# or OE# Change, whichever is first | t <sub>AXQX</sub> | t <sub>OH</sub>  | 0   |     | 0   |     | 0   |     | 0   |     | 0    |     | 0    |     | ns   |

1. Guaranteed by design, not tested.



**FIGURE 5 – AC WAVEFORMS FOR READ OPERATIONS**

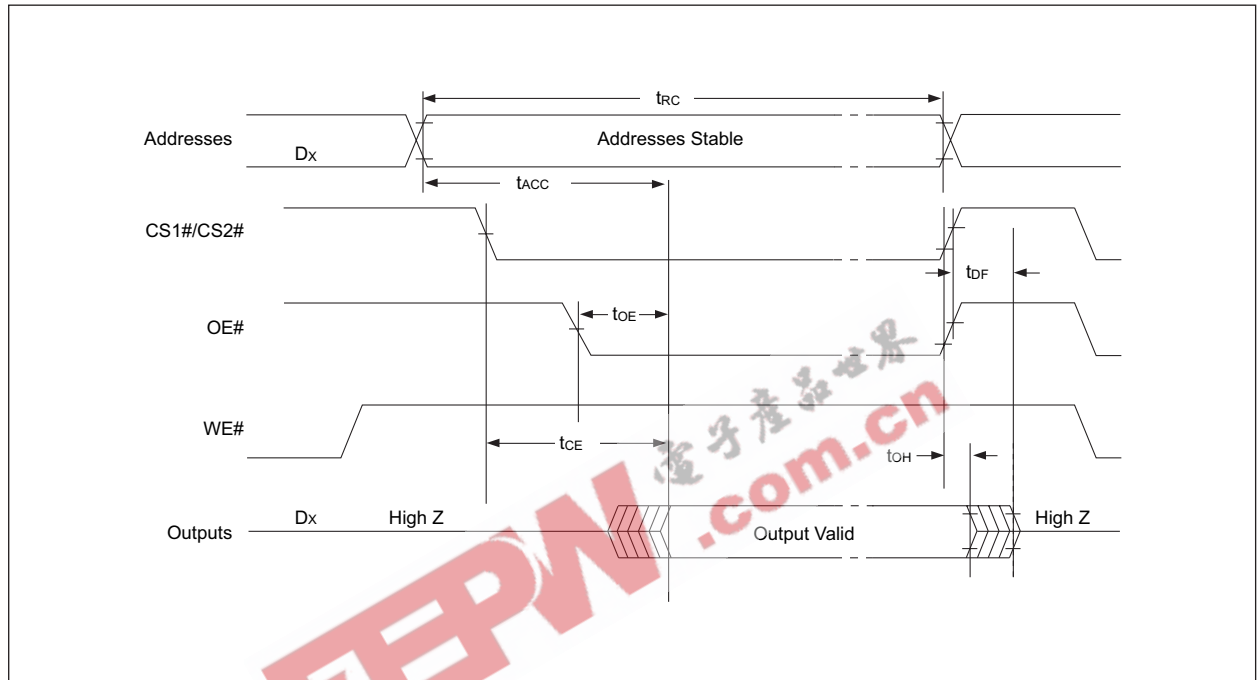




FIGURE 6 – WRITE/ERASE/PROGRAM OPERATION, WE# CONTROLLED



NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to the device (for each chip).
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.



FIGURE 7 – AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



Notes:

1. SA is the sector address for Sector Erase.





FIGURE 8 – AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS

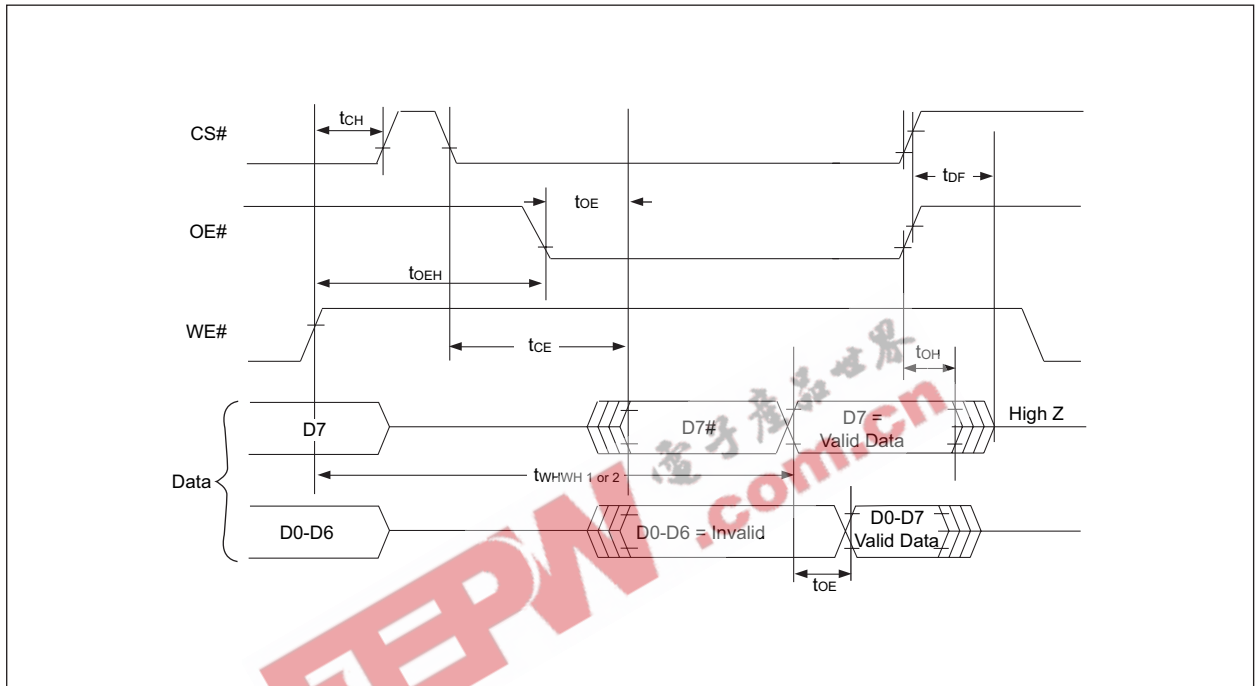
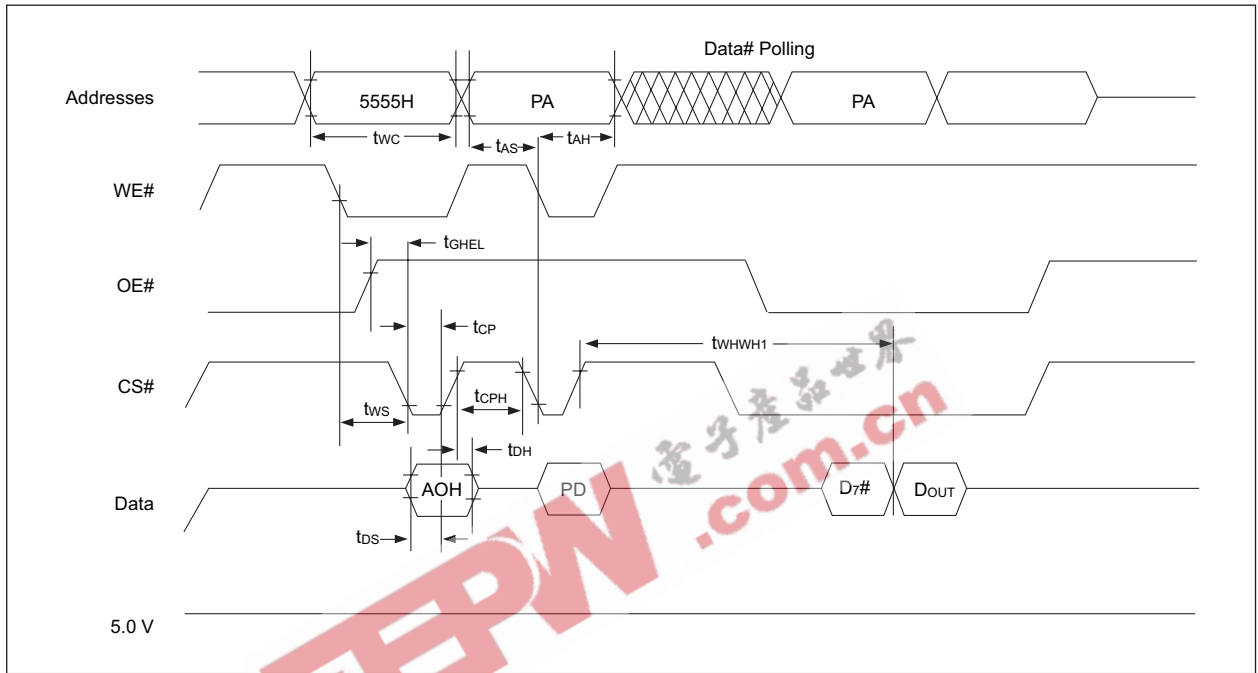




FIGURE 9 – WRITE/ERASE/PROGRAM OPERATION, CS# CONTROLLED

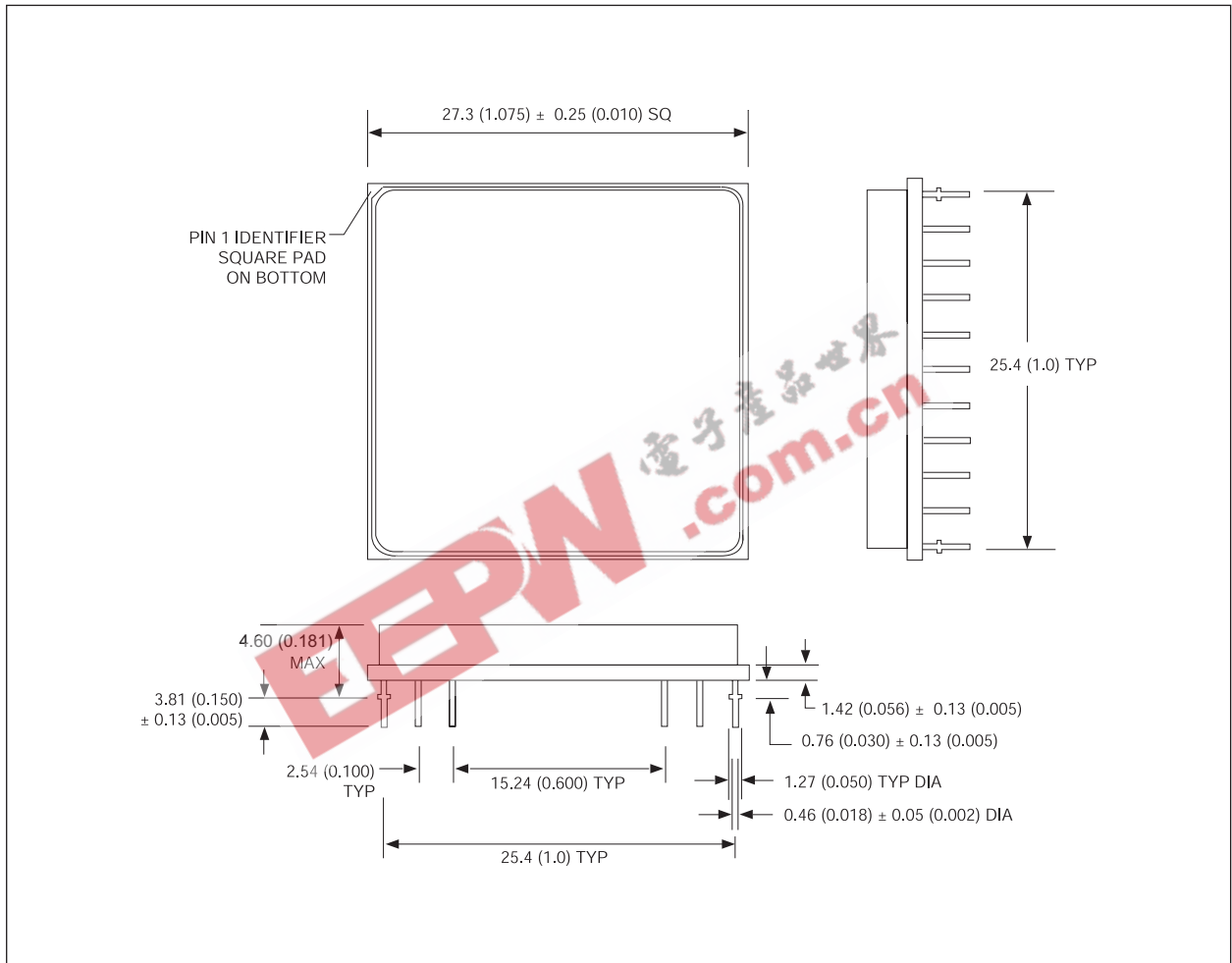


NOTES:

1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to the device (for each chip).
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.



**PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)**

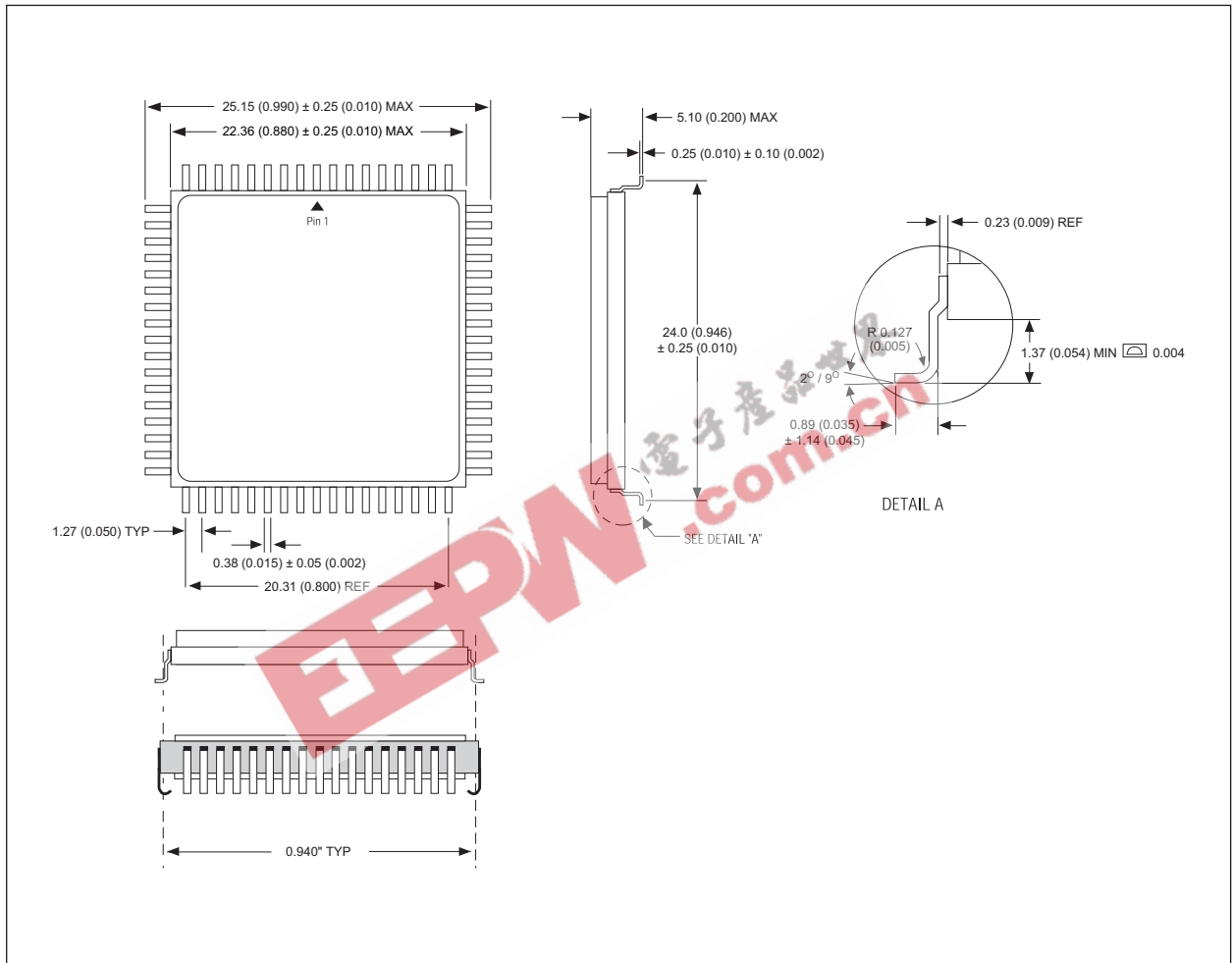


ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES





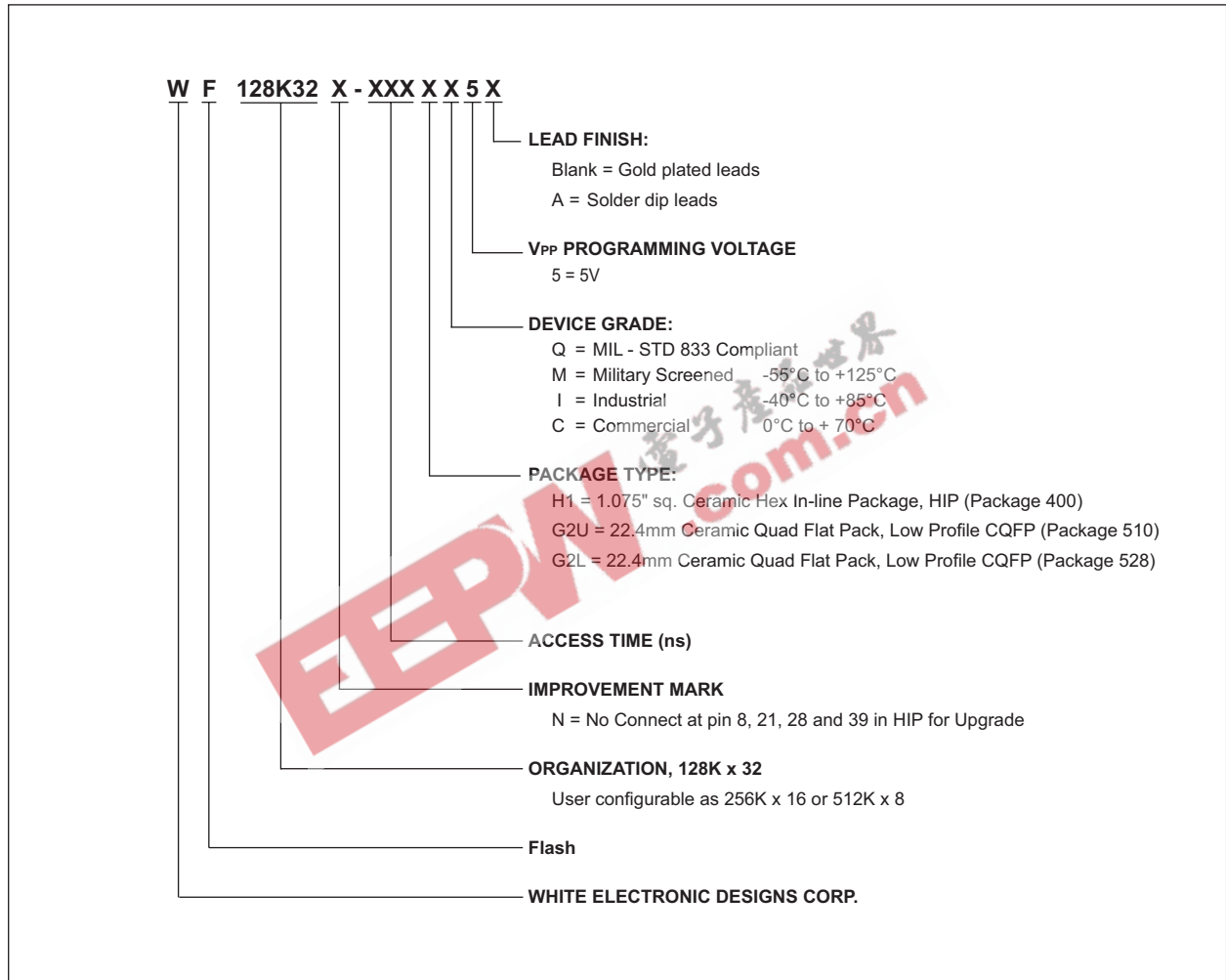
**PACKAGE 528 : 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2L)**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



**ORDERING INFORMATION**





| DEVICE TYPE     | SPEED | PACKAGE            | SMD NO.          |
|-----------------|-------|--------------------|------------------|
| 128K x 32 Flash | 150ns | 66 pin HIP (H1)    | 5962-94716 01H8X |
| 128K x 32 Flash | 120ns | 66 pin HIP (H1)    | 5962-94716 02H8X |
| 128K x 32 Flash | 90ns  | 66 pin HIP (H1)    | 5962-94716 03H8X |
| 128K x 32 Flash | 70ns  | 66 pin HIP (H1)    | 5962-94716 04H8X |
| 128K x 32 Flash | 60ns  | 66 pin HIP (H1)    | 5962-94716 05H8X |
| 128K x 32 Flash | 150ns | 68 lead CQFP (G2U) | 5962-94716 01HNX |
| 128K x 32 Flash | 120ns | 68 lead CQFP (G2U) | 5962-94716 02HNX |
| 128K x 32 Flash | 90ns  | 68 lead CQFP (G2U) | 5962-94716 03HNX |
| 128K x 32 Flash | 70ns  | 68 lead CQFP (G2U) | 5962-94716 04HNX |
| 128K x 32 Flash | 60ns  | 68 lead CQFP (G2U) | 5962-94716 05HNX |
| 128K x 32 Flash | 150ns | 68 lead CQFP (G2L) | 5962-94716 01HAX |
| 128K x 32 Flash | 120ns | 68 lead CQFP (G2L) | 5962-94716 02HAX |
| 128K x 32 Flash | 90ns  | 68 lead CQFP (G2L) | 5962-94716 03HAX |
| 128K x 32 Flash | 70ns  | 68 lead CQFP (G2L) | 5962-94716 04HAX |
| 128K x 32 Flash | 60ns  | 68 lead CQFP (G2L) | 5962-94716 05HAX |

Note 1: Package Not Recommended For New Design