512Kx32 SRAM 3.3V MULTICHIP PACKAGE

FEATURES

- Access Times of 15, 17, 20ns
- Low Voltage Operation
- Packaging
  - 66-pin, PGA Type, 1.075 inch square, Hermetic Ceramic HIP (Package 400)
  - 68 lead, 22.4mm (0.880 inch) CQFP, (G2U), 3.56mm (0.140"), (Package 510)
- Organized as 512Kx32; User Configurable as 2x512Kx16 or 4x512Kx8
- Commercial, Industrial and Military Temperature Ranges
- Low Voltage Operation:
  - 3.3V ± 10% Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Fully Static Operation:
  - No clock or refresh required.
- Three State Output.
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  WS512K32V-XG2UX - 8 grams typical
  WS512K32NV-XH1X - 13 grams typical

* This product is subject to change without notice.

PIN CONFIGURATION FOR WS512K32NV-XH1X

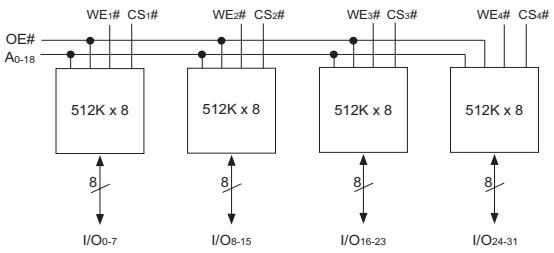
Top View

1	12	23		34	45	56
I/O8	WE2#	I/O15		I/O24	VCC	I/O31
I/O9	CS2#	I/O14		I/O25	CS4#	I/O30
I/O10	GND	I/O13		I/O26	WE4#	I/O29
A13	I/O11	I/O12		A6	I/O27	I/O28
A14	A10	OE#		A7	A3	A0
A15	A11	A18		NC	A4	A1
A16	A12	WE1#		A8	A5	A2
A17	VCC	I/O7		A9	WE3#	I/O23
I/O0	CS1#	I/O6		I/O16	CS3#	I/O22
I/O1	NC	I/O5		I/O17	GND	I/O21
I/O2	I/O3	I/O4		I/O18	I/O19	I/O20
11	22	33		44	55	66

Pin Description

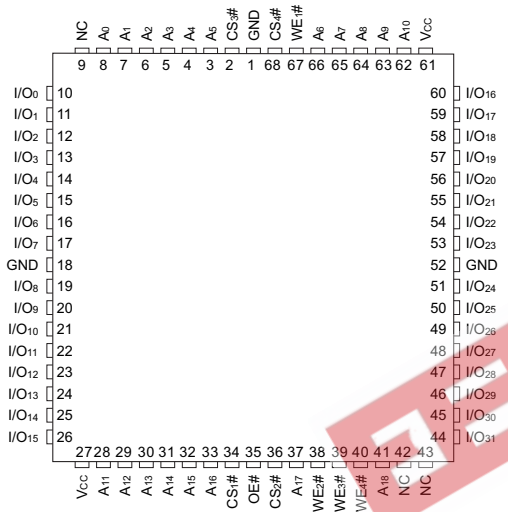
I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
WE1-4#	Write Enables
CS1-4#	Chip Selects
OE#	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

Block Diagram



PIN CONFIGURATION FOR WS512K32V-XG2UX

Top View



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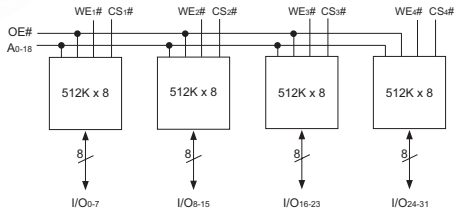


ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	4.6	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	4.6	V

TRUTH TABLE

CS	OE	WE	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C_{OE}	V_{IN} = 0V, f = 1.0 MHz	50	pF
WE1-4# capacitance	C_{WE}	V_{IN} = 0V, f = 1.0 MHz		pF
HIP (PGA)			20	
CQFP G2U			20	
CS_{1-4}# capacitance	C_{CS}	V_{IN} = 0V, f = 1.0 MHz	20	pF
Data# I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

V_{CC} = 3.3V ± 0.3V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	CS# = V_{IH}, OE# = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current	I_{CC} x 32	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz, V_{CC} = 3.6		400	mA
Standby Current	I_{SB}	CS# = V_{IH}, OE# = V_{IH}, f = 5MHz, V_{CC} = 3.6		200	mA
Output Low Voltage	V_{OL}	I_{OL} = 4.0mA		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V.
Contact factory for low power option.

AC CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter Read Cycle	Symbol	-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		ns
Address Access Time	t_{AA}		15		17		20	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns
Chip Select Access Time	t_{ACS}		15		17		20	ns
Output Enable to Output Valid	t_{OE}		8		8		10	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	1		1		1		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		8		8		10	ns
Output Disable to Output in High Z	t_{OHZ}[1]		8		8		10	ns

1. This parameter is guaranteed by design but not tested.

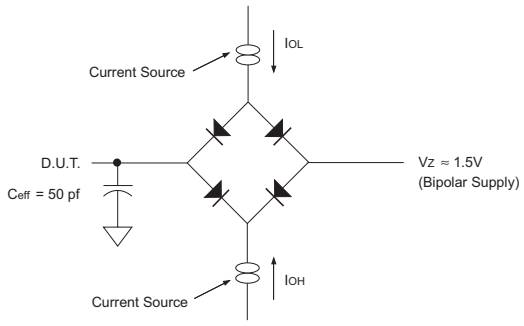
AC CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter Write Cycle	Symbol	-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		ns
Chip Select to End of Write	t_{CW}	12		12		14		ns
Address Valid to End of Write	t_{AW}	12		12		14		ns
Data Valid to End of Write	t_{DW}	9		9		10		ns
Write Pulse Width	t_{WP}	12		14		14		ns
Address Setup Time	t_{AS}	0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		ns
Output Active from End of Write	t_{OW}[1]	2		3		3		ns
Write Enable to Output in High Z	t_{WHZ}[1]		8		8		9	ns
Data Hold Time	t_{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

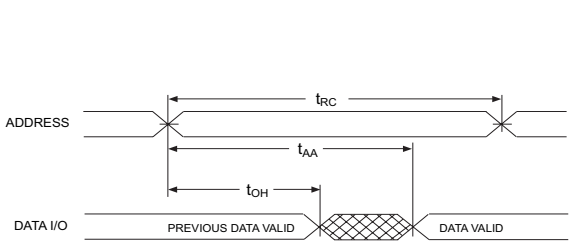


AC Test Conditions

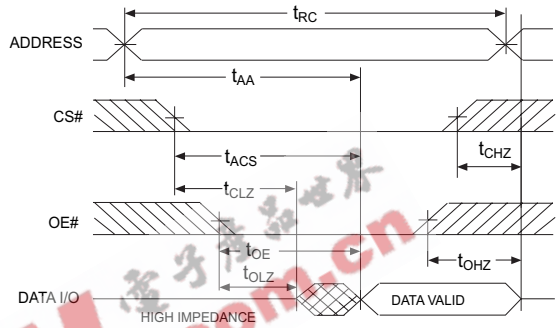
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

TIMING WAVEFORM - READ CYCLE

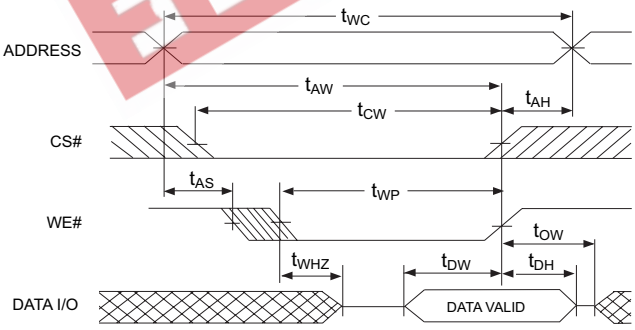


READ CYCLE 1 (CS# = OE# = V_{IL}, WE# = V_{IH})



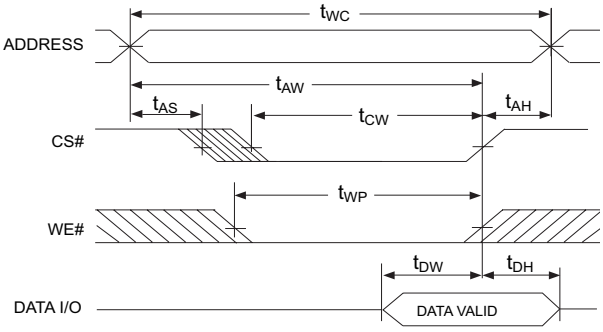
READ CYCLE 2 (WE# = V_{IH})

WRITE CYCLE - WE# CONTROLLED



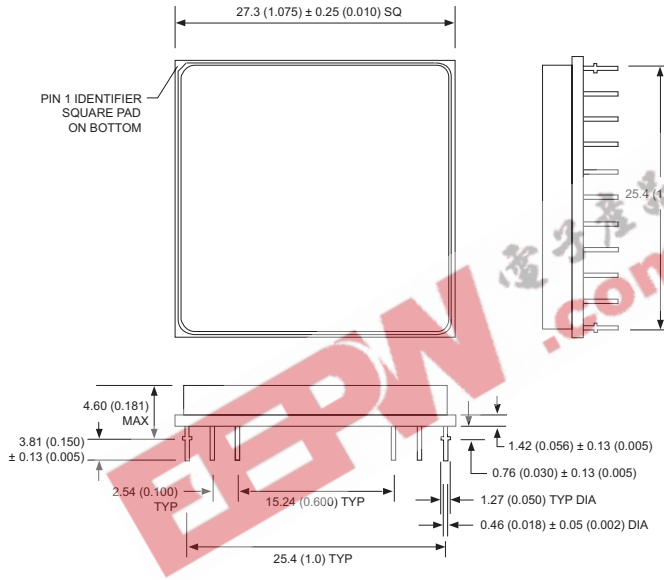
WRITE CYCLE 1, WE# CONTROLLED

WRITE CYCLE - CS# CONTROLLED



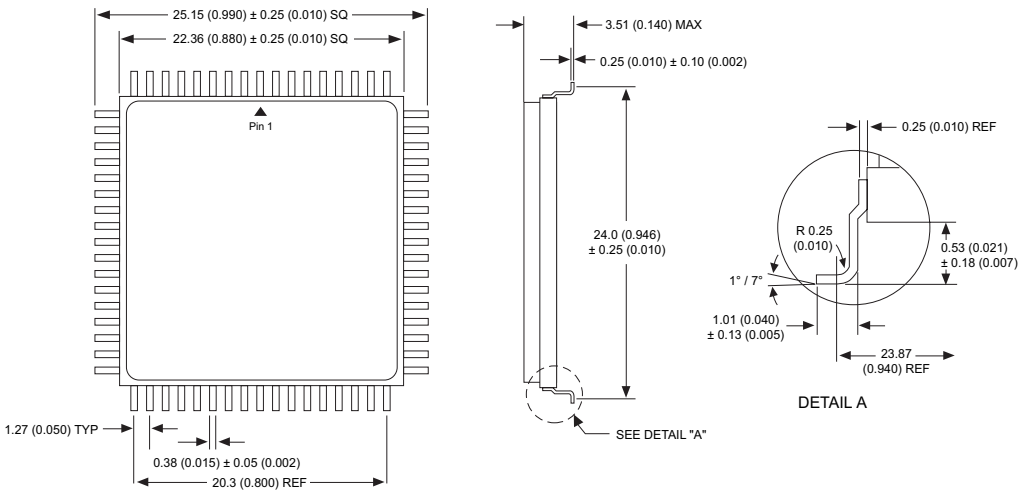
WRITE CYCLE 2, CS# CONTROLLED

PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 510: 68 LEAD, LOW PROFILE CERAMIC QUAD FLAT PACK, CQFP (G2U)



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ORDERING INFORMATION

W S 512K 32 X V - XXX X X X

WHITE ELECTRONIC DESIGNS CORP.

SRAM

ORGANIZATION, 512Kx32
User configurable as 2x512Kx16 or 4x512Kx8

IMPROVEMENT MARK:
N = No Connect at pin 21 and 39 in HIP for Upgrades (H1 only)

Low Voltage Supply 3.3V ± 10%

ACCESS TIME (ns)

PACKAGE TYPE:
H1 = 1.075" sq. Ceramic Hex In Line Package, HIP (Package 400)
G2U = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 510)

DEVICE GRADE:

M = Military	-55°C to +125°C
I = Industrial	-40°C to +85°C
C = Commercial	0°C to +70°C

LEAD FINISH:
Blank = Gold plated leads
A = Solder dip leads