32MB to 4GB Flash Card

FEATURES

- ATA compatibility
- Supports 3 variations of mode access
  - I/O Card Mode
  - Memory Card Mode
  - True- IDE Mode
- +5.5V / +3.0V single power supply.
- Internal Error Correction Logic
  - Data Interleave to 2 for each 256 Bytes.
  - Error Correction of 1 Byte random error per 128 Bytes of data.
  - Automatic on-the-fly, in-buffer error correction.
- Compatible with all PC Card Service and Socket Service.
- Integrated PC Card attribute memory of 256 Bytes(CIS).
- 4 PC Card function register support.
- Supports Host-side Write Protect.
- Automatic wake up from power-down on host reset or command write.
- Sector data transfers without microprocessor intervention.
- Operation Environment
  - Temperature — 0°C ~ 65°C
  - Humidity — 8% ~ 95%

DESCRIPTION

The WED7PxxxATA80xxC25 series ATA card is an ATA interface flash memory card based on flash technology. The ATA card is constructed with a flash disk controller chip and NAND-type flash memory device. Operates from a single 5-Volt or 3.3-Volt power source. The card is available in ATA type-2 form factor from 32MB to 4GB unformatted capacity. Being able to emulate IDE hard disk drives, WEDC's ATA card is a perfect choice for solid-state mass-storage in industrial applications.

* This product is subject to change without notice.

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PRODUCT TYPES

Card Density	Model No.
32MB	7P032ATA80xxC25
64MB	7P064ATA80xxC25
128MB	7P128ATA80xxC25
256MB	7P256ATA80xxC25
512MB	7P512ATA80xxC25
1024MB	7P1G0ATA80xxC25
2048MB	7P2G0ATA80xxC25
4096MB	7P4G0ATA80xxC25

xx = Housing
03 = WEDC logo
04 = No logo

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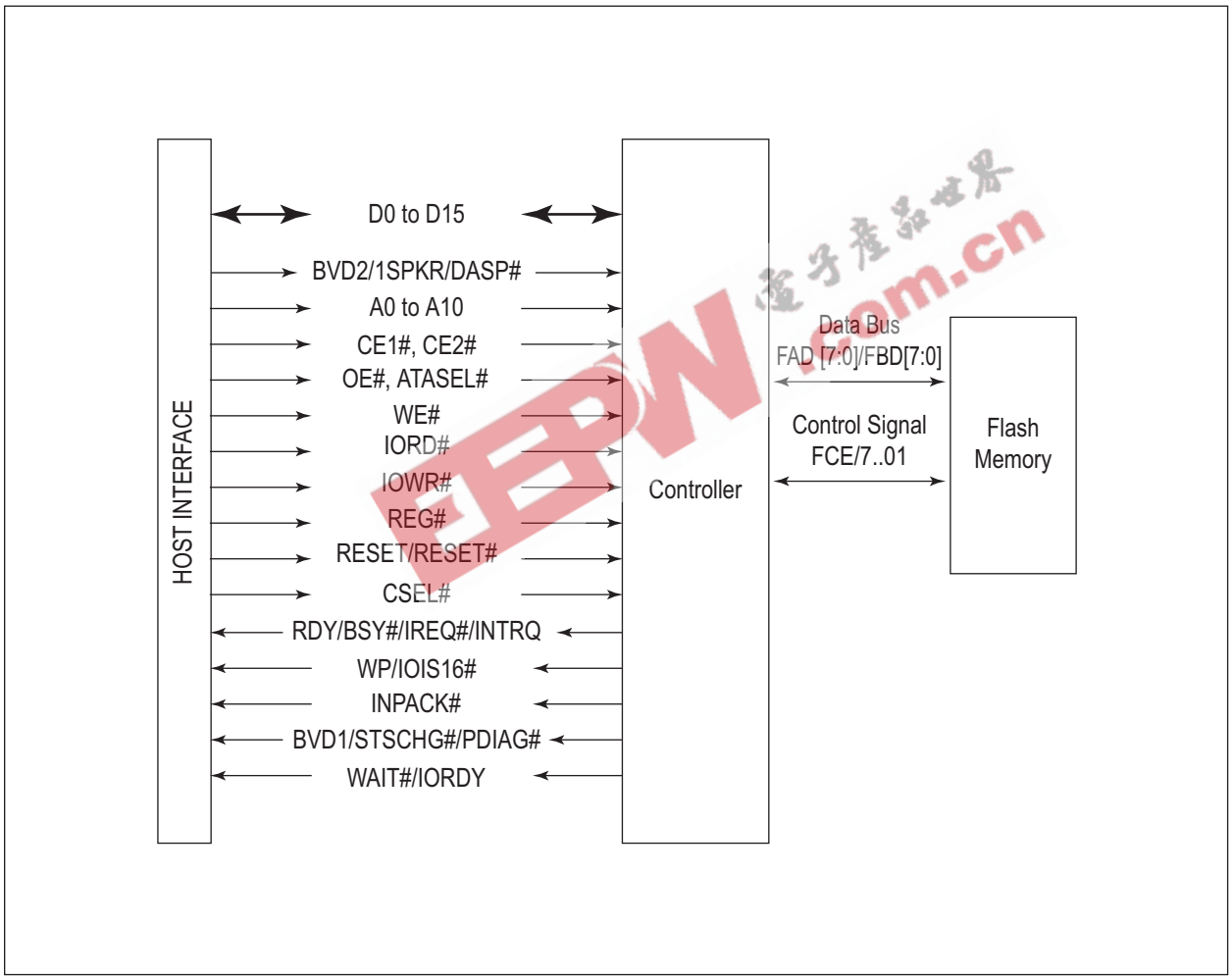
BLOCK DIAGRAM



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PIN ASSIGNMENTS AND PIN TYPE

	Memory card mode		I/O Card Mode		True IDE Mode	
Pin #	Signal Name	I/O	Signal Name	I/O	Signal Name	I/O
1	GND		GND		GND	
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	CE1#	I	CE1#	I	CE1#	I
8	A10	I	A10	I	A10	I
9	OE#	I	OE#	I	ATASEL#	I
10	N.C.	–	N.C.	–	N.C.	–
11	A9	I	A9	I	A9	I
12	A8	I	A8	I	A8	I
13	N.C.	–	N.C.	–	N.C.	–
14	N.C.	–	N.C.	–	N.C.	–
15	WE#	I	WE#	I	WE#	I
16	RDY/BSY	O	IREQ#	O	INTRQ	O
17	Vcc		Vcc		Vcc	
18	N.C.	–	N.C.	–	N.C.	–
19	N.C.	–	N.C.	–	N.C.	–
20	N.C.	–	N.C.	–	N.C.	–
21	N.C.	–	N.C.	–	N.C.	–
22	A7	I	A7	I	A7	I
23	A6	I	A6	I	A6	I
24	A5	I	A5	I	A5	I
25	A4	I	A4	I	A4	I
26	A3	I	A3	I	A3	I
27	A2	I	A2	I	A2	I
28	A1	I	A1	I	A1	I
29	A0	I	A0	I	A0	I
30	D0	I/O	D0	I/O	D0	I/O
31	D1	I/O	D1	I/O	D1	I/O
32	D2	I/O	D2	I/O	D2	I/O
33	WP	O	IOIS16#	O	IOIS16#	O
34	GND	–	GND	–	GND	–

	Memory card mode		I/O Card Mode		True IDE Mode	
Pin #	Signal Name	I/O	Signal Name	I/O	Signal Name	I/O
35	GND	–	GND	–	GND	–
36	CD1#	O	CD1#	O	CD1#	O
37	D11	I/O	D11	I/O	D11	I/O
38	D12	I/O	D12	I/O	D12	I/O
39	D13	I/O	D13	I/O	D13	I/O
40	D14	I/O	D14	I/O	D14	I/O
41	D15	I	D15	I	D15	I
42	CE2#	I	CE2#	I	CE2#	I
43	VS1	O	VS1	O	VS1	O
44	IORD#	I	IORD#	I	IORD#	I
45	IOWR#	I	IOWR#	I	IOWR#	I
46	NC	–	NC	–	NC	–
47	NC	–	NC	–	NC	–
48	NC	–	NC	–	NC	–
49	NC	–	NC	–	NC	–
50	NC	–	NC	–	NC	–
51	Vcc	–	Vcc	–	Vcc	–
52	NC	–	NC	–	NC	–
53	NC	–	NC	–	NC	–
54	NC	–	NC	–	NC	–
55	NC	–	NC	–	NC	–
56	CSEL#	I	CSEL#	I	CSEL#	I
57	VS2	O	VS2	O	VS2	O
58	RESET	I	RESET	I	RESET#	I
59	Wait#	O	Wait#	O	IORDY	O
60	INPACK#	O	INPACK#	O	INPACK#	O
61	REG#	I	REG#	I	REG#	I
62	BVD2	I/O	SPKR#	I/O	DASP	I/O
63	BVD1	I/O	STSCHG#	I/O	PDIAG#	I/O
64	D8	I/O	D8	I/O	D8	I/O
65	D9	I/O	D9	I/O	D9	I/O
66	D10	O	D10	O	D10	O
67	CD2#	O	CD2#	O	CD2#	O
68	GND	–	GND	–	GND	–

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Rating	Units
V_{CC}	Power supply	-0.3 to 6.0	V
V_{IN}	Input voltage	-0.3 to V_{CC}+0.3	V
V_{OUT}	Output voltage	-0.3 to V_{CC}+0.3	V
T_{STG}	Storage temperature	-40 to 125	°C

DC CHARACTERISTICS:

I) Recommended Operating Conditions:

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Power supply	3.0	5.5	V
V_{IN}	Input voltage	0	V_{CC}	V
T_{OPR}	Operating temperature	-20	65	°C

II) General DC Characteristics:

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IL}	Input low current	no pull up/down	-1		1	µA
I_{IH}	Input high current	no pull up/down	-1		1	µA
I_{OZ}	Tri-state leakage current		-10		10	µA
C_{IN}	Input capacitance		4		pF	
C_{OUT}	Output capacitance		4		pF	
C_{BID}	Bi-direction capacitance		4		pF	

III) DC Electrical Characteristics:

Symbol	Parameter	Min	Typ	Max	Units
V_{IL}	Input low voltage			0.3V_{CC}	V
V_{IH}	Input high voltage	0.7V_{CC}			V
V_{IL}	Schmitt input low voltage		1.22		V
V_{IH}	Schmitt input high voltage		2.08		V
V_{OL}	Output low voltage			0.4	V
V_{OH}	Output high voltage	2.3		1	V
R_I	Input pull up/down resistance		75		kΩ

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AC CHARACTERISTICS:

Attribute Memory Read Timing Specification

Attribute Memory access time is defined as 300ns. Detailed timing specs are shown in Table below.

Speed Version			300 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**
Read Cycle Time	tc(R)	t_{AVAV}	300	
Address Access Time	ta(A)	t_{AVQV}		300
Card Enable Access Time	ta(CE)	t_{ELQV}		300
Output Enable Access Time	ta(OE)	t_{GLQV}		150
Output Disable Time from CE	tdis(CE)	t_{EHQZ}		100
Output Disable Time from OE	tdis(OE)	t_{GHQZ}		100
Address Setup Time	tsu(A)	t_{AVGL}	30	
Output Enable Time from CE	ten(CE)	t_{ELQNZ}	5	
Output Enable Time from OE	ten(OE)	t_{GLQNZ}	5	
Data Valid from Address Change	tv(A)	t_{AXQX}	0	

Note: All times are in nanoseconds. The CE# signal or both the OE# signal and the WE# signal must be de-asserted between consecutive cycle operations.

Configuration Register (Attribute Memory) Write Timing Specification

The Card Configuration write access time is defined as 250ns. Detailed timing specifications are shown in Table below.

Speed Version			250 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns**	**Max ns**
Write Cycle Time	tc(W)	t_{AVAV}	250	
Write Pulse Width	tw(WE)	t_{WLWH}	150	
Address Setup Time	tsu(A)	t_{AVWL}	30	
Write Recovery Time	trec(WE)	t_{WMAX}	30	
Data Setup Time for WE	tsu(D-WEH)	t_{DVWH}	80	
Data Hold Time	th(D)	t_{WMDX}	30	

Note: All times are in nanoseconds.

Common Memory Read Timing Specification

Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**
Output Enable Access Time	ta(OE)	t_{GLQV}		125
Output Disable Time from OE	tdis(OE)	t_{GHQZ}		100
Address Setup Time	tsu(A)	t_{AVGL}	30	
Address Hold Time	th(A)	t_{GHAX}	20	
CE Setup before OE	tsu(CE)	t_{ELGL}	0	
CE Hold following OE	th(CE)	t_{GHEH}	20	
Wait Delay Falling from OE	tv(WT-OE)	t_{GLWTV}		35
Data Setup for Wait Release	tv(WT)	t_{QVWTH}		0
Wait Width Time	tw(WT)	t_{WTLWTH}		350 (3000 for CF+)

Note: The maximum load on -WAIT# is 1 LSTTL with 50pF total load. All times are in nanoseconds. The WAIT# signal may be ignored if the OE# cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12ps but is intentionally less in this specification.

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AC CHARACTERISTICS (cont'd):

I/O Input (Read) Timing Specification

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Delay after IORD	td(IORD)	t_{IGLQV}		100
Data Hold following IORD	th(IORD)	t_{IGHQX}	0	
IORD Width Time	tw(IORD)	t_{IGLIGH}	165	
Address Setup before IORD	tsuA(IORD)	t_{AVIGL}	70	
Address Hold following IORD	thA(IORD)	t_{IGHAX}	20	
CE Setup before IORD	tsuCE(IORD)	t_{ELIGL}	5	
CE Hold following IORD	thCE(IORD)	t_{IGHEH}	20	
REG Setup before IORD	tsuREG(IORD)	t_{RGLIGL}	5	
REG Hold following IORD	thREG(IORD)	t_{IGHRGH}	0	
INPACK Delay Falling from IORD	tdfINPACK(IORD)	t_{IGLIAL}	0	45
INPACK Delay Rising from IORD	tdrINPACK(IORD)	t_{IGHIAH}		45
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	t_{AVISL}		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	t_{AVISH}		35
Wait Delay Falling from IORD	tdWT(IORD)	t_{IGLWTL}		35
Data Delay from Wait Rising	td(WT)	t_{WTHQV}		0
Wait Width Time	tw(WT)	t_{WTLWTH}		350 (3000 for CF+)

Note: Maximum load on WAIT#, INPACK# and I0IS16# is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from WAIT# high to IORD# high is Onsec, but minimum IORD# width must still be met. Wait Width time meets PCMCIA specification of 12ps but is intentionally less in this spec.

I/O Output (Write) Timing Specification

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	t_{DVIWH}	60	
Data Hold following IOWR	th(IOWR)	t_{IWHDX}	30	
IOWR Width Time	tw(IOWR)	t_{IWLIWH}	165	
Address Setup before IOWR	tsuA(IOWR)	t_{AVIWL}	70	
Address Hold following IOWR	thA(IOWR)	t_{IWHAX}	20	
CE Setup before IOWR	tsuCE(IOWR)	t_{ELIWL}	5	
CE Hold following IOWR	thCE(IOWR)	t_{IWHEH}	20	
REG Setup before IOWR	tsuREG(IOWR)	t_{RGLIWL}	5	
REG Hold following IOWR	thREG(IOWR)	t_{IWHRGH}	0	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	t_{AVISL}		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	t_{AVISH}		35
Wait Delay Falling from IOWR	tdWT(IOWR)	t_{IWLWTL}		35
IOWR high from Wait high	tdrIOWR(WT)	t_{WTJIWH}	0	
Wait Width Time	tw(WT)	t_{WTLWTH}		350 (3000for CF+)

Note: The maximum load on WAIT#, INPACK#, and I0IS16# is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from WAIT# high to IOWR# high is Onsec, but minimum IOWR# width must still be met. The Wait Width time meets the PCMCIA specification of 12ps but is intentionally less in this specification.

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AC CHARACTERISTICS (cont'd):

True IDE Mode I/O Input (Read) Timing Specification

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Delay after IORD	td(IORD)	t_{IGLQV}		100
Data Hold following IORD	th(IORD)	t_{IGHQX}	0	
IORD Width Time	tw(IORD)	t_{IGLIGH}	165	
Address Setup before IORD	tsuA(IORD)	t_{AVIGL}	70	
Address Hold following IORD	thA(IORD)	t_{IGHAX}	20	
CE Setup before IORD	tsuCE(IORD)	t_{ELIGL}	5	
CE Hold following IORD	thCE(IORD)	t_{IGHEH}	20	
I0IS16 Delay Falling from Address	tdfIOIS16(ADR)	t_{AVISL}		35
I0IS16 Delay Rising from Address	tdrIOIS16(ADR)	t_{AVISH}		35

Note: The maximum load on I0IS16# is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from WAIT# high to IORD# high is 0 nsec, but minimum IORD# width must still be met.

True IDE Mode I/O Output (Write) Timing Specification

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	t_{DVIWH}	60	
Data Hold following IOWR	th(IOWR)	t_{IWHDX}	30	
IOWR Width Time	tw(IOWR)	t_{IWLIWH}	165	
Address Setup before IOWR	tsuA(IOWR)	t_{AVIWL}	70	
Address Hold following IOWR	thA(IOWR)	t_{IWHAX}	20	
CE Setup before IOWR	tsuCE(IOWR)	t_{ELIWL}	5	
CE Hold following IOWR	thCE(IOWR)	t_{IWHEH}	20	
I0IS16 Delay Falling from Address	tdfIOIS16(ADR)	t_{AVISL}		35
I0IS16 Delay Rising from Address	tdrIOIS16(ADR)	t_{AVISH}		35

Note: The maximum load on I0IS16# is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from WAIT# high to IOWR# high is 0 nsec, but minimum IOWR# width must still be met.

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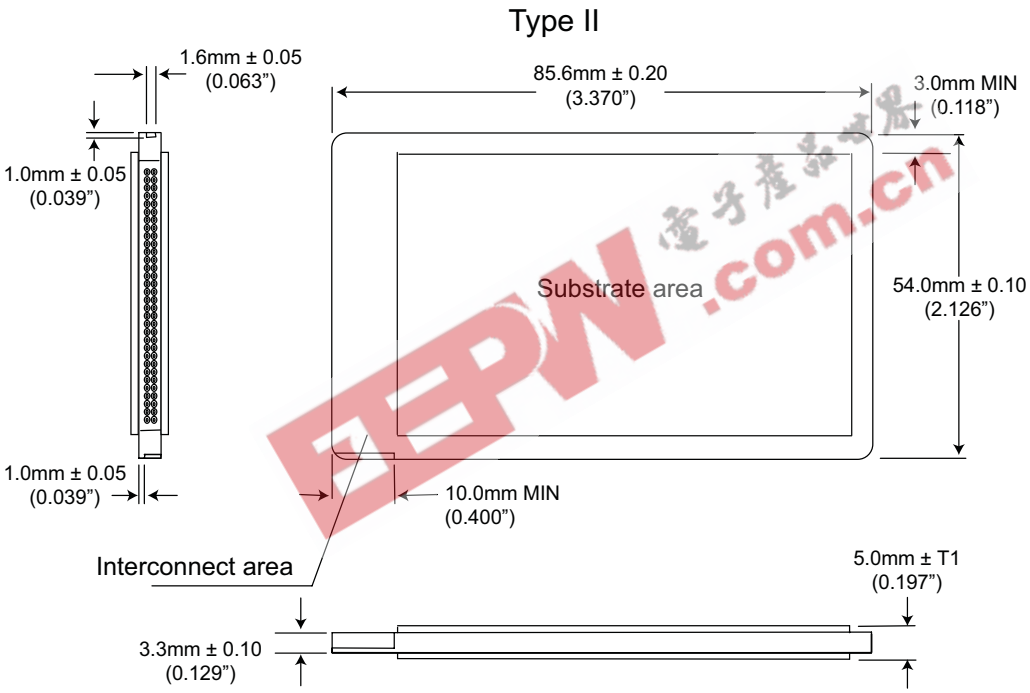
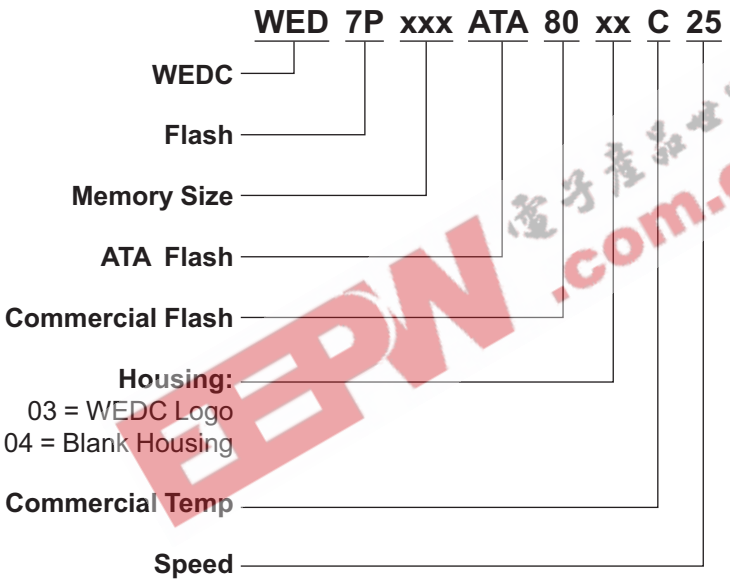
PACKAGE DIMENSIONS



PART NUMBERING GUIDE



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Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	March 2005	Final
Rev 1	1.1 Added "ED" to part marking	July 2005	Final

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