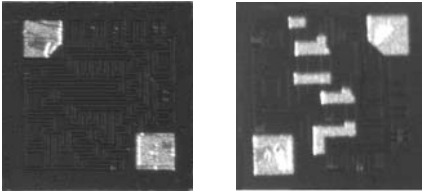


## Thin Film, Back-Contact Resistor



Product may not be to scale

The Back Contact Resistor (BCR) series single-value back-contact resistor chip is one of the smallest chips available. The BCR requires only one wire bond thus saving hybrid space.

The BCRs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The BCRs are 100 % electrically tested and visually inspected to MIL-STD-883.

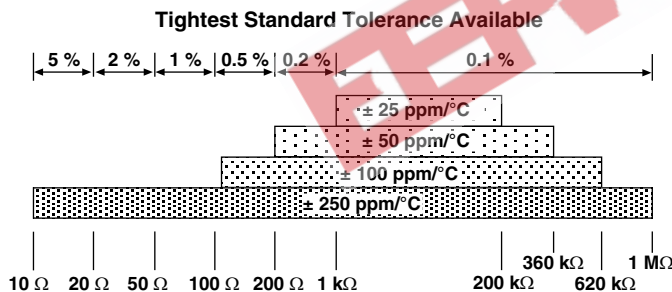
### APPLICATIONS

Vishay EFI BCR resistor chips are widely used in hybrid packages where space is limited. The bottom connection is made by attaching the back of the chip to the substrate either eutectically or with conductive epoxy. The single wire bond is made to the notched pad on the top of the chip. (The other rectangular pad on the top of the chip is a via hole, a low-ohmic contact connecting the resistor to the bottom of the chip.)

### FEATURES

- Wire bondable
- Only one wire bond required
- Small size: 0.020 inches square.
- Resistance range: 10 Ω to 1 MΩ
- Oxidized silicon substrate for good power dissipation
- Resistor material: Tantalum nitride, self-passivating
- Moisture resistant

### TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES



PROCESS CODE	
CLASS H*	CLASS K*
010	056
002	061
027	059
008	052

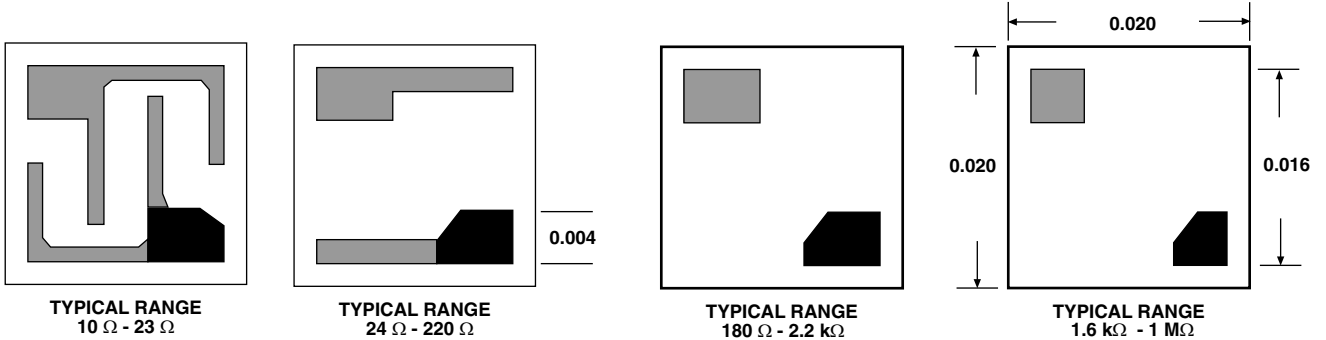
\*MIL-PRF-38534 inspection criteria

### STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308 100 Ω - 250 kΩ < 100 Ω or > 251 kΩ	- 35 dB typ. - 20 dB typ.
Moisture resistance, MIL-STD-202 Method 106	± 0.5 % max. ΔR/R
Stability, 1000 h, + 125 °C, 125 mW	± 1.0 % max. ΔR/R
Operating Temperature Range	- 55 °C to + 125 °C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.25 % max. ΔR/R
High Temperature Exposure, + 150 °C, 100 h	± 0.5 % max. ΔR/R
Dielectric Voltage Breakdown	200 V
Insulation Resistance	10 <sup>12</sup> min.
Operating Voltage	75 V max.
DC Power Rating at + 70 °C (Derated to Zero at + 175 °C)	250 mW
5 x Rated Power Short-Time Overload, + 25 °C, 5 s	± 0.25 % max. ΔR/R



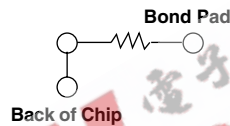
**DIMENSIONS** in inches



**Note:**

- Notched shaded area represents top bonding pad. The backside of the chip constitutes the second resistor connection.

**SCHEMATIC**



<b>MECHANICAL SPECIFICATIONS</b> in inches	
PARAMETER	
Chip Size	0.020 x 0.020 ± 0.002 (0.50 x 0.50 ± 0.05 mm)
Chip Thickness	0.010 ± 0.003 (0.253 ± 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO <sub>2</sub>
Resistor Material	Tantalum nitride, self-passivating
Bonding Pad Size	0.004 x 0.004 (0.100 x 0.100 mm)
Number of Pads	1
Pad Material	10 kÅ minimum aluminum
Backing	3 kÅ minimum gold
Recommended Attachment Method	Eutectic or conductive epoxy

**Options:** Gold bonding pads, 15 kÅ minimum thickness  
Consult Applications Engineer

<b>ORDERING INFORMATION</b>					
Example: 100 % visual, 16 kΩ, ± 1 %, ± 250 ppm/°C TCR, aluminum pads, class H visual inspection					
<b>W</b>	<b>BCR</b>	<b>008</b>	<b>1600</b>	<b>1</b>	<b>F</b>
INSPECTION/ PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100 % visually inspected parts in matrix tray per MIL-STD-883		See Process Code table	Use first 4 digits significant digits of the resistance	<b>B</b> = 0.01 <b>A</b> = 0.1 <b>0</b> = 1 <b>1</b> = 10 <b>2</b> = 100 <b>3</b> = 1000	<b>B</b> = 0.1 % <b>C</b> = 0.2 % <b>D</b> = 0.5 % <b>F</b> = 1.0 % <b>G</b> = 2.0 % <b>H</b> = 2.5 % <b>J</b> = 5.0 % <b>K</b> = 10 %
X = Sample, visually inspected parts loaded in matrix trays (4 % AQL)					



### Disclaimer

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