



## 2Mx16 Flash MODULE, SMD 5962-97610

### FEATURES

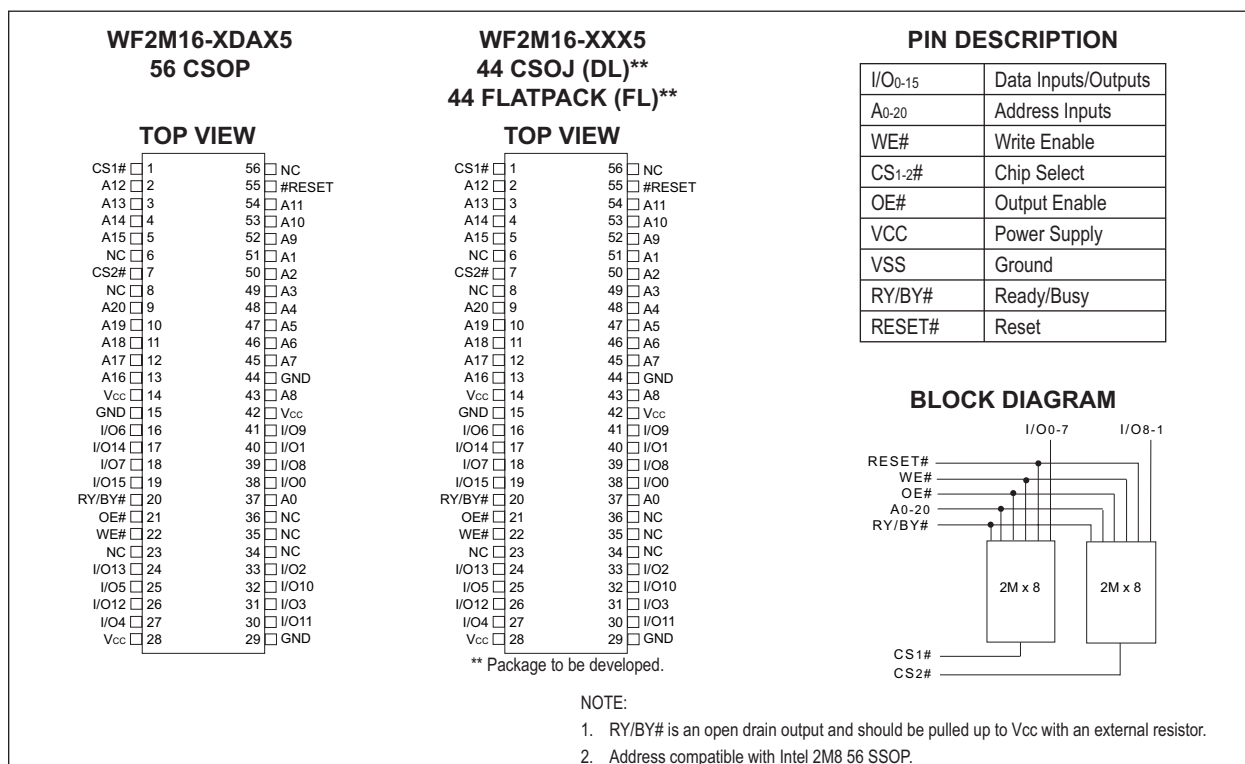
- Access Times of 90, 120, 150ns
- Packaging:
  - 56 lead, Hermetic Ceramic, 0.520" CSOP (Package 207). Fits standard 56 SSOP footprint.
  - 44 pin Ceramic SOJ (Package 102)\*\*
  - 44 lead Ceramic Flatpack (Package 208)\*\*
- Sector Architecture
  - 32 equal size sectors of 64KBytes each
  - Any combination of sectors can be erased. Also supports full chip erase.
- Minimum 100,000 Write/Erase Cycles Minimum
- Organized as 2Mx16; User Configurable as 2 x 2Mx8
- Commercial, Industrial, and Military Temperature Ranges
- 5 Volt Read and Write. 5V ± 10% Supply.
- Low Power CMOS
- Data# Polling and Toggle Bit feature for detection of program or erase cycle completion.
- Supports reading or programming data to a sector not being erased.
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation.
- RESET# pin resets internal state machine to the read mode.
- Ready/Busy (RY#/BY#) output for detection of program or erase cycle completion.
- Multiple Ground Pins for Low Noise Operation

\* This product is under development, is not qualified or characterized and is subject to change without notice.

\*\* Package to be developed.

Note: For programming information refer to Flash Programming 16M5 Application Notes.

FIGURE 1 – PIN CONFIGURATIONS





**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to V <sub>SS</sub>	V <sub>T</sub>	-2.0 to +7.0	V
Power Dissipation	P <sub>T</sub>	8	W
Storage Temperature	T <sub>STG</sub>	-65 to +125	°C
Short Circuit Output Current	I <sub>OS</sub>	100	mA
Data Retention (Mil Temp)		20	years
Endurance — write/erase cycles	(Mil Temp)	100,000 min.	cycles

**CAPACITANCE**

(T<sub>A</sub> = +25°C)

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C <sub>OE</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	25	pF
WE# capacitance	C <sub>WE</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	25	pF
CS# capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	15	pF
Data I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V, f = 1.0 MHz	15	pF
Address input capacitance	C <sub>AD</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	25	pF

This parameter is guaranteed by design but not tested.

**RECOMMENDED DC OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.0	–	V <sub>CC</sub> + 0.5	V
Input Low Voltage	V <sub>IL</sub>	-0.5	–	+0.8	V
Operating Temperature (Mil.)	T <sub>A</sub>	-55	–	+125°C	°C
Operating Temperature (Ind.)	T <sub>A</sub>	-40	–	+85	°C

**DC CHARACTERISTICS - CMOS COMPATIBLE**

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10	µA
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10	µA
V <sub>CC</sub> Active Current for Read (1)	I <sub>CC1</sub>	CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub> , f = 5MHz		80	mA
V <sub>CC</sub> Active Current for Program or Erase (2)	I <sub>CC2</sub>	CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub>		120	mA
V <sub>CC</sub> Standby Current	I <sub>CC3</sub>	V <sub>CC</sub> = 5.5, CS# = V <sub>IH</sub> , f = 5MHz, RESET# = V <sub>CC</sub> ± 0.3V		4.0	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 12.0 mA, V <sub>CC</sub> = 4.5		0.45	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -2.5 mA, V <sub>CC</sub> = 4.5	0.85xV <sub>CC</sub>		V
Low V <sub>CC</sub> Lock-Out Voltage	V <sub>LKO</sub>		3.2	4.2	V

**NOTES:**

- The I<sub>CC</sub> current listed includes both the DC operating current and the frequency dependent component (@ 5MHz). The frequency component typically is less than 2mA/MHz, with OE# at V<sub>IH</sub>.
- I<sub>CC</sub> active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions V<sub>IL</sub> = 0.3V, V<sub>IH</sub> = V<sub>CC</sub> - 0.3V



**AC Characteristics – Write/Erase/Program Operations - WE# Controlled**

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>AVAV</sub>	t <sub>WC</sub>	90		120		150		ns
Chip Select Setup Time	t <sub>ELWL</sub>	t <sub>CS</sub>	0		0		0		ns
Write Enable Pulse Width	t <sub>WLWH</sub>	t <sub>WP</sub>	45		50		50		ns
Address Setup Time	t <sub>AVWL</sub>	t <sub>AS</sub>	0		0		0		ns
Data Setup Time	t <sub>DVWH</sub>	t <sub>DS</sub>	45		50		50		ns
Data Hold Time	t <sub>WHDX</sub>	t <sub>DH</sub>	0		0		0		ns
Address Hold Time	t <sub>WLAX</sub>	t <sub>AH</sub>	45		50		50		ns
Write Enable Pulse Width High	t <sub>WHWL</sub>	t <sub>WPH</sub>	20		20		20		ns
Duration of Byte Programming Operation (1)	t <sub>WHWH1</sub>			300		300		300	μs
Sector Erase (2)	t <sub>WHWH2</sub>			15		15		15	sec
Read Recovery Time before Write	t <sub>GHWL</sub>		0		0		0		μs
V <sub>CC</sub> Setup Time	t <sub>VCS</sub>		50		50		50		μs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)	t <sub>OEHL</sub>		10		10		10		ns
RESET# Pulse Width	t <sub>TRP</sub>		500		500		500		ns

**NOTES:**

1. Typical value for t<sub>WHWH1</sub> is 7μs.
2. Typical value for t<sub>WHWH2</sub> is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

**AC CHARACTERISTICS – READ-ONLY OPERATIONS**

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	T <sub>AVAV</sub>	T <sub>RC</sub>	90		120		150		ns
Address Access Time	T <sub>AVQV</sub>	T <sub>ACC</sub>		90		120		150	ns
Chip Select Access Time	T <sub>ELQV</sub>	T <sub>CE</sub>		90		120		150	ns
Output Enable to Output Valid	T <sub>GLQV</sub>	T <sub>OE</sub>		40		50		55	ns
Chip Select High to Output High Z (1)	T <sub>EHQZ</sub>	T <sub>DF</sub>		20		30		35	ns
Output Enable High to Output High Z (1)	T <sub>GHQZ</sub>	T <sub>DF</sub>		20		30		35	ns
Output Hold from Addresses, CS# or OE# Change, whichever is First	T <sub>AXQX</sub>	T <sub>OH</sub>	0		0		0		ns
RESET# Low to Read Mode (1)		T <sub>READY</sub>		20		20		20	μs

1. Guaranteed by design, not tested.



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, CS# CONTROLLED

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>AVAV</sub>	t <sub>WC</sub>	90		120		150		ns
Write Enable Setup Time	t <sub>WLEL</sub>	t <sub>WS</sub>	0		0		0		ns
Chip Select Pulse Width	t <sub>LELH</sub>	t <sub>CP</sub>	45		50		50		ns
Address Setup Time	t <sub>AVEL</sub>	t <sub>AS</sub>	0		0		0		ns
Data Setup Time	t <sub>DVEH</sub>	t <sub>DS</sub>	45		50		50		ns
Data Hold Time	t <sub>EHDX</sub>	t <sub>DH</sub>	0		0		0		ns
Address Hold Time	t <sub>ELAX</sub>	t <sub>AH</sub>	45		50		50		ns
Chip Select Pulse Width High	t <sub>EHEL</sub>	t <sub>CPH</sub>	20		20		20		ns
Duration of Byte Programming Operation (1)	t <sub>WHWH1</sub>			300	300		300		μs
Sector Erase Time (2)	t <sub>WHWH2</sub>			15	15		15		sec
Read Recovery Time	t <sub>GHSL</sub>		0		0		0		μs
Chip Programming Time				44	44		44		sec
Chip Erase Time (3)				256	256		256		sec
Output Enable Hold Time (4)		t <sub>OEHL</sub>	10		10		10		ns

NOTES:

1. Typical value for t<sub>WHWH1</sub> is 7μs.
2. Typical value for t<sub>WHWH2</sub> is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

FIGURE 2 – AC TEST CIRCUIT

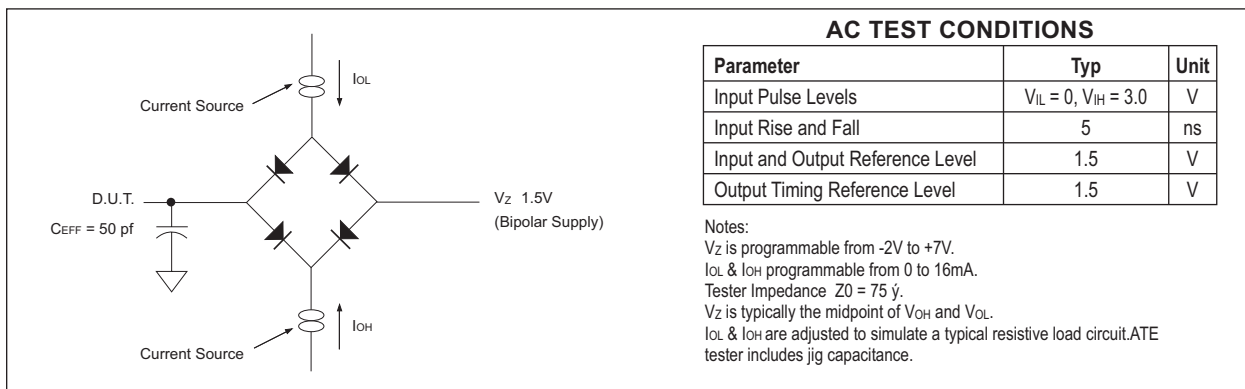


FIGURE 3 – RESET TIMING DIAGRAM

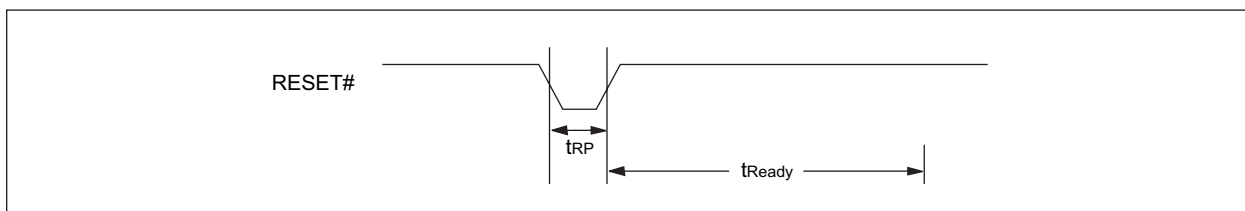




FIGURE 3 – AC WAVEFORMS FOR READ OPERATIONS

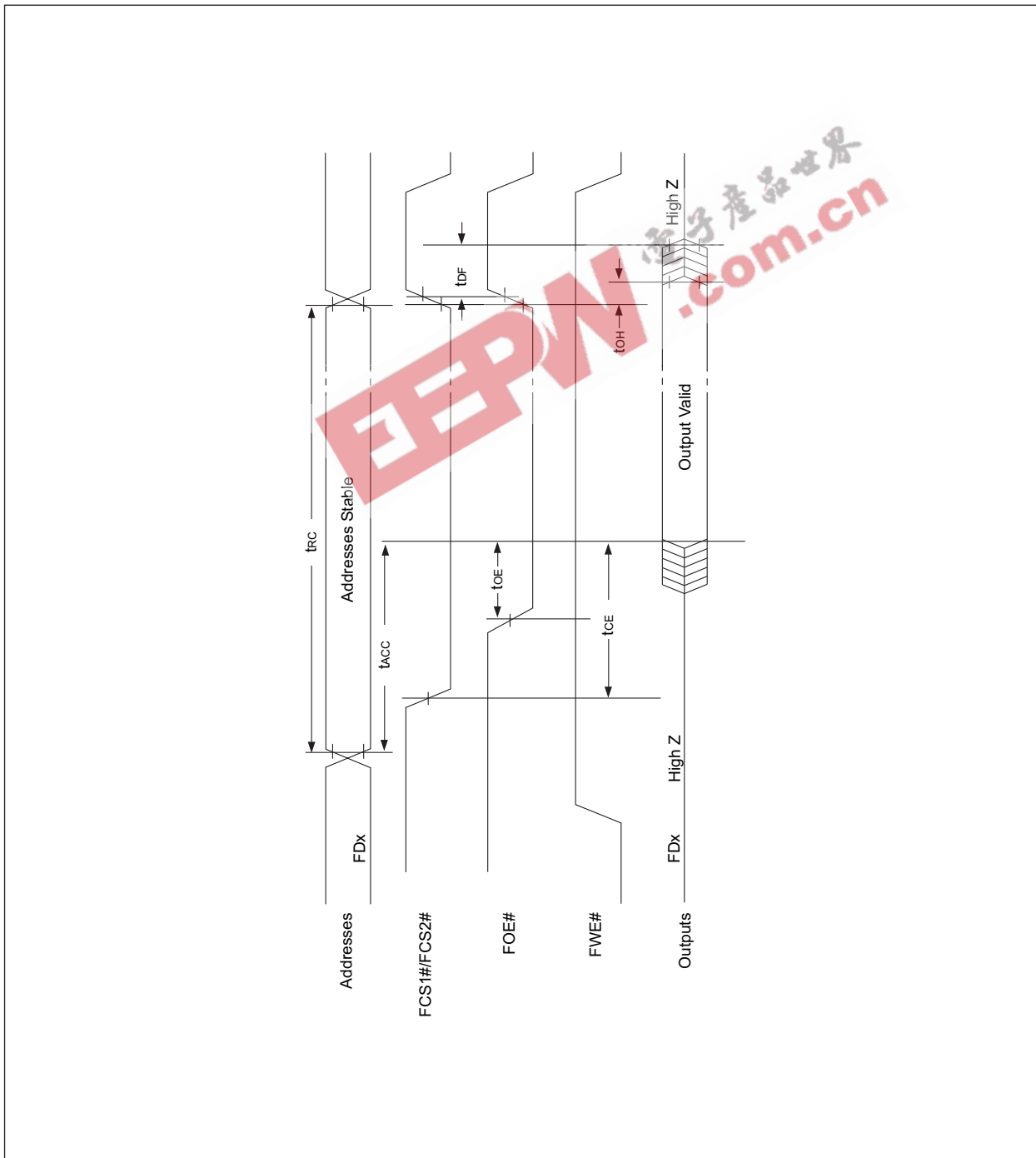
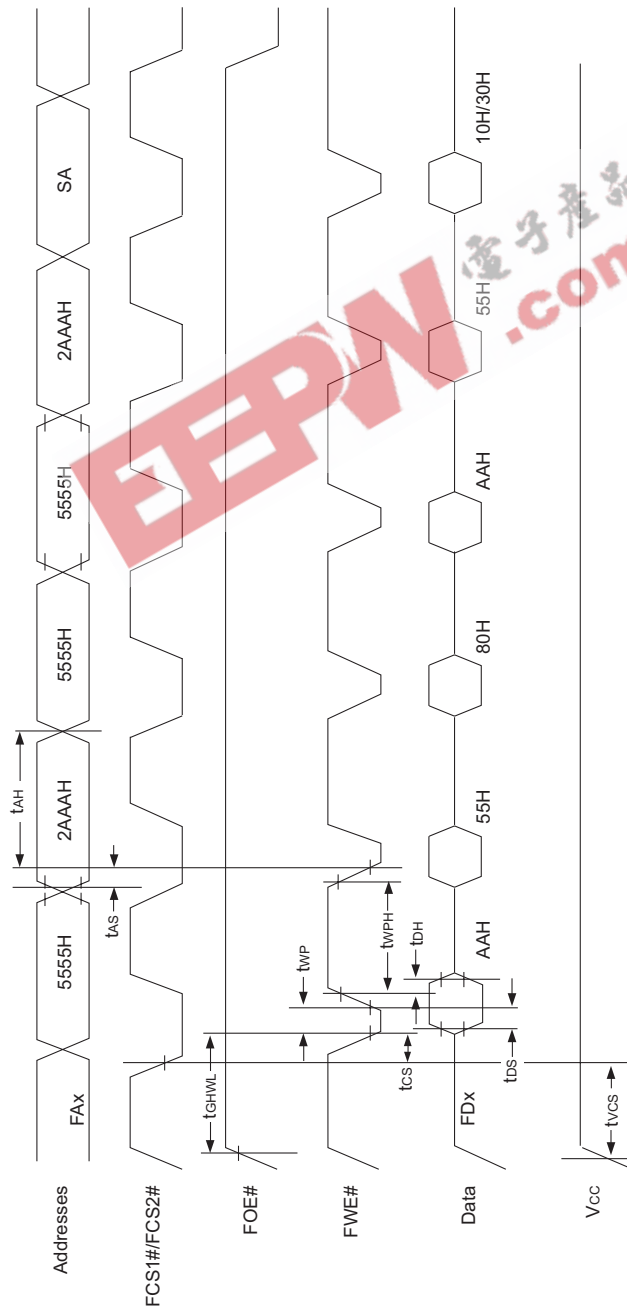






FIGURE 5 – AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



NOTE:

- 1. SA is the sector address for Sector Erase.



FIG. 6 – AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS

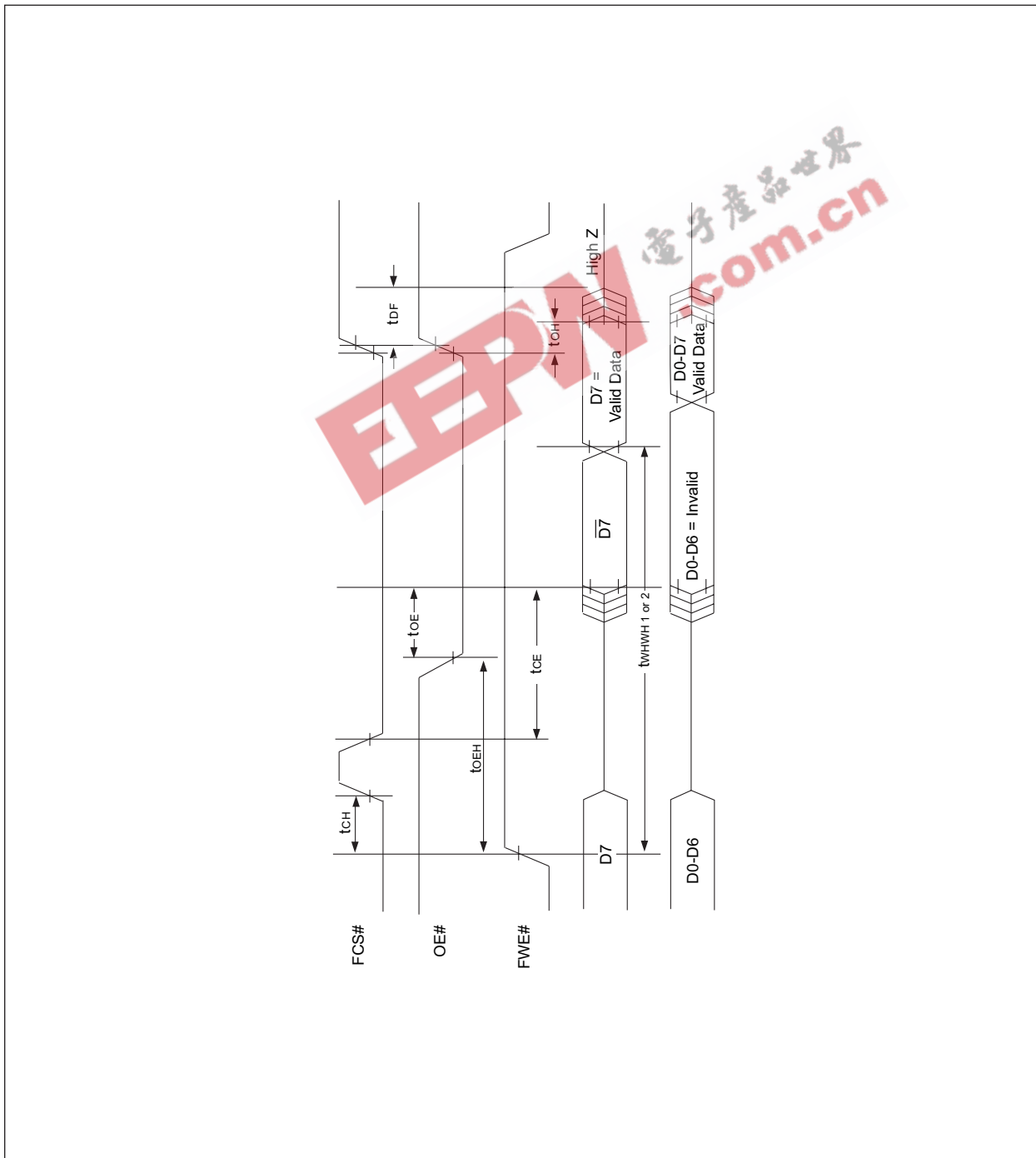
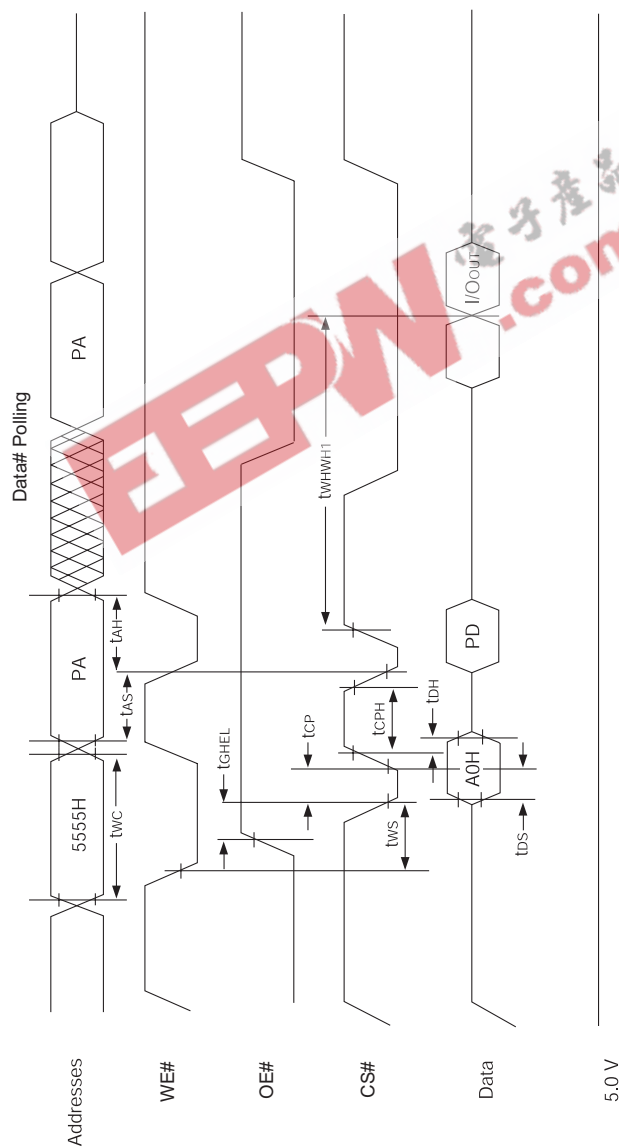






FIGURE 7 – ALTERNATE CS# CONTROLLED PROGRAMMING OPERATION TIMINGS

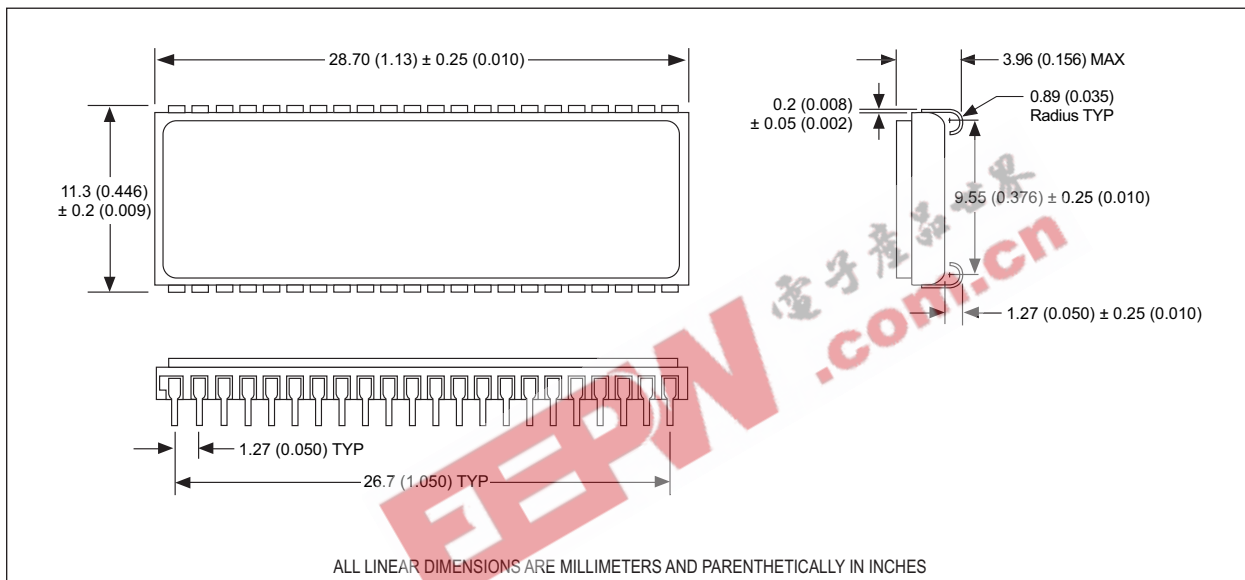


NOTES:

- 1. PA represents the address of the memory location to be programmed.
- 2. PD represents the data to be programmed at byte address.
- 3. D7# is the output of the complement of the data written to the device.
- 4. DOUT is the output of the data written to the device.
- 5. Figure indicates the last two bus cycle sequence.

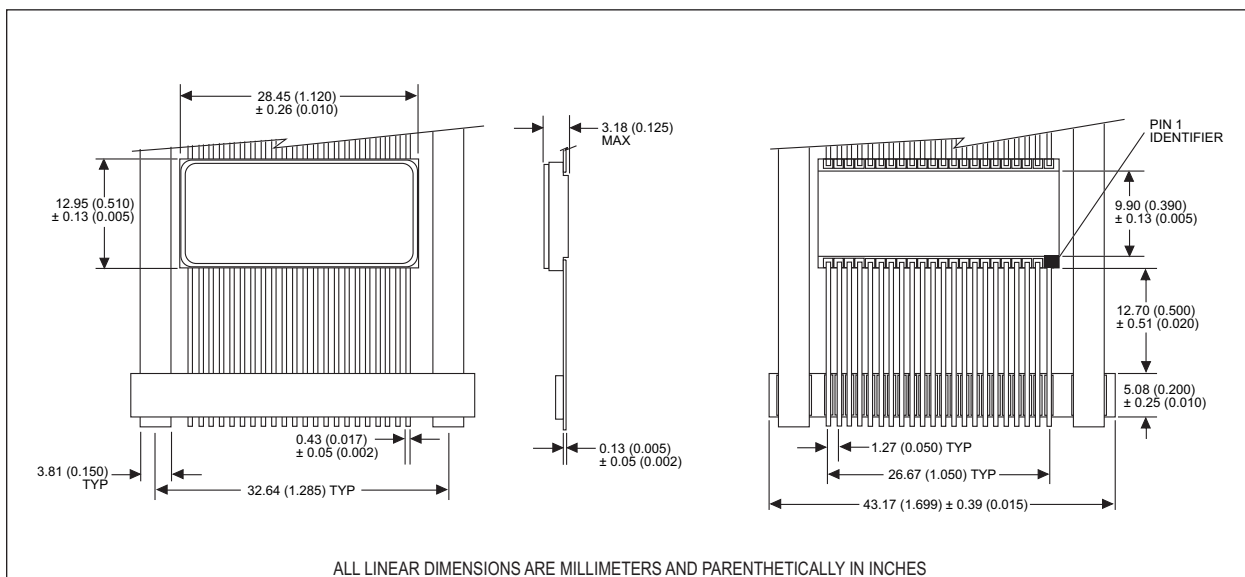


**PACKAGE 102: 44 LEAD, CERAMIC SOJ\*\***



\*\* Package to be developed.

**PACKAGE 208: 44 LEAD, CERAMIC FLAT PACK\*\***

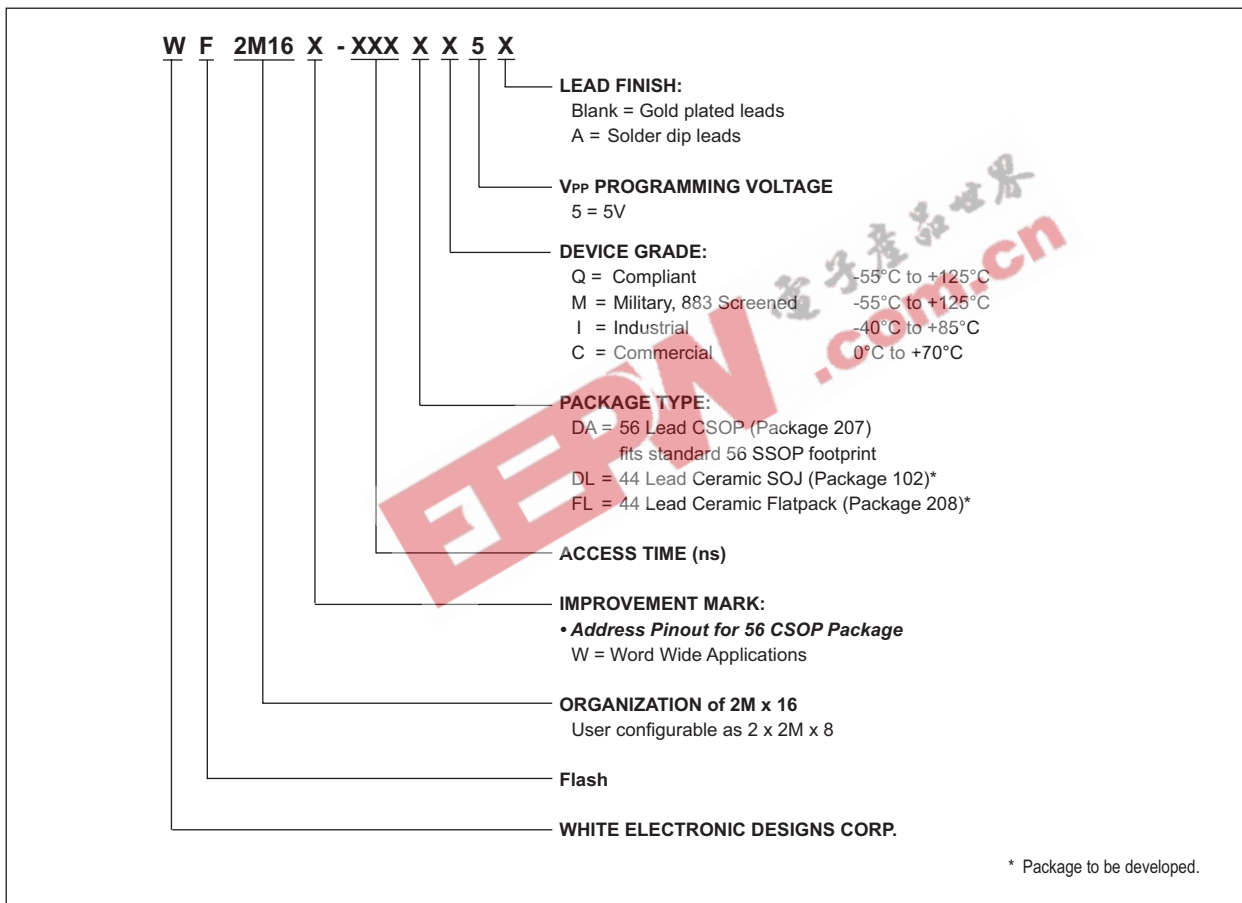


\*\* Package to be developed.





**ORDERING INFORMATION**



DEVICE TYPE	SECTOR SIZE	SPEED	PACKAGE	SMD NO.
2M x 16 Flash MCP		150ns		5962-97610 04HXX
2M x 16 Flash MCP		120ns		5962-97610 05HXX
2M x 16 Flash MCP		90ns		5962-97610 06HXX