



8Mx32 5V FLASH MODULE

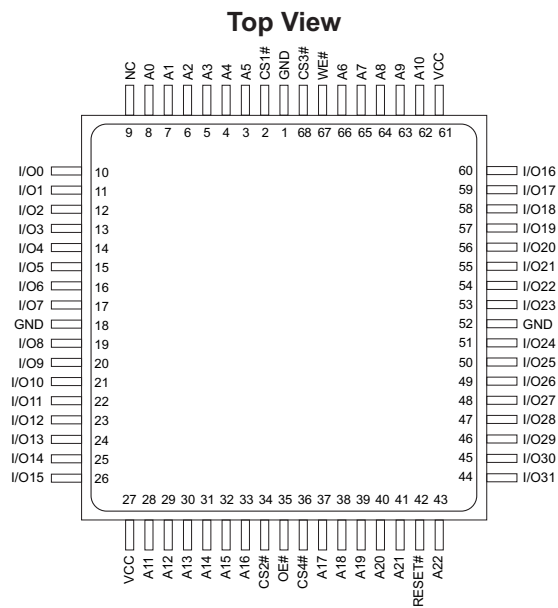
FEATURES

- Access Time of 100, 120, 150ns
- Packaging:
 - 68 Lead, 40 mm (1.560") square hermetic CQFP, 5.2 mm (0.205") high (Package 503)
- Sector Architecture
 - 32 equal size sectors of 64KBytes per each 2Mx8 chip
 - Any combination of sectors can be erased. Also supports full chip erase.
- 100,000 Write/Erase Cycles Minimum
- Organized as 8Mx32
- Commercial, Industrial, and Military Temperature Ranges
- 5 Volt Read and Write. 5V ± 10% Supply.
- Low Power CMOS
- Data# Polling and Toggle Bit feature for detection of program or erase cycle completion.
- Supports reading or programming data to a sector not being erased.
- RESET# pin resets internal state machine to the read mode. (Not available in HIP package for WF2M32-XHX5)
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation, Separate Power and Ground Planes to improve noise immunity.
- Built in Buffering.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

Note: For programming information refer to Flash Programming 16M5 Application Note.

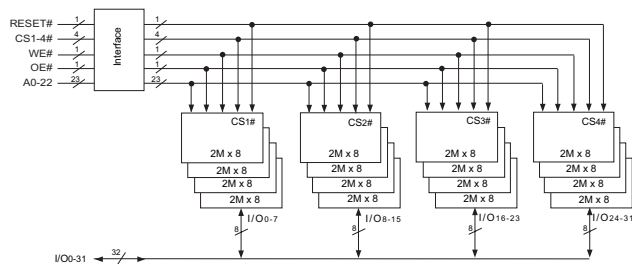
FIGURE 1 – PIN CONFIGURATION FOR WF8M32-XG4DX5



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-22	Address Inputs
WE	Write Enable
CS1-4	Chip Selects
OE	Output Enable
VCC	Power Supply
RESET	Reset
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



CS1# selects I/O0-7, CS2# selects I/O8-15, CS3# selects I/O16-23, CS4# selects I/O24-31



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to Vss	V _T	-2.0 to +7.0	V
Power Dissipation	P _T	8	W
Storage Temperature	T _{STG}	-65 to +125	°C
Short Circuit Output Current	I _{OS}	100	mA
Endurance - Write/Erase Cycles (Mil Temp)		100,000 min	cycles
Data Retention (Mil Temp)		20	years

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
WE# capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
CS1-4# capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	60	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
RESET# capacitance	C _{RST}	V _{IN} = 0 V, f = 1.0 MHz	20	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	—	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.5	—	+0.8	V
Operating Temperature (Mil.)	T _A	-55	—	+125	°C
Operating Temperature (Ind.)	T _A	-40	—	+85	°C

DC CHARACTERISTICS – CMOS COMPATIBLE

V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LOx32}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
V _{CC} Active Current for Read (1)	I _{CC1}	CS# = V _{IL} , OE# = V _{IH} , f = 5MHz		640	mA
V _{CC} Active Current for Program or Erase (2)	I _{CC2}	CS# = V _{IL} , OE# = V _{IH}		960	mA
V _{CC} Standby Current	I _{CC3}	V _{CC} = 5.5, CS# = V _{IH} , f = 5MHz, RESET# = V _{CC} ± 0.3V		160	mA
Output Low Voltage	V _{OL}	I _{OL} = 12.0 mA, V _{CC} = 4.5		0.45	V
Output High Voltage	V _{OH}	I _{OH} = -2.5 mA, V _{CC} = 4.5	0.85 x V _{CC}		V
Low V _{CC} Lock-Out Voltage	V _{LKO}		3.2	4.2	V

Notes:

- The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 5MHz).
The frequency component typically is less than 2mA/MHz, with OE# at V_{IH}.
- I_{CC} active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS – WE# CONTROLLED

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	100		120		150		ns
Chip Select Setup Time	t _{ELWL}	t _{CS}	0		0		0		ns
Write Enable Pulse Width	t _{WLWH}	t _{WP}	50		50		50		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		ns
Data Setup Time	t _{DVWH}	t _{DS}	50		50		50		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		ns
Address Hold Time	t _{WLAX}	t _{AH}	50		50		50		ns
Write Enable Pulse Width High	t _{WHWL}	t _{WPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t _{WHWH1}			300		300		300	μs
Sector Erase (2)	t _{WHWH2}			15		15		15	sec
Read Recovery Time before Write	t _{GHWL}		0		0		0		μs
V _{CC} Setup Time	t _{VCS}		50		50		50		μs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	ns
Output Enable Hold Time (4)		t _{OEHL}	10		10		10		ns
RESET# Pulse Width		t _{RP}	500		500		500		ns

NOTES:

1. Typical value for t_{WHWH1} is 7μs.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

AC CHARACTERISTICS – READ-ONLY OPERATIONS

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	100		120		150		ns
Address Access Time	t _{AVQV}	t _{ACC}		100		120		150	ns
Chip Select Access Time	t _{ELQV}	t _{CE}		100		120		150	ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		50		50		55	ns
Chip Select High to Output High Z (1)	t _{EHQZ}	t _{DF}		30		30		35	ns
Output Enable High to Output High Z (1)	t _{GHQZ}	t _{DF}		30		30		35	ns
Output Hold from Addresses, CS# or OE# Change, whichever is First	t _{AXQX}	t _{OH}	0		0		0		ns
RST Low to Read Mode (1)		t _{Ready}		20		20		20	μs

1. Guaranteed by design, not tested.



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS – CS# CONTROLLED

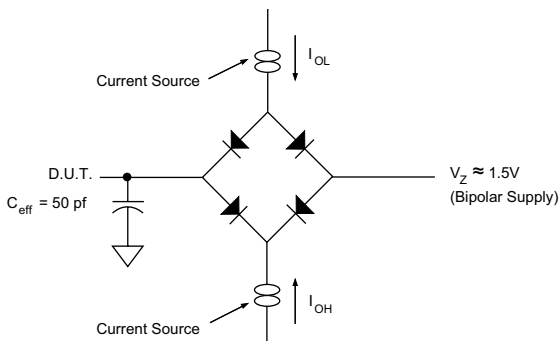
$V_{CC} = 3.3V, V_{SS} = 0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	100		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Select Pulse Width	t_{LELH}	t_{CP}	50		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	50		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	50		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	μs
Sector Erase Time (2)	t_{WHWH2}			15		15		15	sec
Read Recovery Time (2)	t_{GHEL}		0		0		0		μs
Chip Programming Time				100		100		100	sec
Chip Erase Time (3)				480		480		480	sec
Output Enable Hold Time (4)		t_{OEHL}	10		10		10		ns

NOTES:

1. Typical value for t_{WHWH1} is 7 μs .
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

FIGURE 2 – AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

- V_Z is programmable from -2V to +7V.
- I_{OL} & I_{OH} programmable from 0 to 16mA.
- Tester Impedance $Z_0 = 75 \Omega$.
- V_Z is typically the midpoint of V_{OH} and V_{OL} .
- I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
- ATE tester includes jig capacitance.

FIGURE 3 – RESET TIMING DIAGRAM

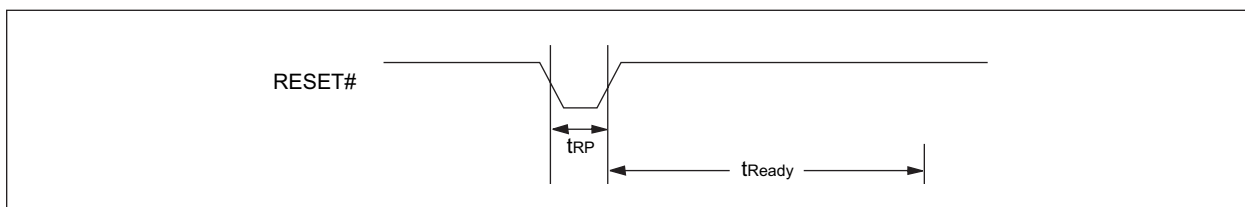
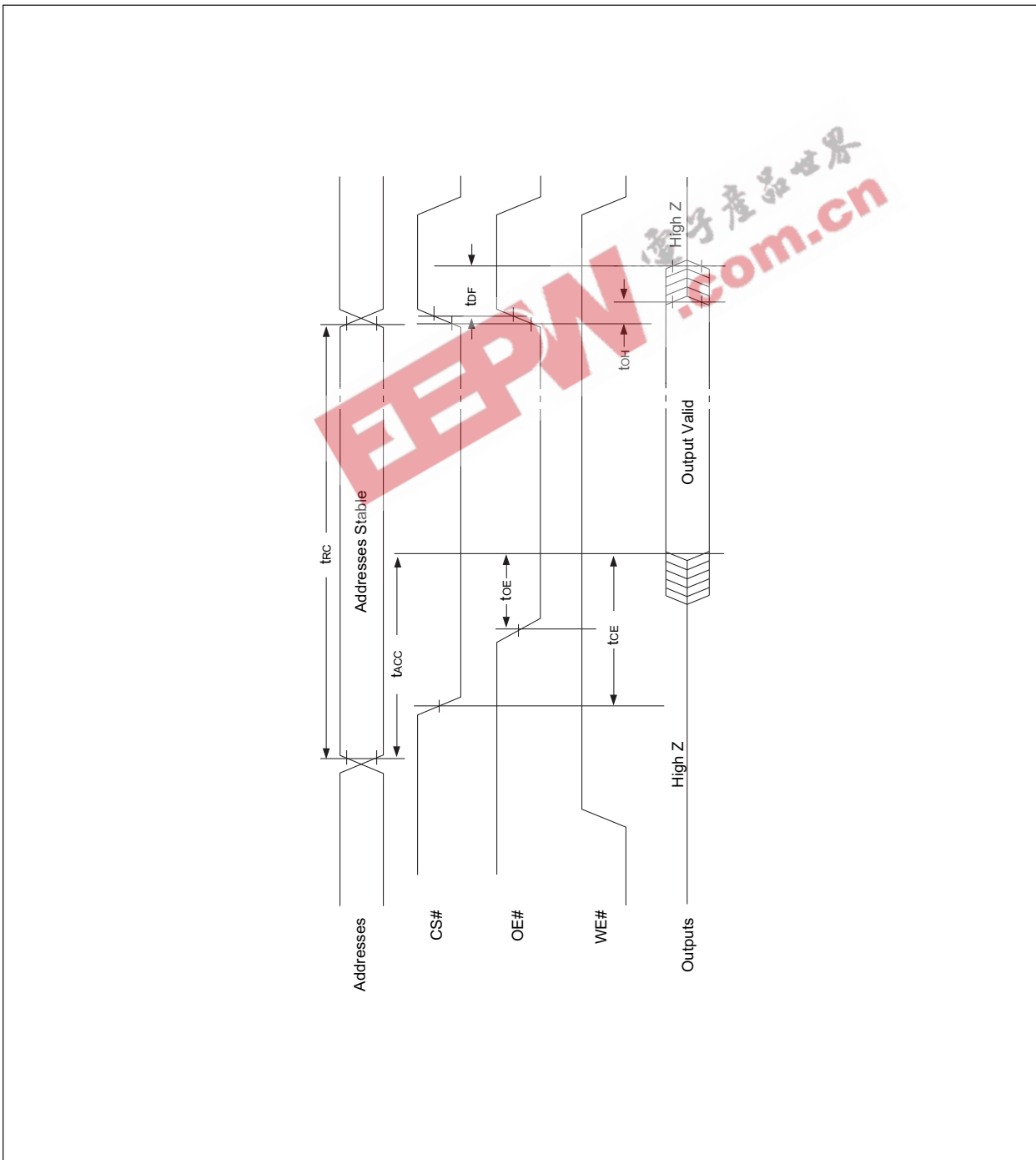


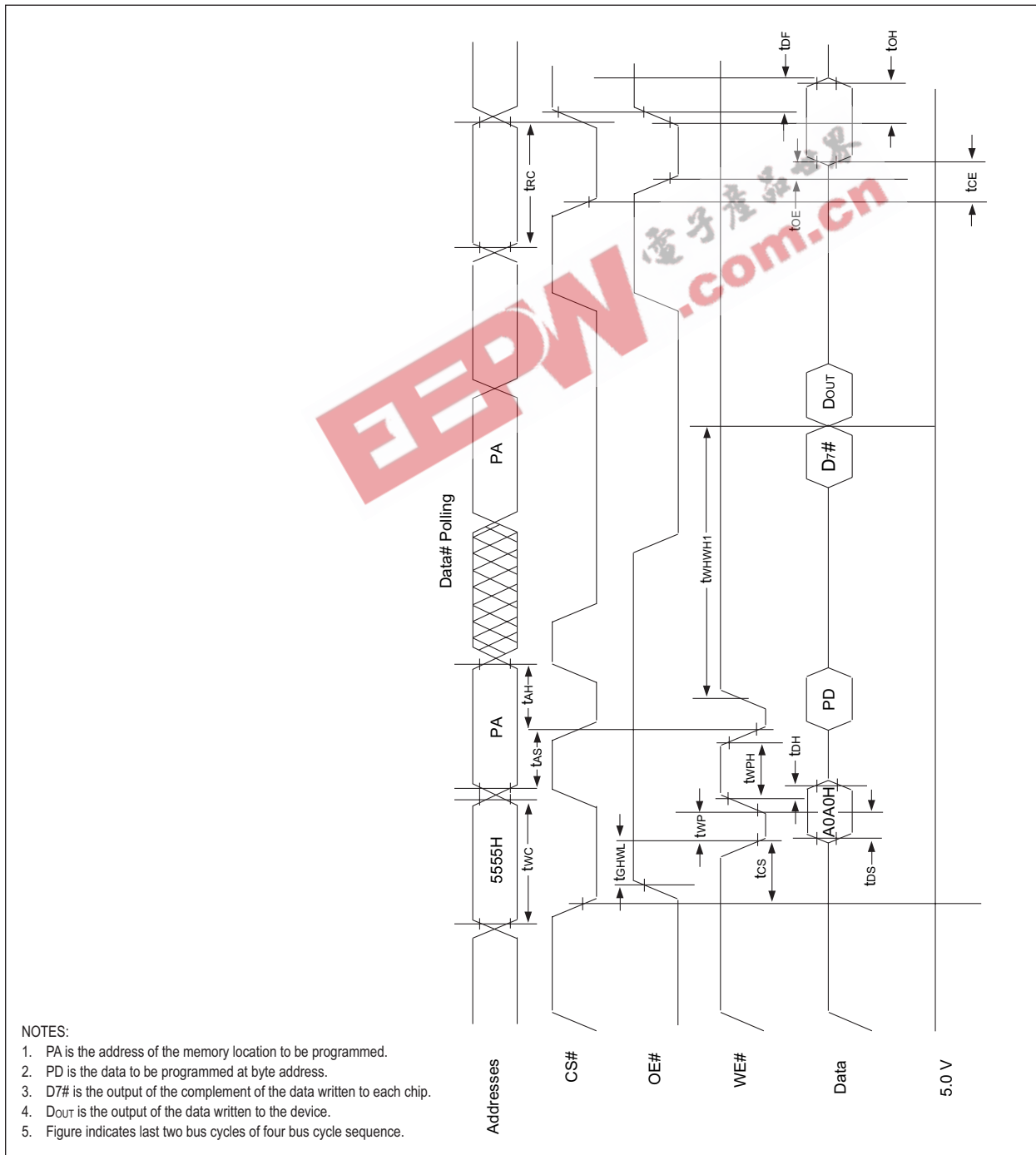


FIGURE 4 – AC WAVEFORMS FOR READ OPERATIONS





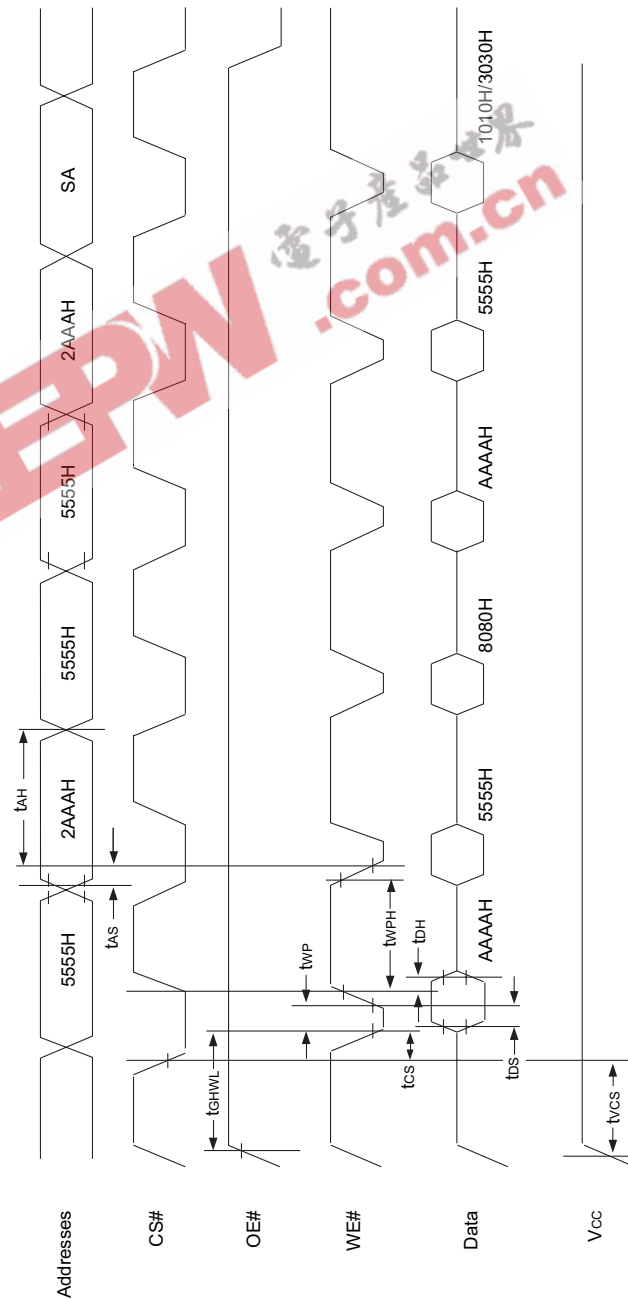
WRITE/ERASE/PROGRAM OPERATION, WE# CONTROLLED



- NOTES:
1. PA is the address of the memory location to be programmed.
 2. PD is the data to be programmed at byte address.
 3. D7# is the output of the complement of the data written to each chip.
 4. D_{OUT} is the output of the data written to the device.
 5. Figure indicates last two bus cycles of four bus cycle sequence.



AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS

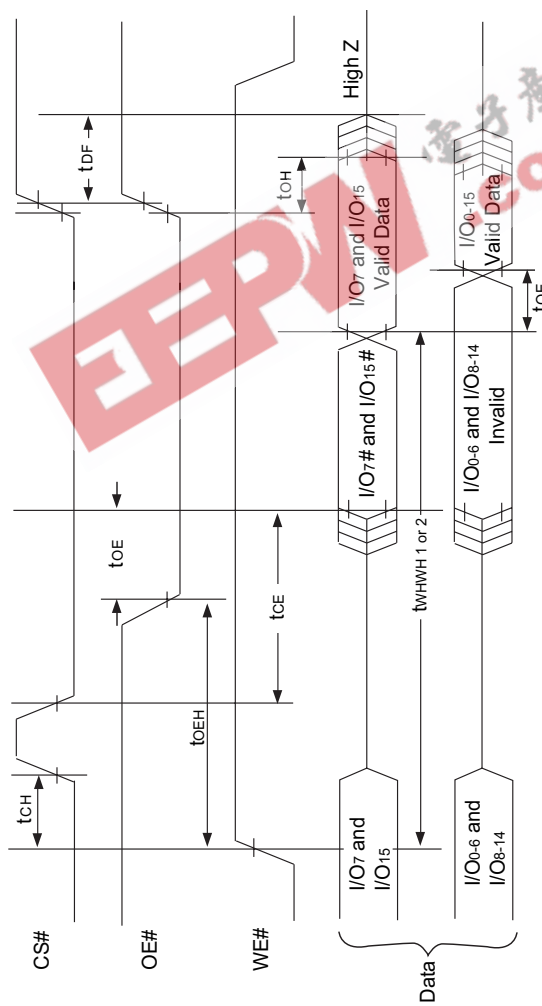


NOTE:

- 1. SA is the sector address for Sector Erase.

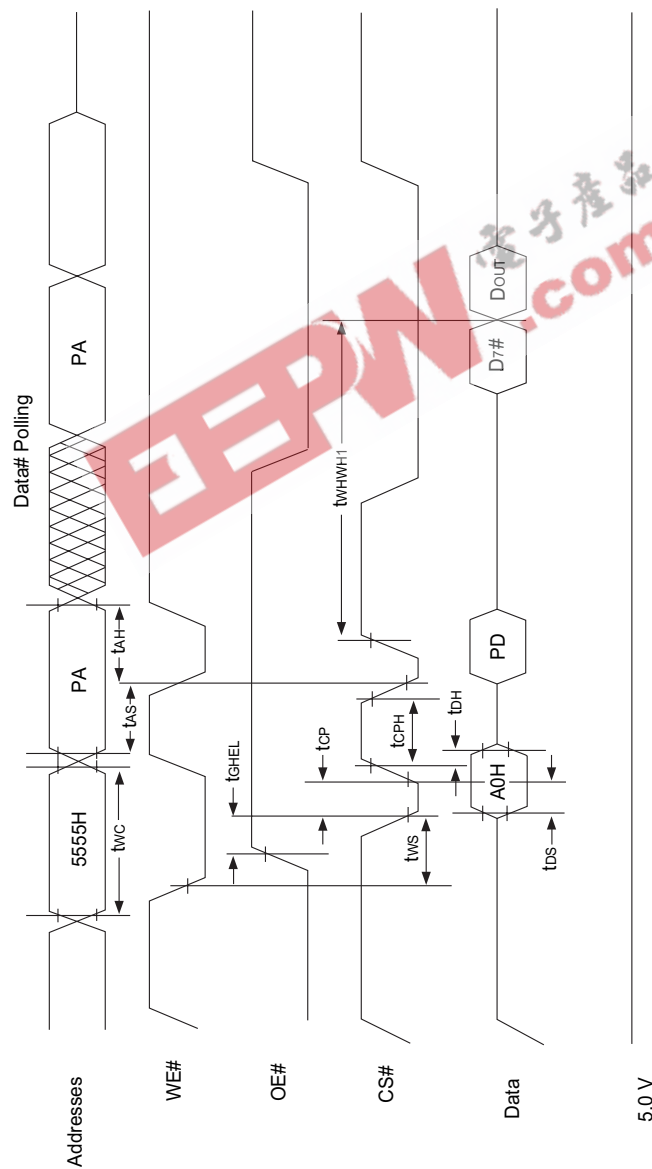


AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS





ALTERNATE CS# CONTROLLED PROGRAMMING OPERATION TIMINGS

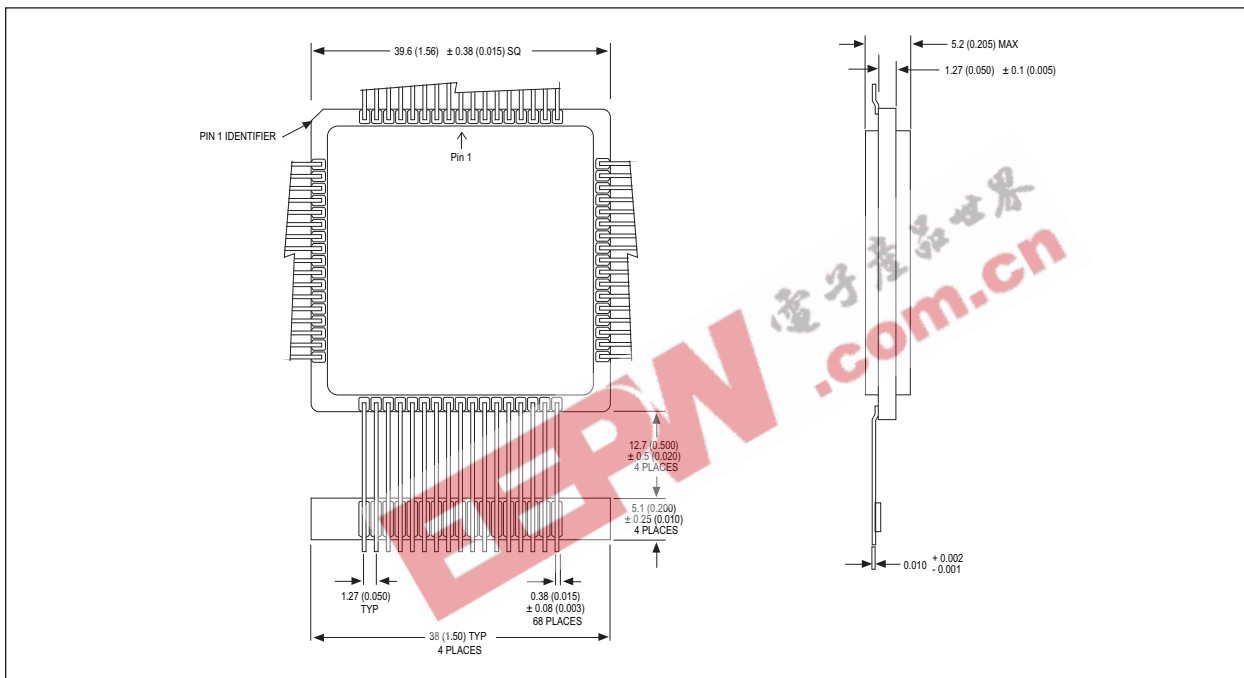


NOTES:

1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to each chip.
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.



PACKAGE 503: 68 LEAD, CERAMIC QUAD FLAT PACK DUAL CAVITY, CQFP (G4D)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W F 8M32 - XXX G4D X 5

