# 512MB – 64Mx72 SDRAM, UNBUFFERED, w/PLL

## FEATURES

- PC100 and PC133
- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- Single Rank
- 3.3V ± 0.3V Power Supply
- 144 Pin SO-DIMM JEDEC
  - D1: 31.75 (1.25") TYP

## DESCRIPTION

The WED3DG7266V is a 64Mx72 synchronous DRAM module which consists of nine 64Mx8 SDRAM components in TSOP II package, and one 2Kb EEPROM in an 8 pin TSOP package for Serial Presence Detect which are mounted on a 144 pin SO-DIMM multilayer FR4 Substrate.

NOTE: Consult factory for availability of:
- RoHS compliant products
- Vendor source control options
- Industrial temperature option



## PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

| PINOUT | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PIN | FRONT | PIN | BACK | PIN | FRONT | PIN | BACK | PIN | FRONT | PIN | BACK |
| 1 | Vss | 2 | Vss | 49 | DQ13 | 50 | DQ45 | 97 | DQ22 | 98 | DQ54 |
| 3 | DQ0 | 4 | DQ32 | 51 | DQ14 | 52 | DQ46 | 99 | DQ23 | 100 | DQ55 |
| 5 | DQ1 | 6 | DQ33 | 53 | DQ15 | 54 | DQ47 | 101 | Vcc | 102 | Vcc |
| 7 | DQ2 | 8 | DQ34 | 55 | Vss | 56 | Vss | 103 | A6 | 104 | A7 |
| 9 | DQ3 | 10 | DQ35 | 57 | CB0 | 58 | CB4 | 105 | A8 | 106 | BA0 |
| 11 | Vcc | 12 | Vcc | 59 | CB1 | 60 | CB5 | 107 | Vss | 108 | Vss |
| 13 | DQ4 | 14 | DQ36 | 61 | CLK0 | 62 | CKE0 | 109 | A9 | 110 | BA1 |
| 15 | DQ5 | 16 | DQ37 | 63 | Vcc | 64 | Vcc | 111 | A10 | 112 | A11 |
| 17 | DQ6 | 18 | DQ38 | 65 | RAS# | 66 | CAS# | 113 | Vcc | 114 | Vcc |
| 19 | DQ7 | 20 | DQ39 | 67 | WE# | 68 | CKE1* | 115 | DQMB2 | 116 | DQMB6 |
| 21 | Vss | 22 | Vss | 69 | SO# | 70 | A12* | 117 | DQMB3 | 118 | DQMB7 |
| 23 | DQMB0 | 24 | DQMB4 | 71 | S1#* | 72 | NC | 119 | Vss | 120 | Vss |
| 25 | DQMB1 | 26 | DQMB5 | 73 | NC | 74 | CLK1 | 121 | DQ24 | 122 | DQ56 |
| 27 | Vcc | 28 | Vcc | 75 | Vss | 76 | Vss | 123 | DQ25 | 124 | DQ57 |
| 29 | A0 | 30 | A3 | 77 | CB2 | 78 | CB6 | 125 | DQ26 | 126 | DQ58 |
| 31 | A1 | 32 | A4 | 79 | CB3 | 80 | CB7 | 127 | DQ27 | 128 | DQ59 |
| 33 | A2 | 34 | A5 | 81 | Vcc | 82 | Vcc | 129 | Vcc | 130 | Vcc |
| 35 | Vss | 36 | Vss | 83 | DQ16 | 84 | DQ48 | 131 | DQ28 | 132 | DQ60 |
| 37 | DQ8 | 38 | DQ40 | 85 | DQ17 | 86 | DQ49 | 133 | DQ29 | 134 | DQ61 |
| 39 | DQ9 | 40 | DQ41 | 87 | DQ18 | 88 | DQ50 | 135 | DQ30 | 136 | DQ62 |
| 41 | DQ10 | 42 | DQ42 | 89 | DQ19 | 90 | DQ51 | 137 | DQ31 | 138 | DQ63 |
| 43 | DQ11 | 44 | DQ43 | 91 | Vss | 92 | Vss | 139 | Vss | 140 | Vss |
| 45 | Vcc | 46 | Vcc | 93 | DQ20 | 94 | DQ52 | 141 | SDA | 142 | SCL |
| 47 | DQ12 | 48 | DQ44 | 95 | DQ21 | 96 | DQ53 | 143 | Vcc | 144 | Vcc |

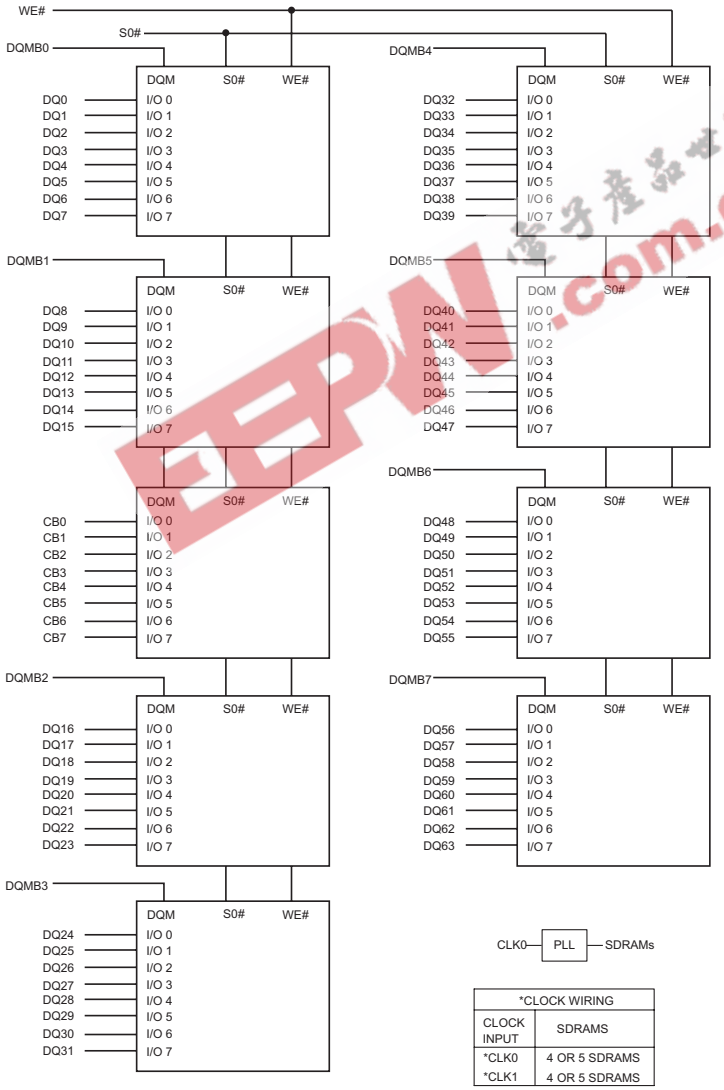
## PIN NAMES

| | |
|---|---|
| A0 – A12 | Address Input (Multiplexed) |
| BA0-1 | Select Bank |
| DQ0-63 | Data Input/Output |
| CLK0, CLK1 | Clock Input |
| CB0-7 | Check Bit (Data-In/Data-Out) |
| CKE0 | Clock Enable Input |
| CS0# | Chip Select Input |
| RAS# | Row Address Strobe |
| CAS# | Column Address Strobe |
| WE# | #Write Enable |
| DQM0-7 | DQM |
| Vcc | Power Supply (3.3V) |
| Vss | Ground |
| SDA | Serial Data I/O |
| SCL | Serial Clock |
| DNU | Do Not Use |
| NC | No Connect |

* These pins are not used in this module

** These pins should be NC in the system which does not support SPD.

## FUNCTIONAL BLOCK DIAGRAM




*CLOCK WIRING

| CLOCK INPUT | SDRAMS |
|---|---|
| *CLK0 | 4 OR 5 SDRAMS |
| *CLK1 | 4 OR 5 SDRAMS |

NOTE: DQ wiring may differ than described in this drawing however, DQ/DQMB/CKE/S relationships must be maintained as shown.

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | -1.0 ~ 4.6 | V |
| Voltage on $V_{CC}$ supply relative to $V_{SS}$ | $V_{CC}$, $V_{CCQ}$ | -1.0 ~ 4.6 | V |
| Storage Temperature | $T_{STG}$ | -55 ~ +150 | °C |
| Power Dissipation | $P_D$ | 9 | W |
| Short Circuit Current | $I_{OS}$ | 50 | mA |

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## RECOMMENDED DC OPERATING CONDITIONS

Voltage Referenced to: $V_{SS}$ = 0V, 0°C ≤ $T_A$ ≤ +70°C

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 3.0 | 3.3 | 3.6 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | 3.0 | $V_{CCQ}$ +0.3 | V | 1 |
| Input Low Voltage | $V_{IL}$ | -0.3 | — | 0.8 | V | 2 |
| Output High Voltage | $V_{OH}$ | 2.4 | — | — | V | $I_{OH}$= -2mA |
| Output Low Voltage | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$= -2mA |
| Input Leakage Current | $I_{LI}$ | -10 | — | 10 | µA | 3 |

Note: 1. $V_{IH}$ (max)= 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. $V_{IL}$ (min)= -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ $V_{IN}$ ≤ $V_{CCQ}$
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

## CAPACITANCE

$T_A$ = 25°C, f = 1MHz, $V_{CC}$ = 3.3V, $V_{REF}$ = 1.4V ± 200mV

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Input Capacitance (A0-A12) | $C_{IN1}$ | 40 | pF |
| Input Capacitance (RAS#,CAS#,WE#) | $C_{IN2}$ | 40 | pF |
| Input Capacitance (CKE0) | $C_{IN3}$ | 40 | pF |
| Input Capacitance (CK0) | $C_{IN4}$ | 6 | pF |
| Input Capacitance (CS0#) | $C_{IN5}$ | 40 | pF |
| Input Capacitance (DQM0-DQM7) | $C_{IN6}$ | 7 | pF |
| Input Capacitance (BA0-BA1) | $C_{IN7}$ | 40 | pF |
| Data Input/Output Capacitance (DQ0-DQ63) | $C_{OUT}$ | 9 | pF |
| Data Input/Output Capacitance (CB0-7) | $C_{OUT1}$ | 9 | pF |

## OPERATING CURRENT CHARACTERISTICS

($V_{CC}$ = 3.3V, $T_A$ = 0°C ≤ +70°C)

| | | | Version | | |
|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Conditions** | **133/100** | **Units** | **Note** |
| Operating Current (One bank active) | $I_{CC1}$ | Burst Length = 1<br>$t_{RC} \geq t_{RC}$ (min)<br>$I_{OL}$ = 0mA | 1,925 | mA | 1 |
| Precharge Standby Current in Power Down Mode | $I_{CC2P}$ | CKE ≤ $V_{IL}$(max), $t_{CC}$ = 10ns | 64 | mA | |
| | $I_{CC2PS}$ | CKE & CLK ≤ $V_{IL}$(max), $t_{CC}$ = ∞ | 64 | | |
| Precharge Standby Current in Non-Power Down Mode | $I_{CC2N}$ | CKE ≥ $V_{IH}$(min), CS ≥ $V_{IH}$(min), $t_{CC}$ =10ns<br>Input signals are charged one time during 20 | 395 | mA | |
| | $I_{CC2NS}$ | CKE ≥ $V_{IH}$(min), CLK ≥$V_{IL}$(max), $t_{CC}$ = ∞<br>Input signals are stable | 215 | | |
| Active Standby Current in Power-Down Mode | $I_{CC3P}$ | CKE ≥ $V_{IL}$(max), $t_{CC}$ = 10ns | 100 | mA | |
| | $I_{CC3PS}$ | CKE & CLK ≤ $V_{IL}$(max), $t_{CC}$ = ∞ | 100 | | |
| Active Standby Current in Non-Power Down Mode | $I_{CC3N}$ | CKE ≥ $V_{IH}$(min), CS ≥ $V_{IH}$(min), tcc = 10ns Input signals are changed one time during 20ns | 575 | mA | |
| | $I_{CC3NS}$ | CKE ≤ $V_{IH}$(min), CLK ≤ $V_{IL}$(max), tcc = ∞<br>Input signals are stable | 420 | mA | |
| Operating Current (Burst mode) | $I_{CC4}$ | Io = mA<br>Page burst<br>4 Banks activated<br>$t_{CCD}$ = 2CLK | 1,925 | mA | 1 |
| Refresh Current | $I_{CC5}$ | $t_{RC} \geq t_{RC}$(min) | 3,095 | mA | 2 |
| Self Refresh Current | $I_{CC6}$ | CKE ≤ 0.2V | 180 | mA | |

Notes:
1. Measured with outputs open.
2. Refresh period is 64ms.

## ORDERING INFORMATION FOR D1

| Ordering Information | Speed | CAS Latency | Height |
|---|---|---|---|
| WED3DG7266V10D1xx | 100MHz | CL=2 | 31.75 (1.250") TYP |
| WED3DG7266V7D1xx | 133MHz | CL=2 | 31.75 (1.250") TYP |
| WED3DG7266V75D1xx | 133MHz | CL=3 | 31.75 (1.250") TYP |

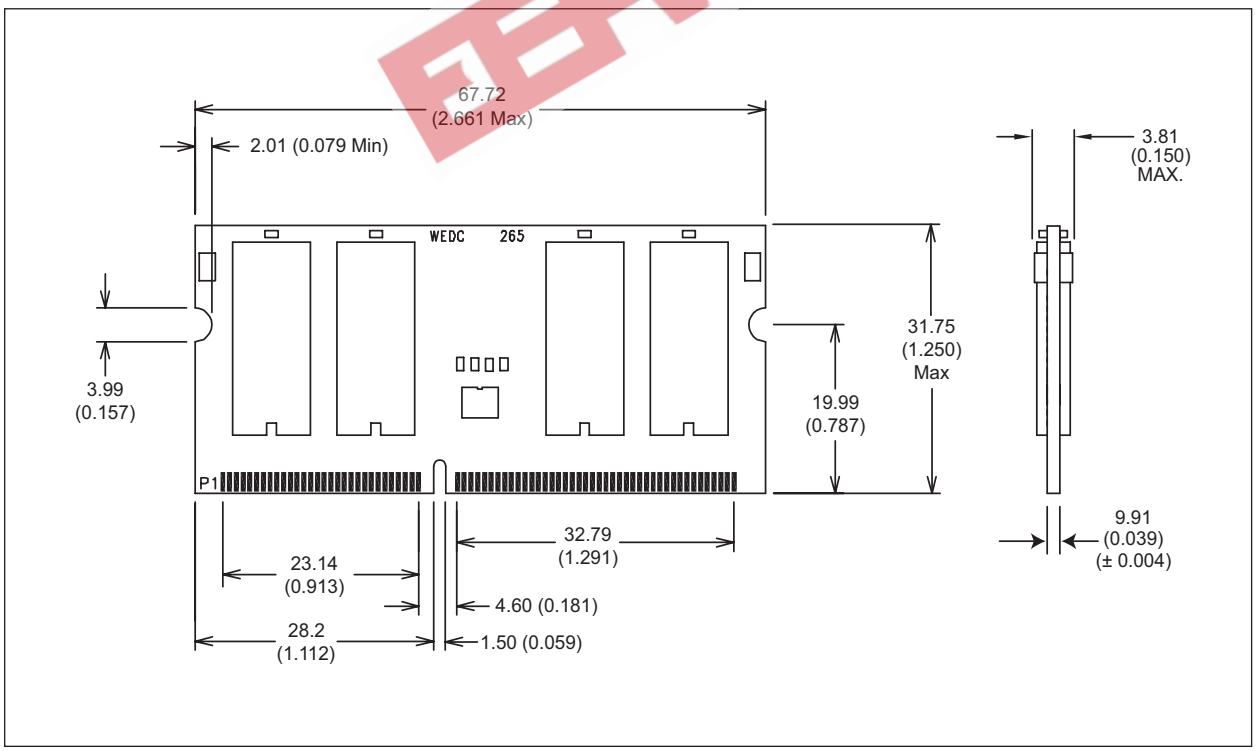
Industrial Temperature

| Ordering Information | Speed | CAS Latency | Height |
|---|---|---|---|
| WED3DG7266V10D1I-xx | 100MHz | CL=2 | 31.75 (1.250") TYP |
| WED3DG7266V7D1I-xx | 133MHz | CL=2 | 31.75 (1.250") TYP |
| WED3DG7266V75D1I-xx | 133MHz | CL=3 | 31.75 (1.250") TYP |

Notes:

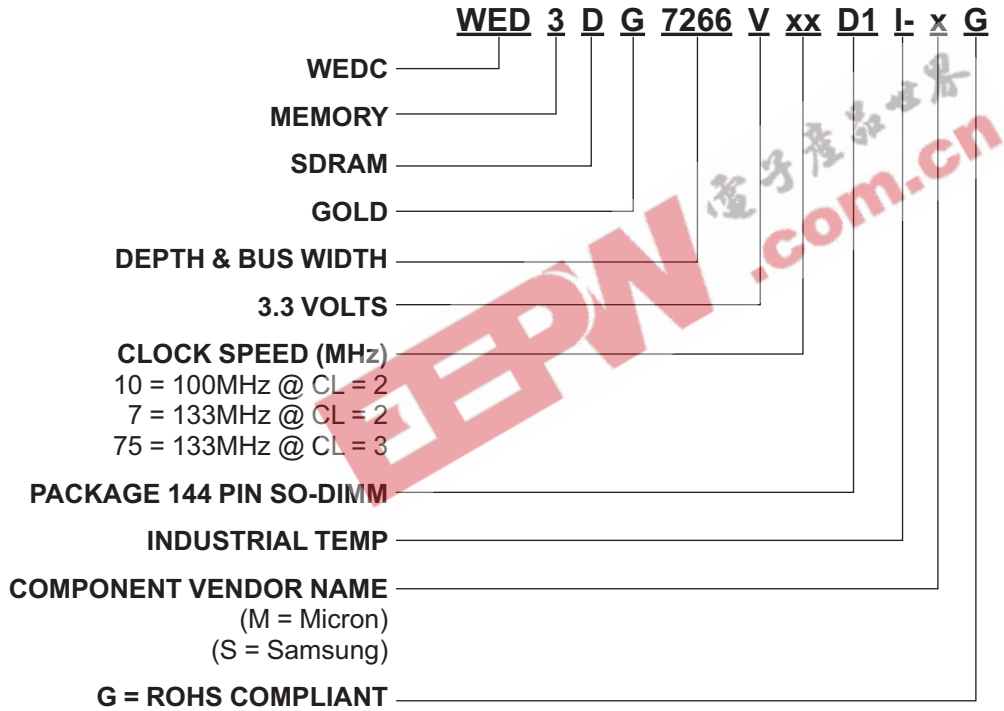
- Consult Factory for availability of RoHS products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

## PACKAGE DIMENSIONS FOR D1




* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES).

## PART NUMBERING GUIDE



## Document Title

512MB - 64Mx72 SDRAM UNBUFFERED, w/PLL

## Revision History

| Rev # | History | Release Date | Status |
|---|---|---|---|
| Rev A | Created | 3-02 | Advanced |
| Rev 0 | 0.1 Added PLL spec<br>0.2 Updated CAP and IDD specs<br>0.3 Moved status from advanced to preliminary<br>0.4 Removed “ED” from part number<br>0.5 Moved from Advanced to preliminary | 6-04 | Preliminary |
| Rev 1 | 1.1 Added “ED” to part number | 7-05 | Preliminary |
| Rev 2 | 2.1 Added RoHS, vendor source and industrial option notes<br>2.2 Added part number guide | 2-06 | Preliminary |