



## 4Mx32 5V FLASH MODULE

### FEATURES

- Access Times of 100, 120, 150ns
- Packaging:
  - 66 pin, PGA Type, 1.385" square, Hermetic Ceramic HIP (Package 402).
  - 68 lead, 40mm Low Profile CQFP (Package 502), 3.5mm (0.140") height.
  - 68 lead, Hermetic CQFP (G2T), 22.4mm (0.880") square (Package 509) 4.57mm (0.180") height. Designed to fit JEDEC 68 lead 0.990CQFJ footprint (Fig. 3)
- Sector Architecture
  - 32 equal size sectors of 64KBytes per each 2Mx8 chip
  - Any combination of sectors can be erased. Also supports full chip erase.
- Minimum 100,000 Write/Erase Cycles Minimum
- Organized as 4Mx32
- User configurable as 2x4Mx16 or 4x4Mx8 in HIP and G4T packages.
- Commercial, Industrial, and Military Temperature Ranges
- 5 Volt Read and Write. 5V ± 10% Supply.
- Low Power CMOS
- Data# Polling and Toggle Bit feature for detection of program or erase cycle completion.
- Supports reading or programming data to a sector not being erased.
- RESET# pin resets internal state machine to the read mode.
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation, Separate Power and Ground Planes to improve noise immunity

\* This product is under development, is not qualified or characterized and is subject to change without notice.

Note: For programming information refer to Flash Programming 16M5 Application Note.

**FIGURE 1 – PIN CONFIGURATION FOR WF4M32-XH2X5**

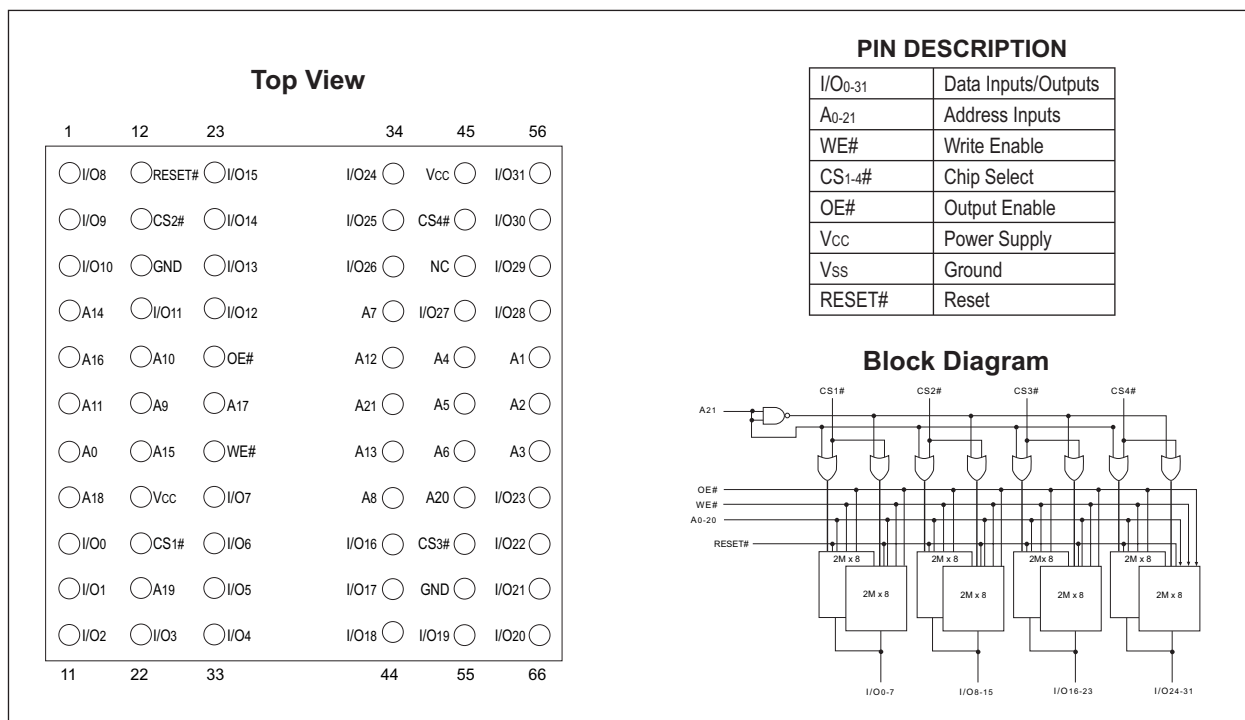




FIGURE 2 – PIN CONFIGURATION FOR WF4M32-XG4TX5

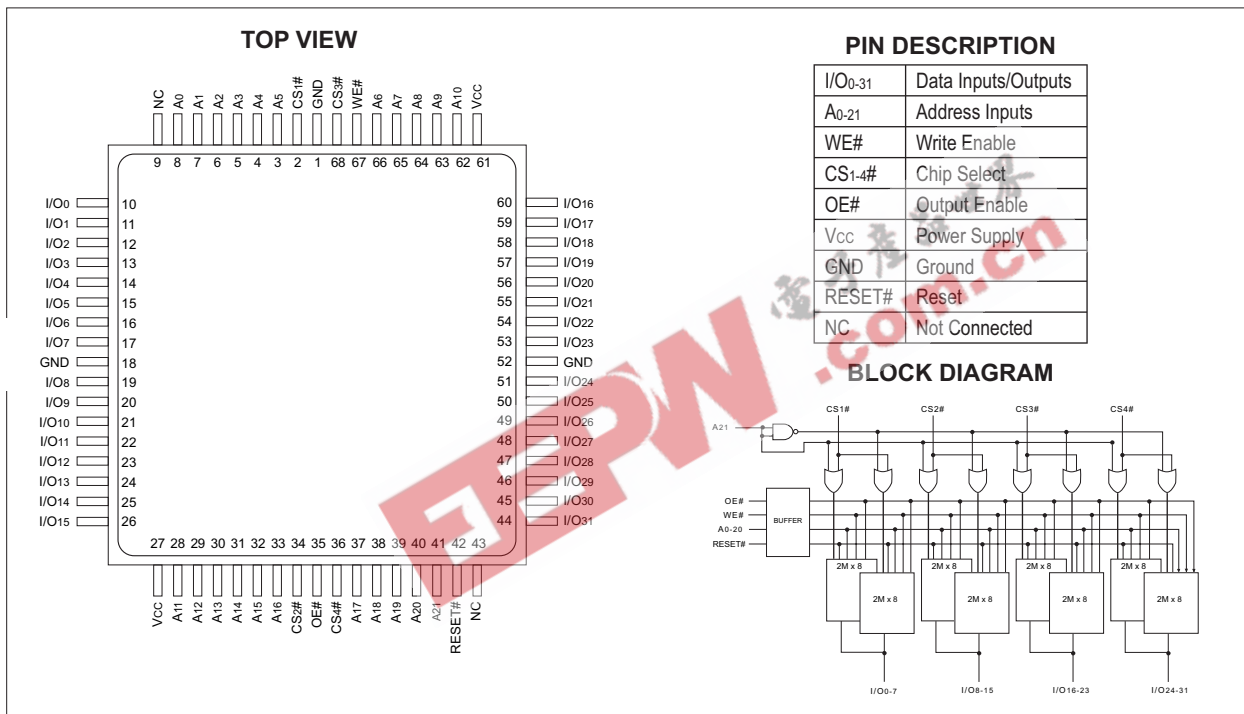
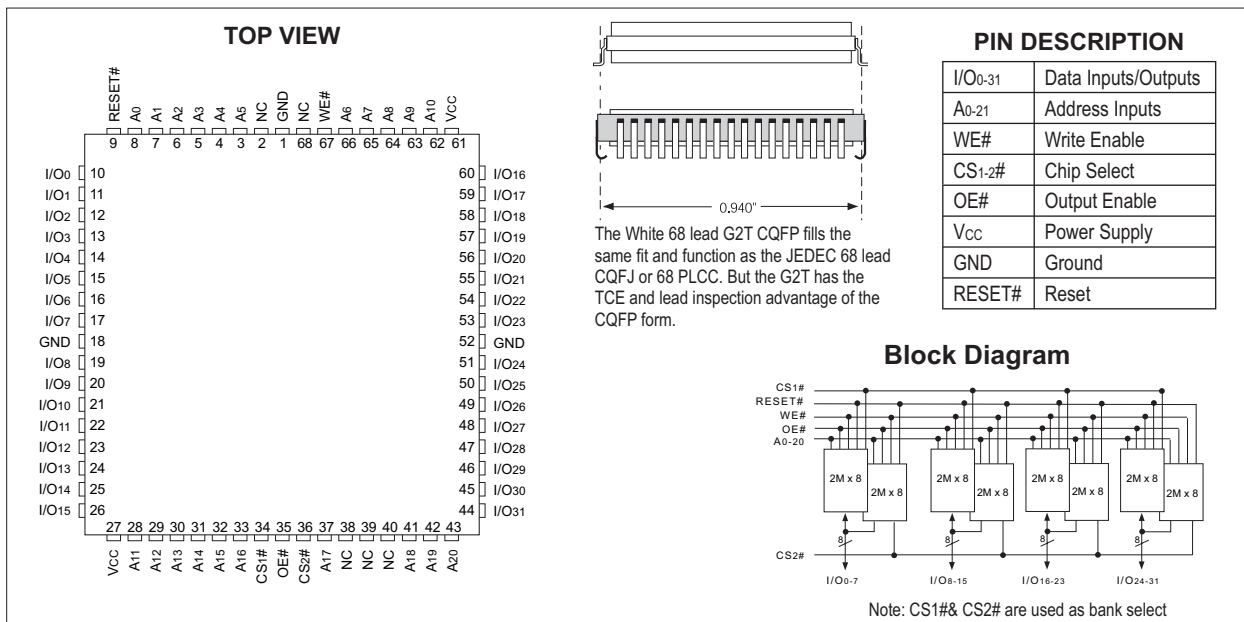


FIGURE 3 – PIN CONFIGURATION FOR WF4M32-XG2TX5





**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to V <sub>ss</sub>	V <sub>T</sub>	-2.0 to +7.0	V
Power Dissipation	P <sub>T</sub>	8	W
Storage Temperature	T <sub>STG</sub>	-65 to +125	°C
Short Circuit Output Current	I <sub>OS</sub>	100	mA
Endurance — write/erase cycles (Mil Temp)		100,000 min.	cycles
Data Retention (Mil Temp)		20	years

**CAPACITANCE**

T<sub>A</sub> = +25°C, V<sub>IN</sub> = 0V, F = 1.0MHz

Parameter	Symbol	HIP (H2)	CQFP (G2T)	CQFP(G4T)
OE# capacitance	C <sub>OE</sub>	75	75	20
WE# capacitance	C <sub>WE</sub>	75	75	20
CS# capacitance	C <sub>CS</sub>	20	50	20
Data I/O capacitance	C <sub>I/O</sub>	30	30	30
Address input capacitance	C <sub>AD</sub>	75	75	20

This parameter is guaranteed by design but not tested.

**RECOMMENDED DC OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.0	—	V <sub>CC</sub> + 0.5	V
Input Low Voltage	V <sub>IL</sub>	-0.5	—	+0.8	V
Operating Temperature (Mil.)	T <sub>A</sub>	-55	—	+125	°C
Operating Temperature (Ind.)	T <sub>A</sub>	-40	—	+85	°C

**DC CHARACTERISTICS - CMOS COMPATIBLE**

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol	Conditions	HIP		G2T		G4T		Unit
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10		10		10	μA
Output Leakage Current	I <sub>LOX2</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10		10		10	μA
V <sub>CC</sub> Active Current for Read (1)	I <sub>CC1</sub>	CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub> , f = 5MHz		320		215		345	mA
V <sub>CC</sub> Active Current for Program or Erase (2)	I <sub>CC2</sub>	CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub>		420		295		445	mA
V <sub>CC</sub> Standby Current	I <sub>CC3</sub>	V <sub>CC</sub> = 5.5, CS# = V <sub>IH</sub> , f = 5MHz, RESET# = V <sub>IH</sub>		20		2.0		95	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 12.0 mA, V <sub>CC</sub> = 4.5		0.45		0.45		0.45	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -2.5 mA, V <sub>CC</sub> = 4.5	0.85 x V <sub>CC</sub>		0.85 x V <sub>CC</sub>		0.85 x V <sub>CC</sub>		V
Low V <sub>CC</sub> Lock-Out Voltage	V <sub>LKO</sub>		3.2	4.2	3.2	4.2	3.2	4.2	V

**NOTES:**

- The I<sub>CC</sub> current listed includes both the DC operating current and the frequency dependent component (@ 5MHz). The frequency component typically is less than 2mA/MHz, with OE# at V<sub>IH</sub>.
- I<sub>CC</sub> active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions V<sub>IL</sub> = 0.3V, V<sub>IH</sub> = V<sub>CC</sub> - 0.3V

HIP = 66 pin, PGA Type, 1.385" square, Hermetic Ceramic HIP (Package 402).

G2T = 68 lead, Hermetic CQFP (G2T), 22.4mm (0.880") square. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3) (Package 509)

G4T = 68 lead, 40mm Low Profile CQFP, 3.5mm (0.140") (Package 502)



**AC Characteristics – Write/Erase/Program Operations - WE# Controlled**

V<sub>CC</sub> = 5.0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>AVAV</sub>	t <sub>WC</sub>	100		120		150		ns
Chip Select Setup Time	t <sub>ELWL</sub>	t <sub>CS</sub>	0		0		0		ns
Write Enable Pulse Width	t <sub>WLWH</sub>	t <sub>WP</sub>	45		50		50		ns
Address Setup Time	t <sub>AVWL</sub>	t <sub>AS</sub>	0		0		0		ns
Data Setup Time	t <sub>DVWH</sub>	t <sub>DS</sub>	45		50		50		ns
Data Hold Time	t <sub>WHDX</sub>	t <sub>DH</sub>	0		0		0		ns
Address Hold Time	t <sub>WLAX</sub>	t <sub>AH</sub>	45		50		50		ns
Write Enable Pulse Width High	t <sub>WHWL</sub>	t <sub>WPH</sub>	20		20		20		ns
Duration of Byte Programming Operation (1)	t <sub>WHWH1</sub>			300	300			300	μs
Sector Erase (2)	t <sub>WHWH2</sub>			15	15			15	sec
Read Recovery Time before Write	t <sub>GHWL</sub>		0		0		0		μs
V <sub>CC</sub> Setup Time	t <sub>VCS</sub>		50		50		50		μs
Chip Programming Time				44	44		44		sec
Chip Erase Time (3)				256	256		256		sec
Output Enable Hold Time (4)	t <sub>OEHL</sub>		10		10		10		ns
RESET# Pulse Width	t <sub>RP</sub>		500		500		500		ns

**NOTES:**

1. Typical value for t<sub>WHWH1</sub> is 7μs.
2. Typical value for t<sub>WHWH2</sub> is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

**AC CHARACTERISTICS – READ-ONLY OPERATIONS**

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol		-1000		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>AVAV</sub>	t <sub>RC</sub>	100		120		150		ns
Address Access Time	t <sub>AVQV</sub>	t <sub>ACC</sub>		100		120		150	ns
Chip Select Access Time	t <sub>ELOV</sub>	t <sub>CE</sub>		100		120		150	ns
Output Enable to Output Valid	t <sub>GLQV</sub>	t <sub>OE</sub>		40		50		55	ns
Chip Select High to Output High Z (1)	t <sub>EHQZ</sub>	t <sub>DF</sub>		20		30		35	ns
Output Enable High to Output High Z (1)	t <sub>GHQZ</sub>	t <sub>DF</sub>		20		30		35	ns
Output Hold from Addresses, CS# or OE# Change, whichever is First	t <sub>AXQX</sub>	t <sub>OH</sub>	0		0		0		ns
RESET# Low to Read Mode (1)		t <sub>READY</sub>		20		20		20	μs

1. Guaranteed by design, not tested.



**AC CHARACTERISTICS FOR G2T PACKAGE – WRITE/ERASE/PROGRAM OPERATIONS,  
CS# CONTROLLED**

V<sub>CC</sub> = 5.0V, GND = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>WAV</sub>	t <sub>WC</sub>	100		120		150		ns
Write Enable Setup Time	t <sub>WLEL</sub>	t <sub>WS</sub>	0		0		0		ns
Chip Select Pulse Width	t <sub>LEH</sub>	t <sub>CP</sub>	45		50		50		ns
Address Setup Time	t <sub>AVEL</sub>	t <sub>AS</sub>	0		0		0		ns
Data Setup Time	t <sub>DVEH</sub>	t <sub>DS</sub>	45		50		50		ns
Data Hold Time	t <sub>EDX</sub>	t <sub>DH</sub>	0		0		0		ns
Address Hold Time	t <sub>ELAX</sub>	t <sub>AH</sub>	45		50		50		ns
Chip Select Pulse Width High	t <sub>EHL</sub>	t <sub>CPH</sub>	20		20		20		ns
Duration of Byte Programming Operation (1)	t <sub>WHWH1</sub>			300		300		300	μs
Sector Erase Time (2)	t <sub>WHWH2</sub>			15		15		15	sec
Read Recovery Time	t <sub>GHEL</sub>		0		0		0		μs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		t <sub>OEH</sub>	10		10		10		ns

**NOTES:**

1. Typical value for t<sub>WHWH1</sub> is 7μs.
2. Typical value for t<sub>WHWH2</sub> is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.



**AC CHARACTERISTICS FOR G4T AND H2 PACKAGES – WRITE/ERASE/PROGRAM OPERATIONS  
- WE# CONTROLLED**

V<sub>CC</sub> = 5.0V, T<sub>A</sub> = -55°C, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>AVAV</sub>	t <sub>WC</sub>	100		120		150		ns
Chip Select Setup Time	t <sub>ELWL</sub>	t <sub>CS</sub>	0		0		0		ns
Write Enable Pulse Width	t <sub>WLWH</sub>	t <sub>WP</sub>	45		50		50		ns
Address Setup Time	t <sub>AVWL</sub>	t <sub>AS</sub>	0		0		0		ns
Data Setup Time	t <sub>DVWH</sub>	t <sub>DS</sub>	45		50		50		ns
Data Hold Time	t <sub>WHDX</sub>	t <sub>DH</sub>	15		15		15		ns
Address Hold Time (1)	t <sub>WLAX</sub>	t <sub>AH</sub>	45		50		50		ns
Write Enable Pulse Width High (2)	t <sub>WHWL</sub>	t <sub>WPH</sub>	20		20		20		ns
Duration of Byte Programming Operation (3)	t <sub>WHWH1</sub>			300		300		300	μs
Sector Erase (4)	t <sub>WHWH2</sub>			15		15		15	sec
Read Recovery Time before Write	t <sub>GHWL</sub>		0		0		0		μs
V <sub>CC</sub> Setup Time	t <sub>VCS</sub>		50		50		50		μs
Chip Programming Time				44		44		44	sec
Chip Erase Time (5)				256		256		256	sec
Output Enable Hold Time (6)		t <sub>OEH</sub>	10		10		10		ns
RESET# Pulse Width		t <sub>RP</sub>	500		500		500		ns

**NOTES:**

1. A21 must be held constant until WE# or CS# go high, whichever occurs first.
2. Guaranteed by design, but not tested.
3. Typical value for t<sub>WHWH1</sub> is 7μs.
4. Typical value for t<sub>WHWH2</sub> is 1sec.
5. Typical value for Chip Erase Time is 32sec.
6. For Toggle and Data Polling.

**AC CHARACTERISTICS FOR G4T AND H2 PACKAGES – READ-ONLY OPERATIONS**

V<sub>CC</sub> = 5.0V, T<sub>A</sub> = -55°C, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol		-1000		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	T <sub>AVAV</sub>	T <sub>RC</sub>	100		120		150		ns
Address Access Time	T <sub>AVQV</sub>	T <sub>ACC</sub>		100		120		150	ns
Chip Select Access Time	T <sub>ELQV</sub>	T <sub>CE</sub>		100		120		150	ns
Output Enable to Output Valid	T <sub>GLQV</sub>	T <sub>OE</sub>		50		50		55	ns
Chip Select High to Output High Z	T <sub>EHQZ</sub>	T <sub>DF</sub>		40		45		45	ns
Output Enable High to Output High Z	T <sub>GHQZ</sub>	T <sub>DF</sub>		40		45		45	ns
Output Hold from Addresses, CS# or OE# Change, whichever is First	T <sub>AXQX</sub>	T <sub>OH</sub>	0		0		0		ns
RESET# Low to Read Mode		T <sub>READY</sub>		20		20		20	μs



AC CHARACTERISTICS FOR G4T AND H2 PACKAGES – WRITE/ERASE/PROGRAM OPERATIONS, CS# CONTROLLED

VCC = 5.0V, GND = 0V, -55°C ≤ TA ≤ +125°C

Parameter	Symbol		-100		-120		-150		Unit
	Min	Max	Min	Max	Min	Max			
Write Cycle Time	t <sub>AVAV</sub>	t <sub>WC</sub>	100		120		150		ns
Write Enable Setup Time	t <sub>WLEL</sub>	t <sub>WS</sub>	0		0		0		ns
Chip Select Pulse Width	t <sub>LELH</sub>	t <sub>CP</sub>	45		50		50		ns
Address Setup Time	t <sub>VEL</sub>	t <sub>AS</sub>	0		0		0		ns
Data Setup Time	t <sub>DVEH</sub>	t <sub>DS</sub>	45		50		50		ns
Data Hold Time	t <sub>EHDX</sub>	t <sub>DH</sub>	15		15		15		ns
Address Hold Time (1)	t <sub>ELAX</sub>	t <sub>AH</sub>	45		50		50		ns
Chip Select Pulse Width High	t <sub>EHEL</sub>	t <sub>CPH</sub>	20		20		20		ns
Duration of Byte Programming Operation (2)	t <sub>WHWH1</sub>			300		300		300	μs
Sector Erase Time (3)	t <sub>WHWH2</sub>			15		15		15	sec
Read Recovery Time	t <sub>GHEL</sub>		0		0		0		μs
Chip Programming Time				44		44		44	sec
Chip Erase Time (4)				256		256		256	sec
Output Enable Hold Time (5)		t <sub>OEH</sub>	10		10		10		ns

NOTES:

- A21 must be held constant until WE# or CS# go high, whichever occurs first.
- Typical value for t<sub>WHWH1</sub> is 7 μs.
- Typical value for t<sub>WHWH2</sub> is 1 sec.
- Typical value for Chip Erase Time is 32sec.
- For Toggle and Data Polling.

FIGURE 4 – AC TEST CIRCUIT

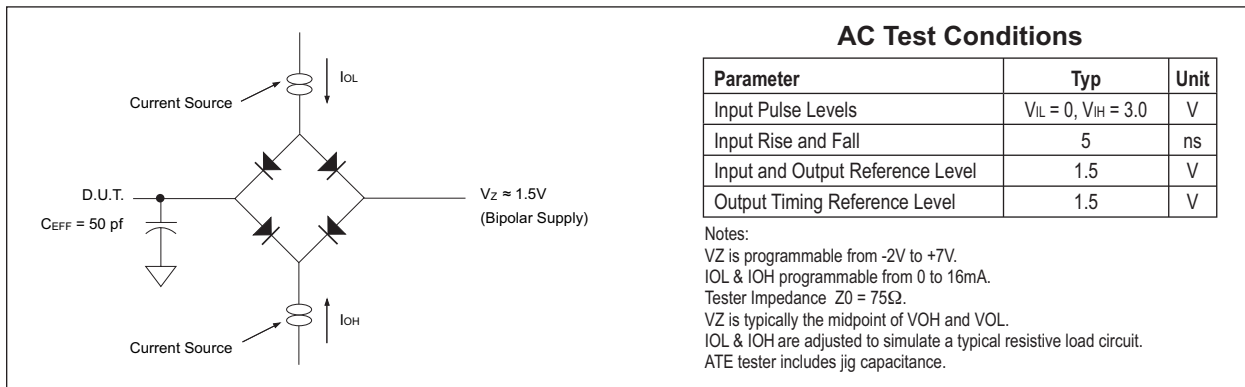


FIGURE 5 – RESET TIMING DIAGRAM

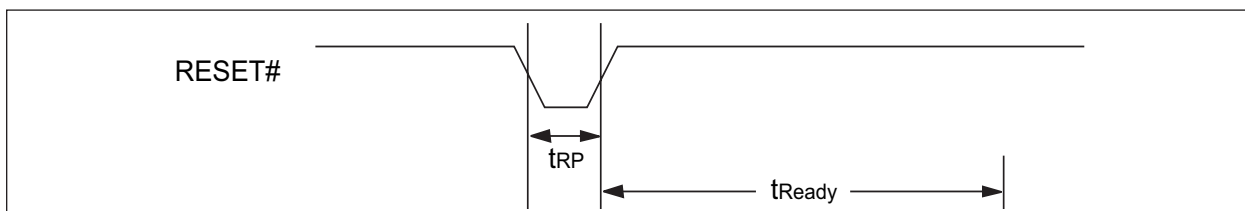




FIGURE 6 – AC WAVEFORMS FOR READ OPERATIONS

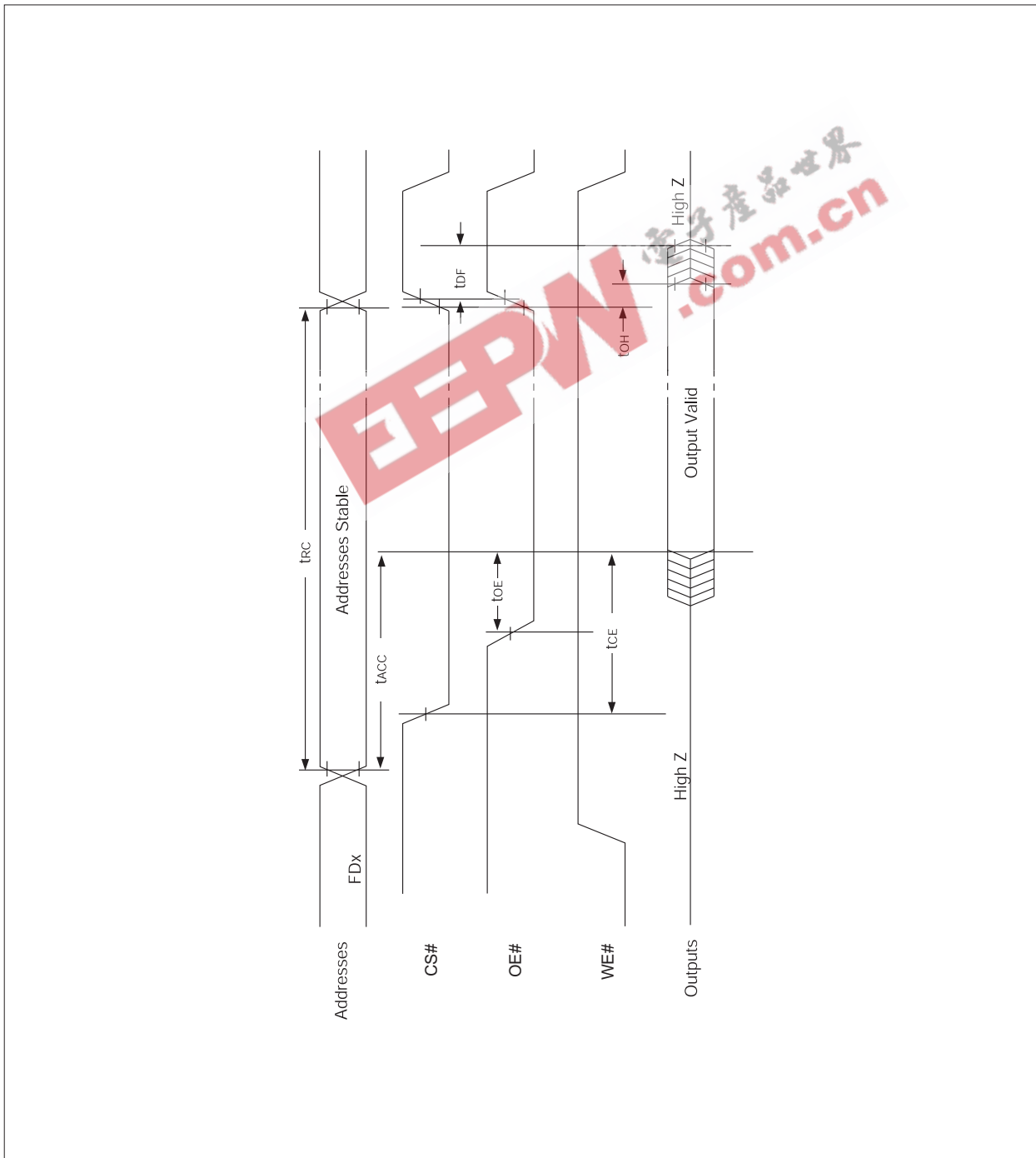
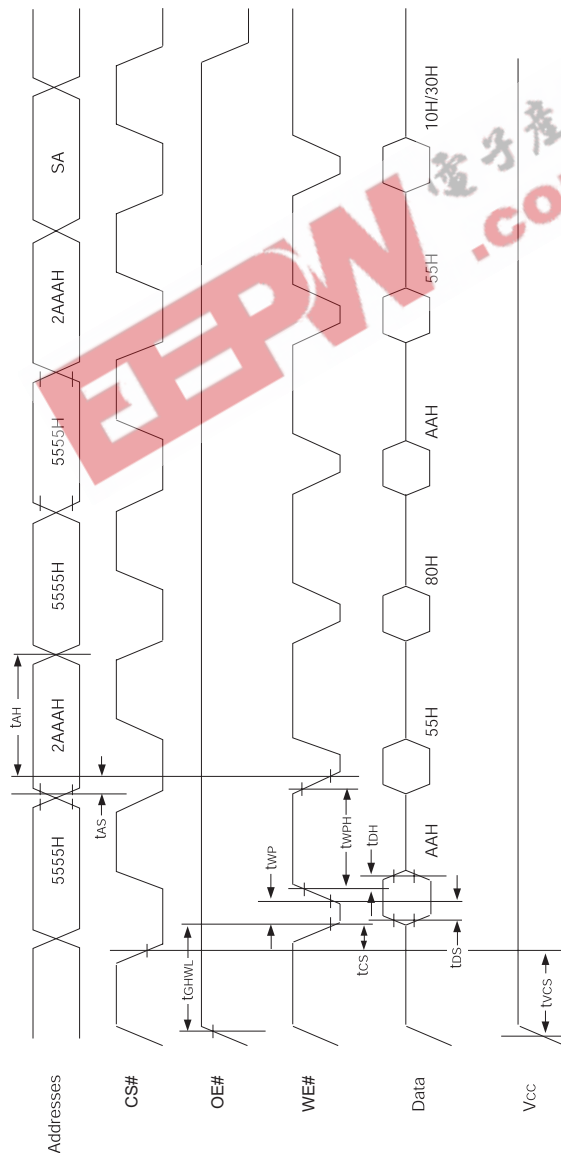








FIGURE 8 – AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



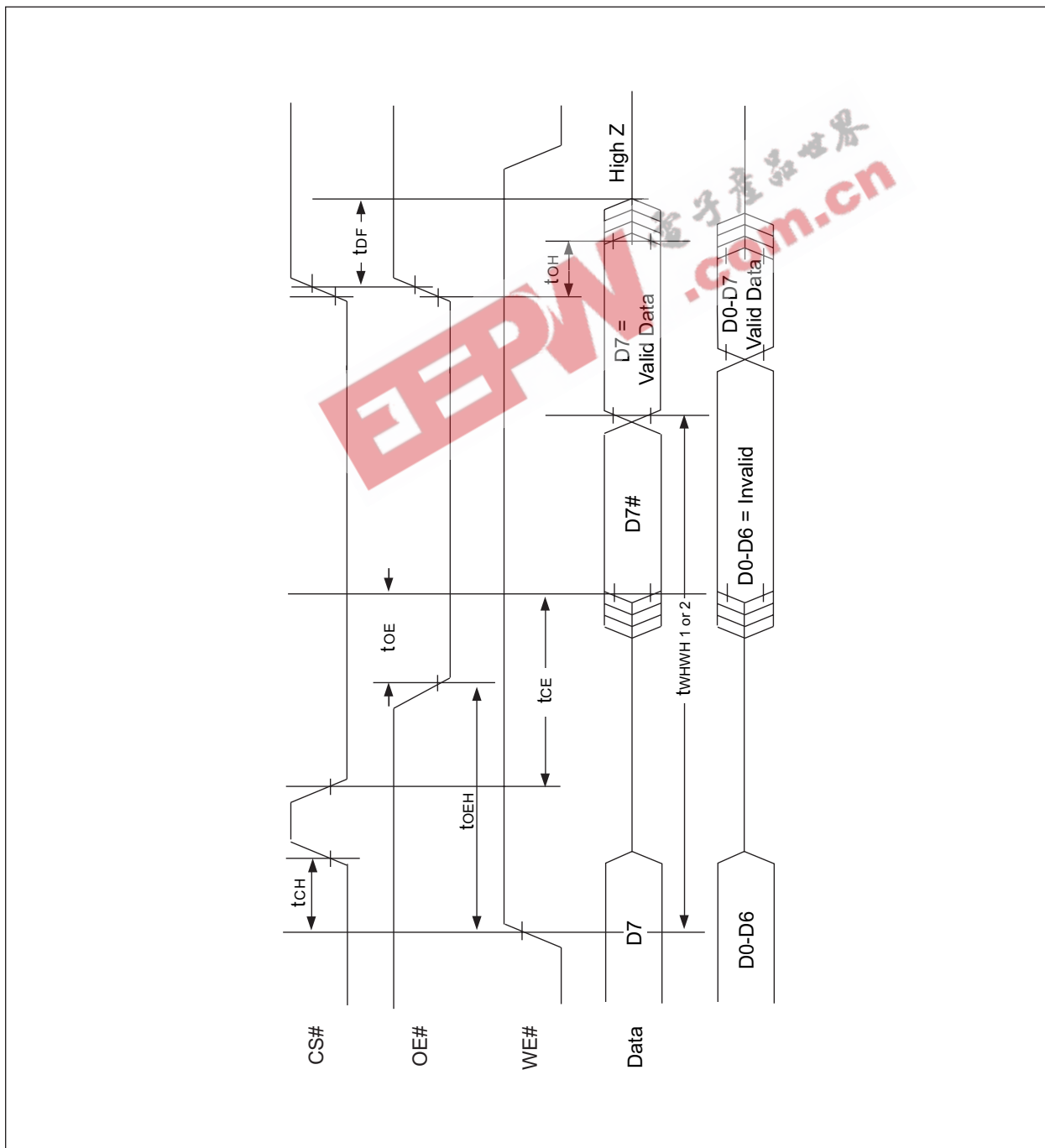
电子产品世界  
www.epw.com.cn

NOTE:

- 1. SA is the sector address for Sector Erase.



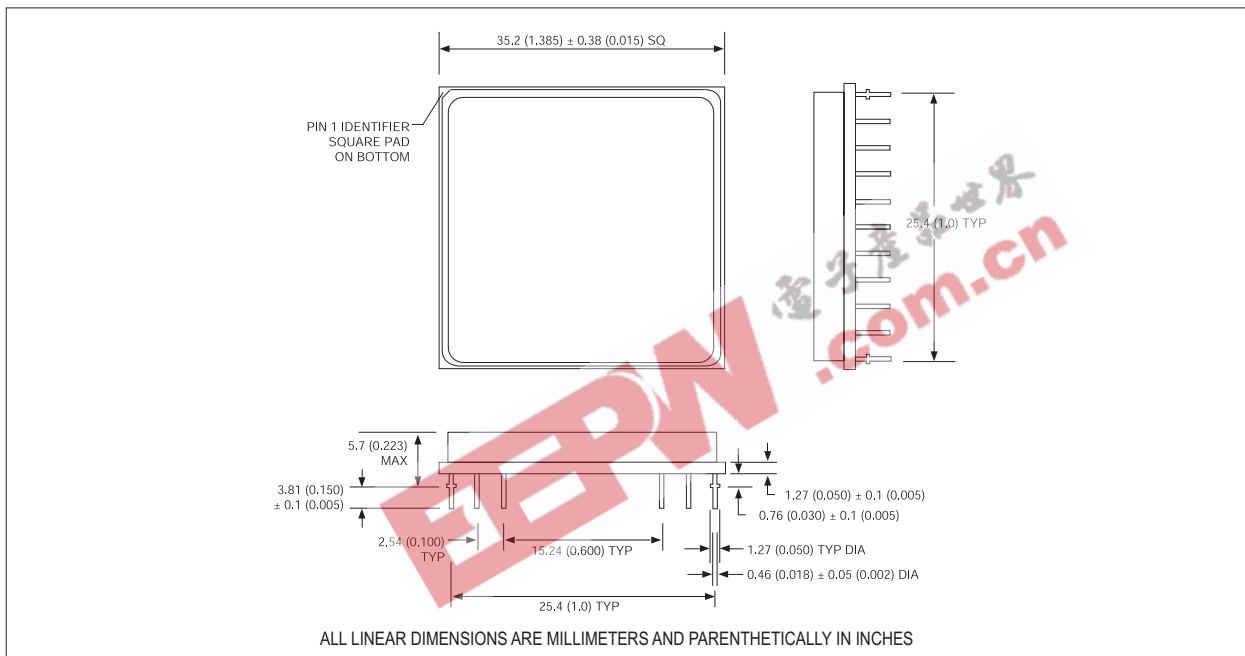
**FIGURE 9 – AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS**



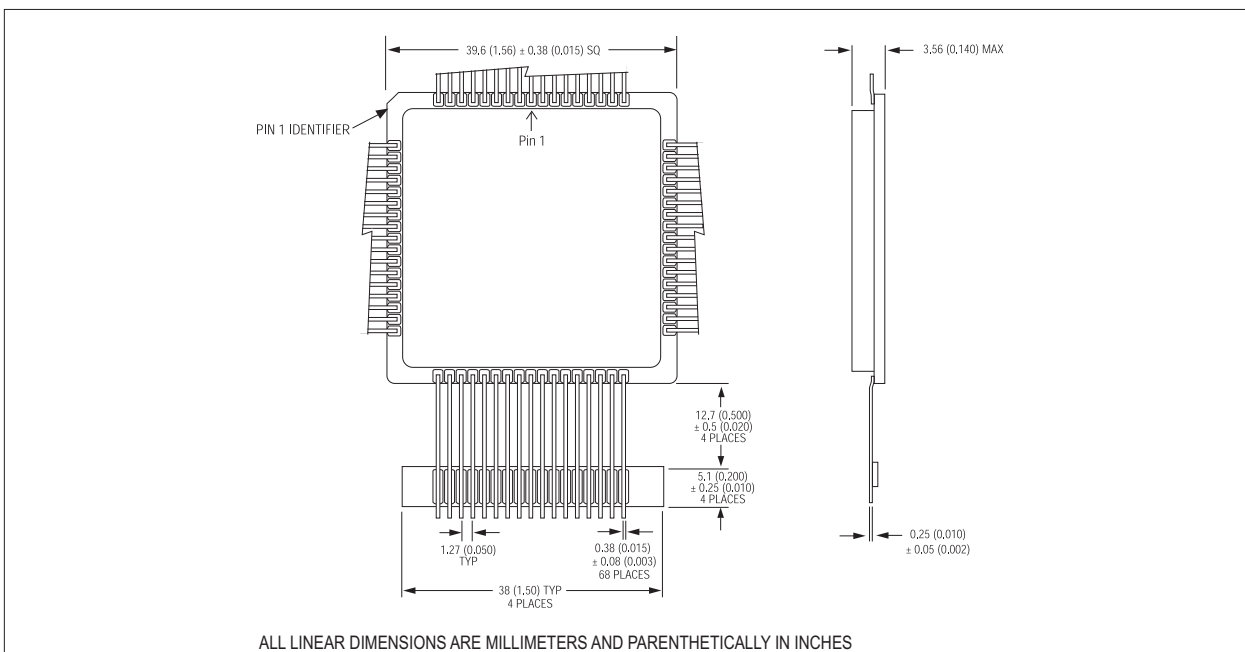




PACKAGE 402: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)

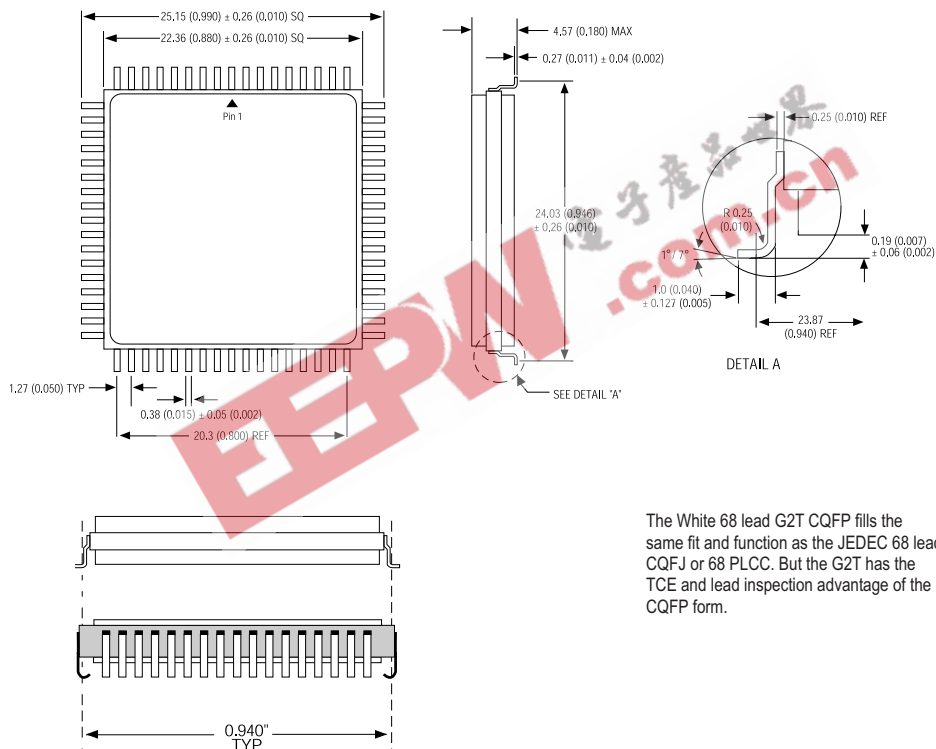


PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)





**PACKAGE 509: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)**



The White 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



**ORDERING INFORMATION**

