Winbond W551Cxxx

Serial Voice Memory

Data Sheet

Winbond Electronics Corp.

Contents

General Description

The W551Cxxx series is designated to interface with Winbond *PowerSpeech™*, *BandDirector™*, and *ViewTalk™* family ICs directly. Application with *PowerSpeech™*, *BandDirector™*, and *ViewTalk™* the serial voice memory W551Cxxx can lengthen the playback duration to meet the increasing market demand on complicated scenarios. The W551Cxxx was already utilized the same serial interface as Winbond serial flash memory W55Fxx for designer to simulate & verify the memory contents in advance. Besides that, W551Cxxx also provides a "Self-test mode" to verify the voice memory contents easily and quickly.

1.1 W551Cxxx Product Selection Guide

W551Cxxx Serial Voice Memory is used to store pre-determined data. To communicate with W551Cxxx in serial data mode, the connection interface total pin counts can be reduced to three pins only. The following table is shown the product selection guide of part number vs. memory density.

Part #	W551C002	W551C005	W551C010	W551C020	W551C040	W551C060	W551C080
Density	256K bits	512K bits	1M bits	2M bits	4M bits	6M bits	8M bits

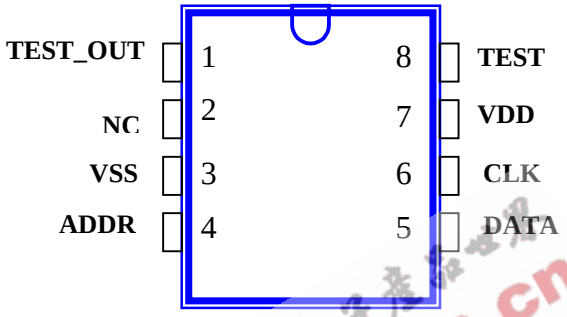
Features

2.1 W551Cxxx Features Description

- Wide range of operating voltage: **2.4V ~ 5.5V**
- Operating frequency up to **1 MHz** (@VDD = 2.4V)
- Versatile operation modes
  - Serial read mode
  - Serial check-sum output mode
  - Fast self-test mode
- Directly cascade for longer duration applications
- Serial shift-in address bus
- Serial data mode, the connection interface can be reduced to three pins:
  - CLK, ADDR, DATA
- Read access time: **500 ns**
- Low power consumption
  - Operation current: **5 mA (typ.)**
  - Standby current: **2 uA (typ.)**

2.2 W551Cxxx Pin Configuration & Description

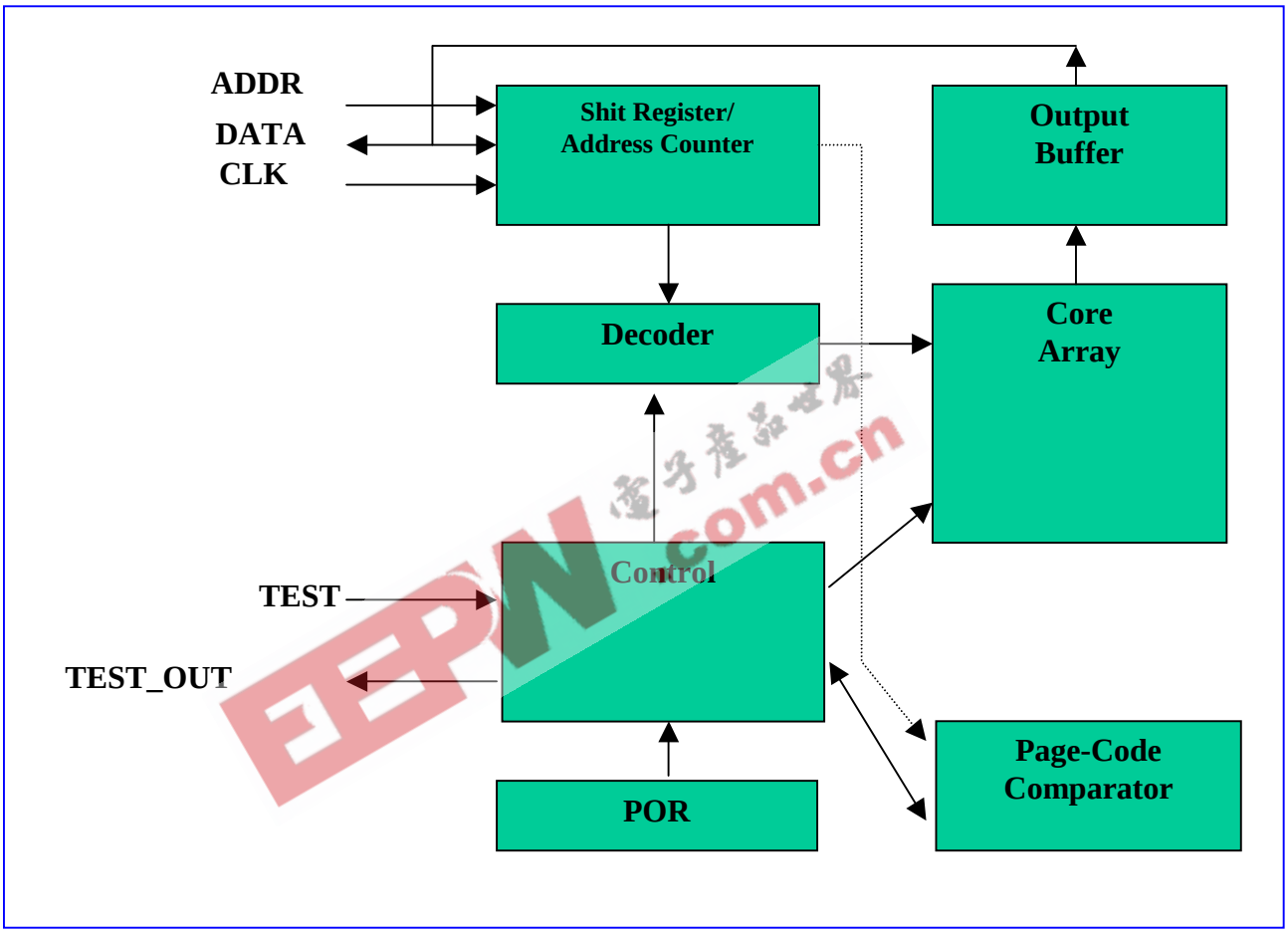
Pin Configuration



Pin Description

Pin Name	I/O	Description
TEST	I	Internal pulled high. Set TEST to low will enable **"Self-test"** function.
TEST_OUT	O	The output pin indicates the result of self-test process. For correct result, a logic " **0** " signal will be output. For incorrect result, a logic " **1** " signal will be output. At Power-On-Reset condition, it outputs a logic " **1** " signal.
ADDR	I	Clock input for shift-in start address; The first rising-edge signal will reset the address counter.
DATA	IO	Bi-directional data pin with the internal pull-high.
CLK	I	Clock input for data read-out.
VDD	Power	Positive power supply pin.
VSS	Ground	

2.3 W551Cxxx System Block Diagram



Function Description

3.1 W551Cxxx Functional Description

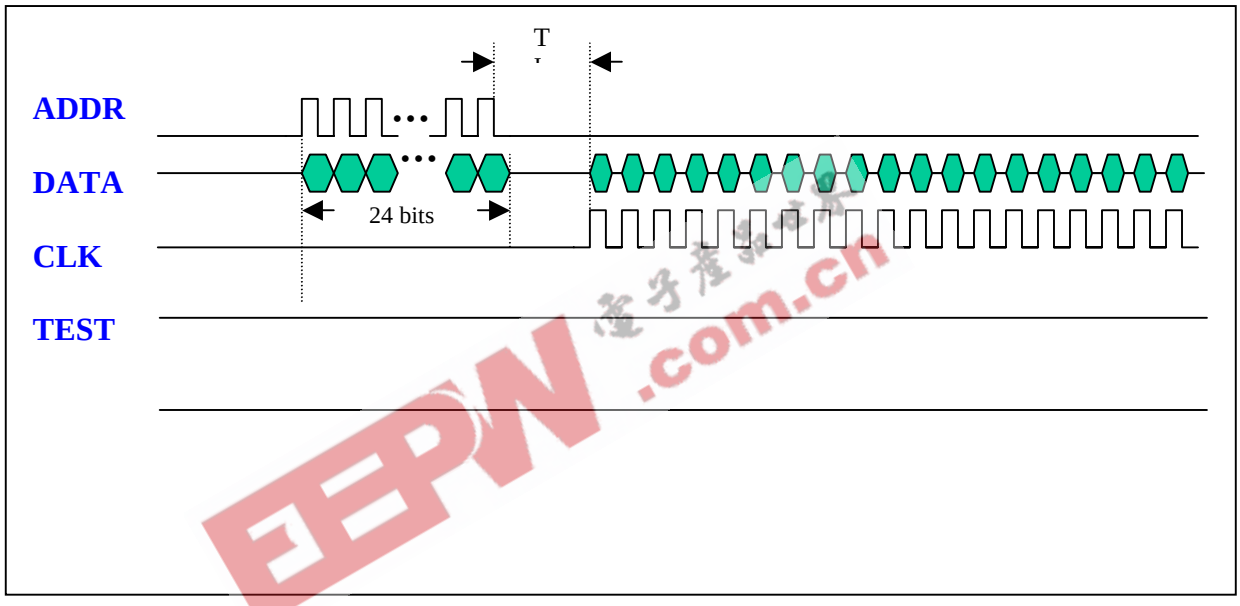
The maximum number of the ADDR clock is 24 bits. The address data is shifted into the 24 bits address counter by the ADDR clock. The MSB x bits of the address counter are the page codes, and the rest (24 - x) bits are the bit of address. Note that the MSB is shifted first. The MSB 5 bits of the address counter are always gating (exclusive OR) with the content of the page-code cells to determine whether these two articles are match or not. Only when the page codes are matched with the content of the page-code cells, this device can be enabled. The counting source of the address counter is the CLK clock, the falling edge signal of the CLK clock up-count the counter.

In normal-read mode the ADDR and CLK clock cannot be active simultaneously. The first rising edge signal of the ADDR clock after CLK clocking will reset the address shift registers. The following table describes the needed bits of ″page code″:

Part #	W551C002	W551C005	W551C010	W551C020	W551C040	W551C060	W551C080
Density	256K bits	512K bits	1M bits	2M bits	4M bits	6M bits	8M bits
Bits of page code	6	5	4	3	2	2	1

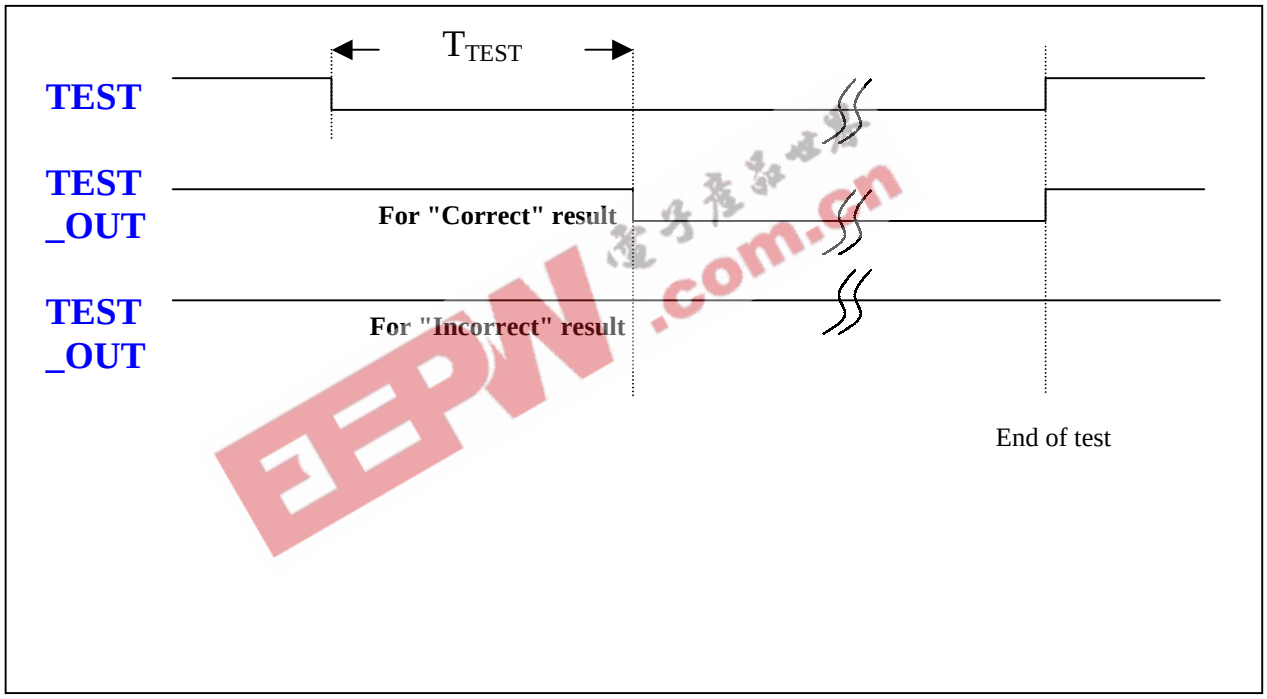
3.2 W551Cxxx Normal Read Mode

This chip can also be connected with Winbond *PowerSpeech*™ , *BandDirector*™ , and *ViewTalk*™ series directly. Because in power-on condition, the default function mode is the normal read mode, then the mode selected procedure can be skipped.



3.3 W551Cxxx Self-test Mode

In normal read mode, the TEST pin is internally pulled high, and the TEST_OUT pin is in logic ' **1** ' state. When the TEST pin is pulled low, the W551Cxxx enters the "self-test mode". In this mode, the self-test process is started at the falling edge of the TEST signal. The self-test process accumulates each byte (8 bit) of voice memory content from address 00000h to 7FFFFh. If the accumulated result is 00h, a logic ' **0** ' will be output from TEST_OUT pin. Or else, a logic ' **1** ' signal will be output from TEST_OUT pin.



Electrical Characteristics

4.1 W551Cxxx Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITION	RATING	UNIT
Operation Temperature	TOPR	-	0 to +70	° C
Storage Temperature	TSTG	-	-65 to +150	° C
Power Supply (VDD-VSS)	VDD-VSS	-	-0.3 to +7.0	V
Input D.C. Voltage	VDC	All pins	-0.5 to Vcc+1.0	V
Transient Voltage (<20ns)	VTRAN	All pins	-1.0 to Vcc+1.0	V

4.2 W551Cxxx DC Characteristics

VDD = 4.5V, TA = 25° C

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Operating Voltage	V_{OP}	-	2.4 **(Note)**	4.5	5.5	V
Operating Current	I_{OP}	In normal read mode, DATA, TEST & TEST_OUT pins open; f=1MHz	-	5	10	mA

Standby Current	I_{SB}	All inputs = GND; DATA, TEST & TEST_OUT pins open	-	1	2	uA
Input Leakage Current for DATA	I_{LI1}	V_{IN} = 0 V	-	-	-4.5	uA
Input Leakage Current for TEST	I_{LI2}	V_{IN} = 4.5 V	22.5	45	90	uA
Input Low Voltage	V_{IL}	All input pins	-0.3	-	0.8	V
Input High Voltage	V_{IH}	All input pins	2.0	-	VDD	V
Output Sink Current	I_{OL}	V_{OL}= 0.5V	2.5	5		mA
Output Drive Current	I_{OH}	V_{OH} = 4.0V	-2.5	-5		mA
ESD capability	V_{ESD}	-	2	-	-	KV

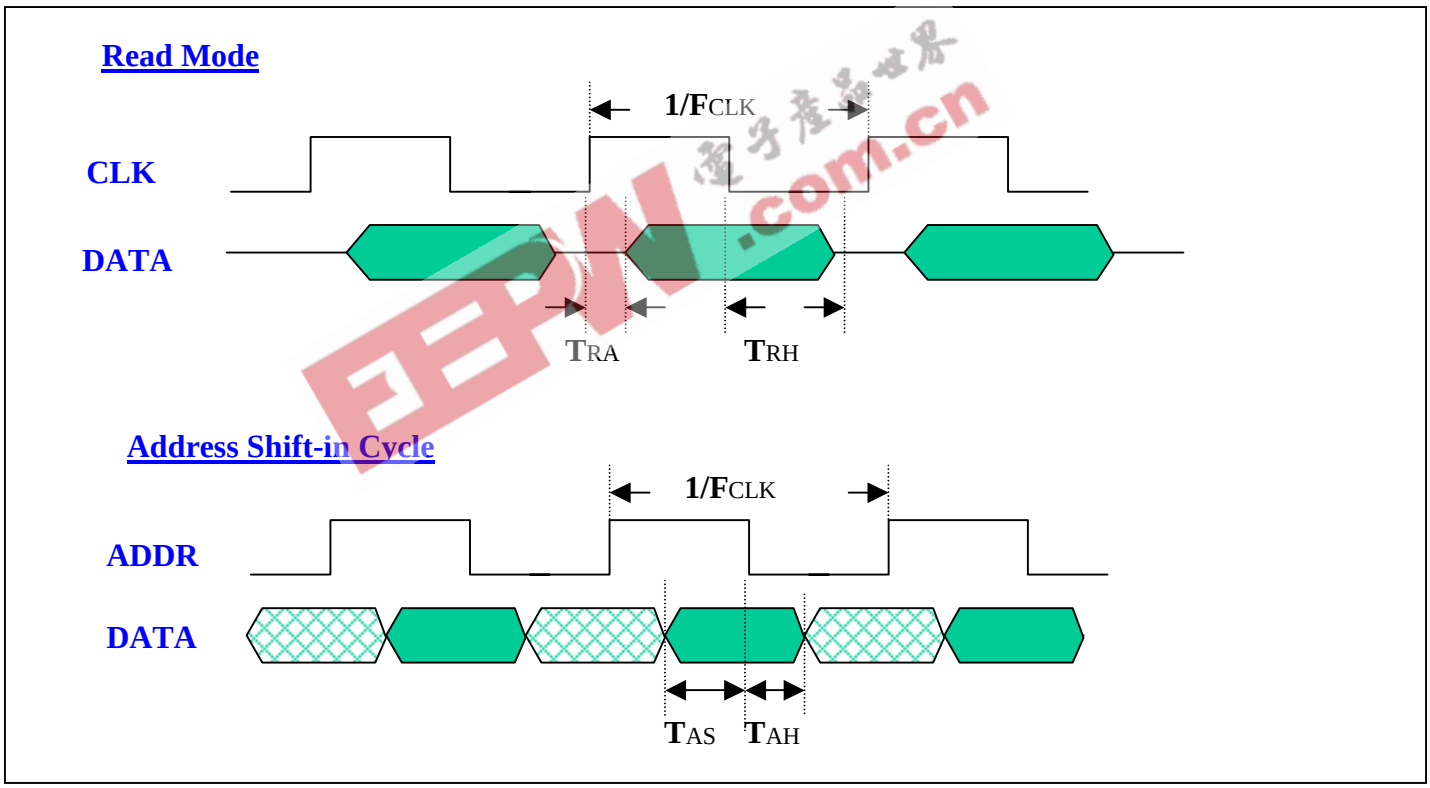
4.3 W551Cxxx AC Characteristics

VDD = 4.5V TA = 25° C

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Clock frequency of ADDR	FADDR	-	-	-	1	MHz
Clock frequency of CLK	FCR	-	-	-	1	MHz
Interval time between ADDR and CLK	TI	Read mode	1	-	-	uS
Interval between DATA to another pin active	TCFA	-	10	-	-	uS
Data access time	TRA	Read mode	-	-	500	nS
Data setup time	TAS	Address shift-in	250	-	-	nS
Data hold time	TRH	Read mode	0	-	-	nS
	TAH	Address shift-in	10	-	-	nS
Self-test time	T_{TEST}	Self-test mode		500		mS

Timing Waveform

5.1 W551Cxxx Timing Waveform

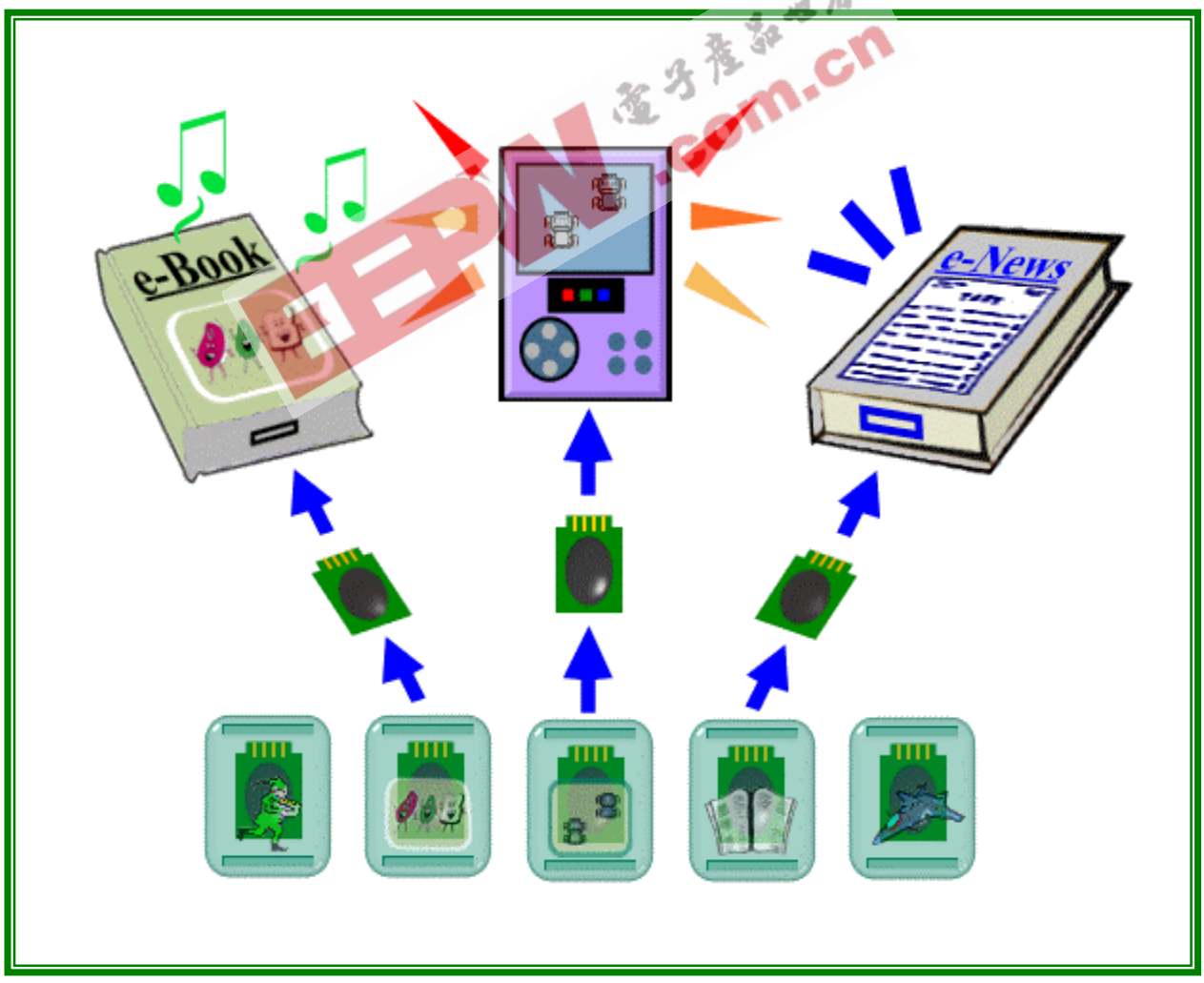


Note: The duty cycle of any clock is 50%

Applications

6.1 W551Cxxx Applications

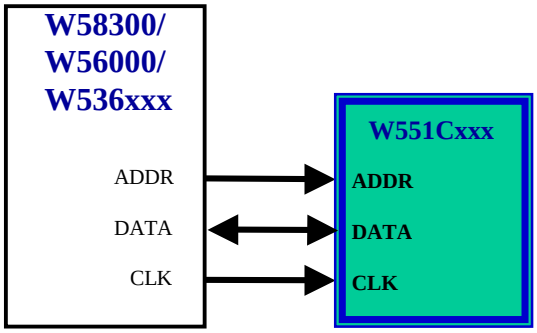
W551Cxxx Applications for e-Book, e-Magazine, e-Novel, e-Story Book, or Hand-held Game



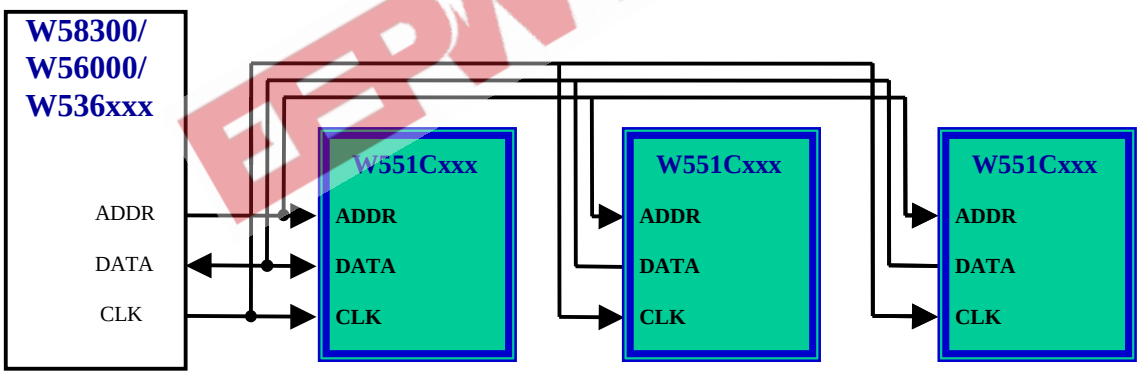
6.2 W551Cxxx Application Circuits

Application Circuits (for reference only)

❑ With *PowerSpeech*™, *BandDirector*™, *ViewTalk*™ Applications



❑ For Cascading Applications



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