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HIGH FIDELITY Power Speech ™

GENERAL DESCRIPTION

W583xxx are fabricated using the Winbond CMOS process. The W583xxx family is a new member of the PowerSpeech™ synthesizer series, with voice quality which is even better than before. The W583xxx family has adopted the same architecture as the PowerSpeech™ synthesizers while replacing the 4-bit ADPCM algorithm with Winbond′s new high fidelity voice synthesis algorithm to produce better quality voice. W583xxx provides IR function, CPU interface, pad option for Ring or Crystal oscillator and voice output in DAC current or PWM type.

According different voice duration, there are 11 bodies in W583xxx family, list them below.

PART NO.	W583S10	W583S15	W583S20	W583S25	W583S30	W583S40
Duration	10 sec	15 sec	20 sec	25 sec	30 sec	40 sec
PART NO.	W583S50	W583S60	W583S80	W583S99	W583M02	
Duration	50 sec	60 sec	80 sec	99 sec	120 sec	

Notes:
1. The voice duration is estimated by 6.4 KHz sampling rate.
2. W583S10 provides less I/O pins, and do not provide crystal oscillator.

FEATURES

- Programmable speech synthesizer
- New high fidelity synthesis algorithm
- Wide operating voltage range: 2.4 - 5.5 Volts
- Direct drive speaker by PWM output or Built-in 8-bit D/A converter
- Supports CPU interface operation
- IR interface for command Transmission and Receiving
- Symbolic compiler supported
- Instruction cycle $\leq$ 400 μS typically
- Section control
  - − Variable frequency: 4.8/6/8/12 KHz
  - − LED: ON/OFF
- Eight general-purpose registers R0-R7
- Pad option for Ring or Crystal oscillator[1]
- 8 trigger inputs - with separate control of falling/rising edge trigger[2]
- 8 STOP outputs[3]
- Number of interrupt vector / label up to 2,048

Notes:
1. W583S10 provide ring oscillator only.
2. Only 4 trigger pins in W583S10.
3. Only 5 STOP outputs in W583S10.

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BLOCK DIAGRAM

W583S15 to W583M02

W583S10
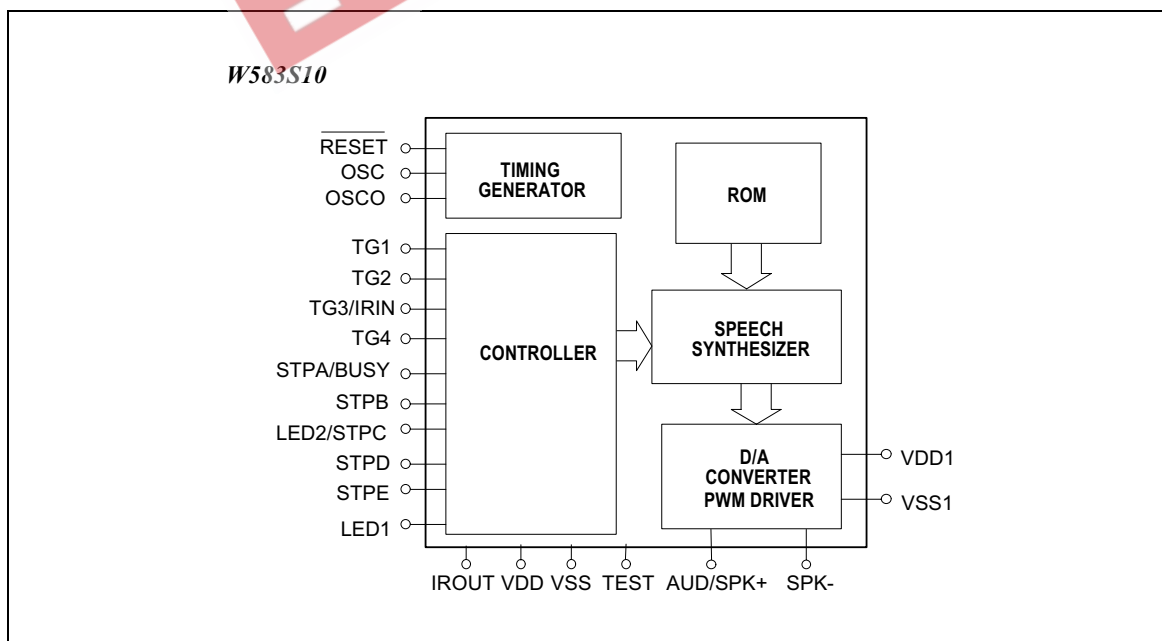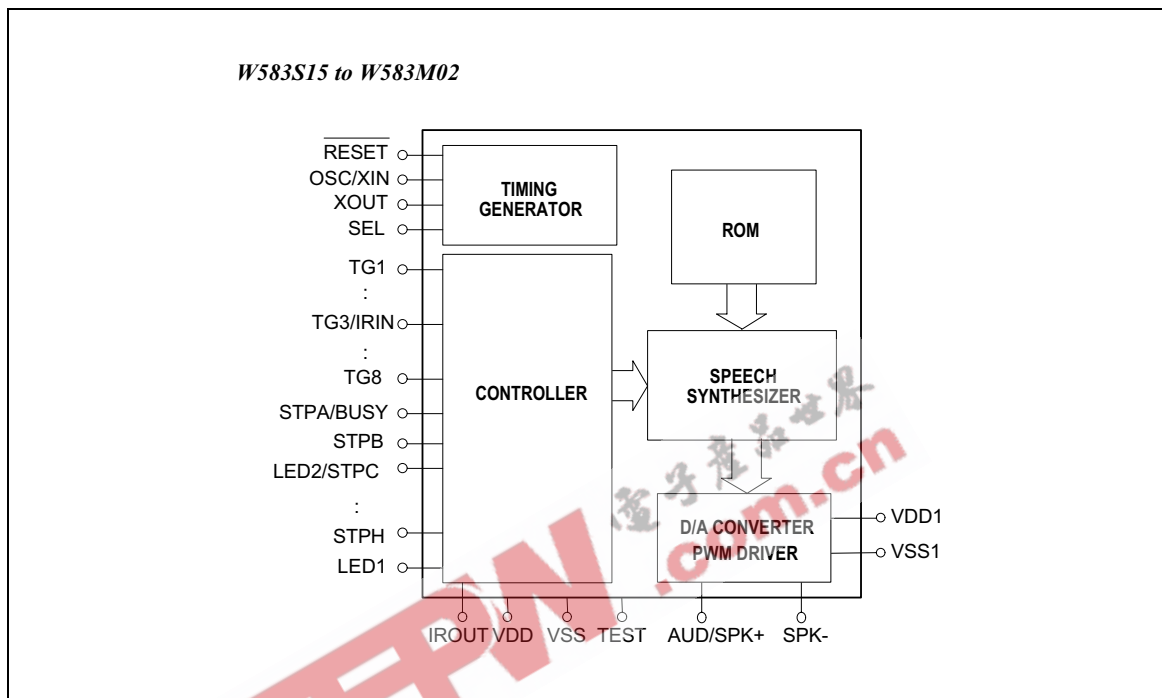
PIN DESCRIPTION

NAME	I/O	DESCRIPTION
V_{DD}	-	Positive power supply
TEST	I	Test pin, internally pulled low
$\overline{\text{RESET}}$	I	Reset all, functions as POR, internally pulled high
TG1	I	Direct trigger input 1, internally pulled high
TG2	I	Direct trigger input 2, internally pulled high
TG3/IRIN	I	Direct trigger input 3 or IR input, internally pulled high. Once this pin is pulled low, the oscillation circuit is active even the chip enters standby mode.
TG4	I	Direct trigger input 4, internally pulled high
V_{SS}	-	Negative power supply
LED1	O	LED1 output
IROUT	O	IR signal output pin, active low
STPA/BUSY	O	Stop signal A or Busy signal
STPB	O	Stop signal B
LED2/STPC	O	LED2 output or Stop signal C
STPD	O	Stop signal D
STPE	O	Stop signal E
AUD/SPK+	O	Current type output or PWM output for speaker
SPK-	O	PWM output
V_{SS1}	-	Negative power supply
V_{DD1}	-	Positive power supply

Pin Description only for W583S15 to W583M02

NAME	I/O	DESCRIPTION
OSC/XIN	I	Ring oscillator input or crystal input
XOUT	I/O	Crystal input or oscillator clock output
SEL	I	Ring/Crystal oscillator select, internally pulled high. Floating for Ring and grounded for crystal.
TG5	I	Direct trigger input 5, internally pulled high
TG6	I	Direct trigger input 6, internally pulled high
TG7	I	Direct trigger input 7, internally pulled high

Pin Description only for W583S15 to W583M02, continued

NAME	I/O	DESCRIPTION
TG8	I	Direct trigger input 8, internally pulled high
STPF	O	Stop signal F
STPG	O	Stop signal G
STPH	O	Stop signal H

Pin Description only for W583S10

NAME	I/O	DESCRIPTION
OSC	I	Ring oscillator input
OSCO	O	Oscillator clock output

FUNCTIONAL DESCRIPTION

The W583xxx is a derivative of Winbond's PowerSpeech™ synthesizers, which are becoming dominant in the consumer market, especially for toy applications.

There are up to 8 trigger inputs and 8 STOP outputs in W583xxx. The maximal number of software key pad by scanning matrix is up to $8 \times 9 = 72$ keys. There are 8 general purpose registers, R0-R7. R0-R7 can apply not only for "LD" and "JP" instructions but also for "MV" instruction. Only R0 can apply for "INC" instruction. CPU interface is the same as the W581xx series.

IR interface is a new feature of PowerSpeech™. User can use IR interface to transmit and receive a command. For example, when X chip executes the "TX R1" instruction, the Pulse Position Modulation waveform (with 38 KHz carrier) outputs from IROUT pin to drive a photo diode. Y chips within a certain distance will receive the IR signal through an IR receiver module to TG3/IRIN pin and execute a "JP" instruction to the interrupt vector/label pointed by R1 of X chip.

There are two kinds of events that can cause the W583xxx to enter the POI (Power On Initialization) process: one is power on, and the other is direct trigger from $\overline{\text{RESET}}$ pin. The interrupt vector "32" is allocated for this special event, and its priority is above all, i.e., no triggers can override the POI process if they all happen simultaneously. So the user can write a program into this interrupt vector to set the power on initial state. If the user does not wish to execute a program on power on, he should write an "END" instruction in interrupt vector "32". During the POI process, triggers can then override it successfully; if the EN0, EN1 and MODE0, MODE1 registers are set properly.

If more than two events happen simultaneously, the priority that is set by the internal H/W is: POI > TG1F > TG1R > TG2F > TG2R > TG3F > TG3R > TG4F > TG4R > TG5F > TG5R > TG6F > TG6R > TG7F > TG7R > TG8F > TG8R > "JP" instruction.

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Register Definition And Control

The register file of the W583xxx family is composed of 14 registers, including 8 general purpose registers and 6 special purpose registers.

They are defined to facilitate the operations for various purposes. The default setting values of the registers are given in the following table.

REGISTER	NAME	DEFAULT SETTING
General Register	R0-R7	00100000B
Special Register	EN0, EN1	11111111B
	MODE0, MODE1	11111111B
	STOP	11111111B
	PAGE	00000000B

Note: EN1 register and bits 5-7 of STOP register are not provided in W583S10.

1. MODE0 Register

BIT	DESCRIPTION	DEFINITION
7	LED mode	1: Flash
		0: DC
6	LED2/STPC pin selection	1: LED2 output
		0: STPC output
5	IR output source	1: Hardware control IR output
		0: STPC control IR output
4	Debounce time	1: Long
		0: Short
3, 1, 0	Reserved	-
2	STPA/BUSY pin selection	1: STPA output
		0: BUSY output

MODE0.7 controls the output type of LED1 (and LED2) pin. MODE0.6 controls the configuration of LED2/STPC pin. MODE0.5 controls the output source of IR. If hardware control IR output is selected, IR output can have signal with carrier or without carrier which is selected by MODE1.0. MODE0.4 controls the trigger pin debounce time. MODE0.2 controls the behavior of the STPA/BUSY pin which is usually used as Busy signal in CPU mode.

2. MODE1 Register

BIT	DESCRIPTION	DEFINITION	
7, 6, 1	Reserved		
5	LED Flash Type	1: Alternate	
		0: Synchronous	
4	LED1 Section Control	1: YES	
		0: NO	
3	LED2 Control	1: SECTION control	
		0: STPC control	
2	LED1 Volume Control	1: Off	
		0: On	
0	IR Output Format	1: IR output carrier with duty cycle 75%	
		0: IR output without carrier	

MODE1.5 is for LED flash type control. MODE1.4 is for LED1 section control ON/OFF. MODE1.3 is for LED2 Section/STPC control. MODE1.2 is for LED1 volume control. MODE1.0 is for IR output with or without carrier and this bit is useful only MODE0.5 is "1". For STPC control IR output (MODE0.5 is 0), the IR output always has 38 KHz carrier signal no matter what the setting of MODE1.0 is.

3. PAGE Register

BIT	7	6	5	4	3	2	1	0
PAGE	-	-	-	PG4	PG3	PG2	PG1	PG0

Bits 5-7 of PAGE register are reserved; bits 0-4 are used for page selection. The user must setup the page mode configuration described in the Option Control Function section. Once the page mode is decided, the working page is selected by the bits 0-4 of PAGE register. Hence, the user can execute "LD PAGE, value" instruction to change the working page of the voice entry group. Not all of the bits 0-4 of PAGE register are used in different page mode; they are listed below.

PAGE MODE	PG4	PG3	PG2	PG1	PG0
1-page	×	×	×	×	×
8-page	×	×	√	√	√
16-page	×	√	√	√	√
32-page	√	√	√	√	√

Where "×" means don't care and "√" means must be set properly.

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4. EN0, EN1 Registers

BIT	7	6	5	4	3	2	1	0
EN0	TG4R	TG3R	TG2R	TG1R	TG4F	TG3F	TG2F	TG1F
EN1	TG8R	TG7R	TG6R	TG5R	TG8F	TG7F	TG6F	TG5F

A "1" means "enabled", while a "0" means "disabled" for that edge of the particular TG pin. For example, the instruction "LD EN0, 0x0F" enables all the falling edge triggers of TG1-TG4, while disabling all the rising edge triggers of TG1-TG4. The user can modify the EN0 and EN1 registers during operation of the W583xxx to achieve various kinds of trigger functions, like retriggerable or not, one shot or level hold play mode, etc.

That is to say, users can change the contents of EN0, EN1 register during synthesis at will to determine which trigger pin is to be enabled or disabled for its falling/rising edge.

EN1 register is not provided in W583S10.

5. STOP Register

BIT	7	6	5	4	3	2	1	0
STOP	STH	STG	STF	STE	STD	STC	STB	STA

The STOP register is used to control the status of the STPA-STPH pins. For example STB bit, the corresponding bit 1 of the STOP register is used to drive the output buffer of STPB pin, an inverted stage, to show its logic status. Notes that bits 5-7 of STOP register are reserved in W583S10.

6. R0-R7 Registers

These eight registers function as general purpose registers. They can be used to hold interrupt vector/label. R0 is a special register which can be incremented by "INC" instruction.

Option Control Function

There are four types of option control in W583xxx. They can be determined by a declaration in the user's program file, but can not be controlled by register.

FUNCTION	MASK OPTION DECLARATION	DEFINITION
Page Mode Configuration	DEFPAGE 1	256 interrupt vector/label for 1 page, 1 page in total (1-page mode)
	DEFPAGE 8	256 interrupt vector/label for 1 page, 8 pages in total (8-page mode)
	DEFPAGE 16	128 interrupt vector/label for 1 page, 16 pages in total (16-page mode)
	DEFPAGE 32	64 interrupt vector/label for 1 page, 32 pages in total (32-page mode)
Operation Mode	NORMAL	Normal mode operation
	CPU	CPU mode operation
Oscillator Frequency	OSC_3MHz	3 MHz oscillator
	OSC_1.5MHz	1.5 MHz oscillator
Voice Output Type	VOUT_DAC	DAC (AUD) output
	VOUT_PWM	PWM output

"DEFPAGE" decides the page operation mode of W583xxx. The default setting of the page mode is 1-page mode. The 8-page, 16-page or 32-page mode must be declared in order to reach the interrupt vector/label from 256 to 2047 when the interrupt vector/label is beyond 0-255.

The W583xxx can communicate with an external microprocessor through the simple serial CPU interface, which is the same as the W581xx series. The CPU interface consists of the TG1, TG2, and STPA/BUSY pins. "NORMAL" and "CPU" decide whether the operation mode of W583xxx will be normal mode or CPU mode.

"OSC_3MHz" and "OSC_1.5MHz" select the frequency of the system clock. "VOUT_DAC" and "VOUT_PWM" select the voice output type.

Interrupt Vector Allocation

The W583xxx provides a total of 8 trigger inputs to communicate with the outside world. Each trigger pin can invoke 2 dedicate interrupt vectors depending on TG pin status. The table below show the relationship between TG pin status and interrupt vectors.

Interrupt vectors 8-15 are not allocated for TG pins in W583S10 because only TG1-TG4 pins are provided in this chip.

INTERRUPT VECTOR	TRIGGER SOURCE	INTERRUPT VECTOR	TRIGGER SOURCE
0	TG1F	8	TG5F
1	TG2F	9	TG6F
2	TG3F	10	TG7F
3	TG4F	11	TG8F
4	TG1R	12	TG5R
5	TG2R	13	TG6R
6	TG3R	14	TG7R
7	TG4R	15	TG8R
32	POI	-	-

Instruction Set

There are two types of instruction in the W583xxx, unconditional and conditional instructions. The first type of instructions are executed immediately after they are issued. The second type of instructions are executed only when the conditions specified in the instruction are satisfied. All the instructions are listed in the following table.

The cycle time for each instruction is 2/Sampling Frequency(Fs). For Fs = 6.0 KHz, the cycle time is 333 μS.

UNCONDITIONAL		CONDITIONAL		
JP	G	JP	G	@STS
JP	Rn	JP	Rn	@STS
LD	EN0, value	LD	EN0, value	@STS
* LD	EN1, value	* LD	EN1, value	@STS

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Continued

LD	MODEi, value		LD	MODEi, value	@STS
LD	STOP, value		LD	STOP, value	@STS
LD	PAGE, value		LD	PAGE, value	@STS
LD	Rn, value		LD	Rn, value	@STS
END			END		@STS
MV	Rn, Rm		MV	Rn, Rm	@STS
INC			INC		@STS
TX	Rn		TX	Rn	@STS

Legend:

G: Interrupt vector/label

Rn: R0-R7

Rm: R0-R7

MODEi: MODE0, MODE1

value: 8-bit data

@STS can be the following: @LAST, @TGn_HIGH, @TGn_LOW, n = 1–8.

　　But n = 1–4 for W583S10.

*: These instructions are not provided in W583S10.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITIONS	RATED VALUE	UNIT
Power Supply	V_{DD}–V_{SS}	-	-0.3 to +7.0	V
Input Voltage	V_{IN}	All Inputs	V_{SS} -0.3 to V_{DD} +0.3	V
Storage Temp.	T_{STG}	-	-55 to +150	°C
Operating Temp.	T_{OPR}	-	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

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ELECTRICAL CHARACTERISTICS

(T_A = 25° C, V_{SS} = 0V, V_{DD} = 4.5V unless otherwise specified.)

DC Characteristics

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V_{DD}		2.4	3	5.5	V
Input Voltage	V_{IL}		V_{SS} -0.3	-	$0.3 \times V_{DD}$	V
	V_{IH}		$0.7 \times V_{DD}$	-	V_{DD}	
Standby Current	I_{SB1}	V_{DD} = 3V, All I/O pins unconnected, No Playing			1	μA
	I_{SB2}	V_{DD} = 5V, All I/O pins unconnected, No Playing			1	μA
Operating Current (Ring type)	I_{OP1}	V_{DD} = 3V, No Load			500	μA
	I_{OP2}	V_{DD} = 5V, No Load			1	mA
Operating Current (Crystal type)	I_{OP3}	V_{DD} = 3V, No Load			600	μA
	I_{OP4}	V_{DD} = 5V, No Load			1.2	mA
Input Current of TG1-TG8 Pins	I_{IN1}	V_{DD} = 3V, Vin = 0V			-8	μA
Input Current of TEST Pin	I_{IN2}	V_{DD} = 3V, Vin = 3V			50	μA
Input Current of SEL, $\overline{RESET}$	I_{IN3}	V_{DD} = 3V, Vin = 0V			-8	μA
SPK (D/A Full Scale)	I_{DAC}	V_{DD} = 4.5V, RI = 100Ω	-4.0	-5.0	-6.0	mA
Output Current of STPA-STPH	I_{OL1}	V_{DD} = 3V, Vout = 0.4V	0.8			mA
	I_{OH1}	V_{DD} = 3V, Vout = 2.7V	-0.8			mA
Output Current of SPK+, SPK-	I_{OL2}	V_{DD} = 3V, RI = 8Ω	100			mA
	I_{OH2}		-100			mA

AC Characteristics

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillation Frequency[1]	Fosc	Ring Oscillator, Rosc = 750 KΩ	2.7	3	3.3	MHz
		Ring Oscillator, Rosc = 1.6 MΩ	1.3	1.5	1.7	
Oscillation Frequency Deviation by Voltage Drop	$\frac{\Delta Fosc}{Fosc}$	$\frac{F(3V)-F(2.4V)}{F(3V)}$			7.5	%
Instruction Cycle Time	Tins	Fosc = 3 MHz, SR = 6 KHz		1/3		mS
POI Delay Time	TPD	Fosc = 3 MHz		160		mS
Long Debounce Time	TDEBL	Fosc = 3 MHz, SR = 6 KHz	50			mS
Short Debounce Time[2]	TDEBS		400			μS

1. This parameter is different from that of W58300.

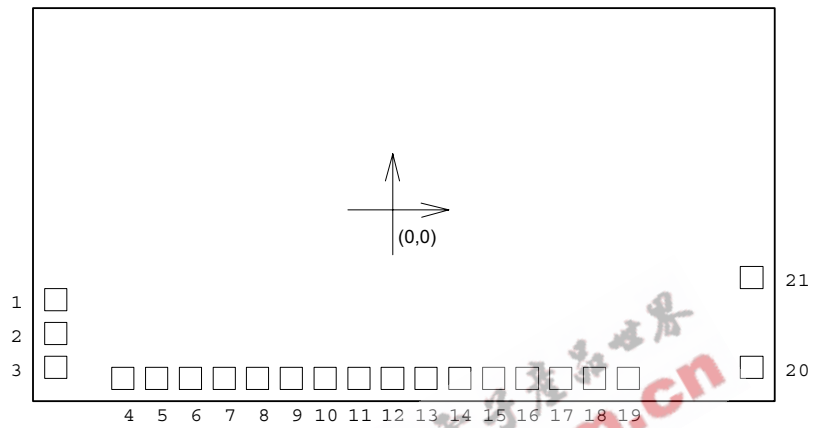2. For ring oscillator only.

TYPICAL APPLICATION CIRCUIT

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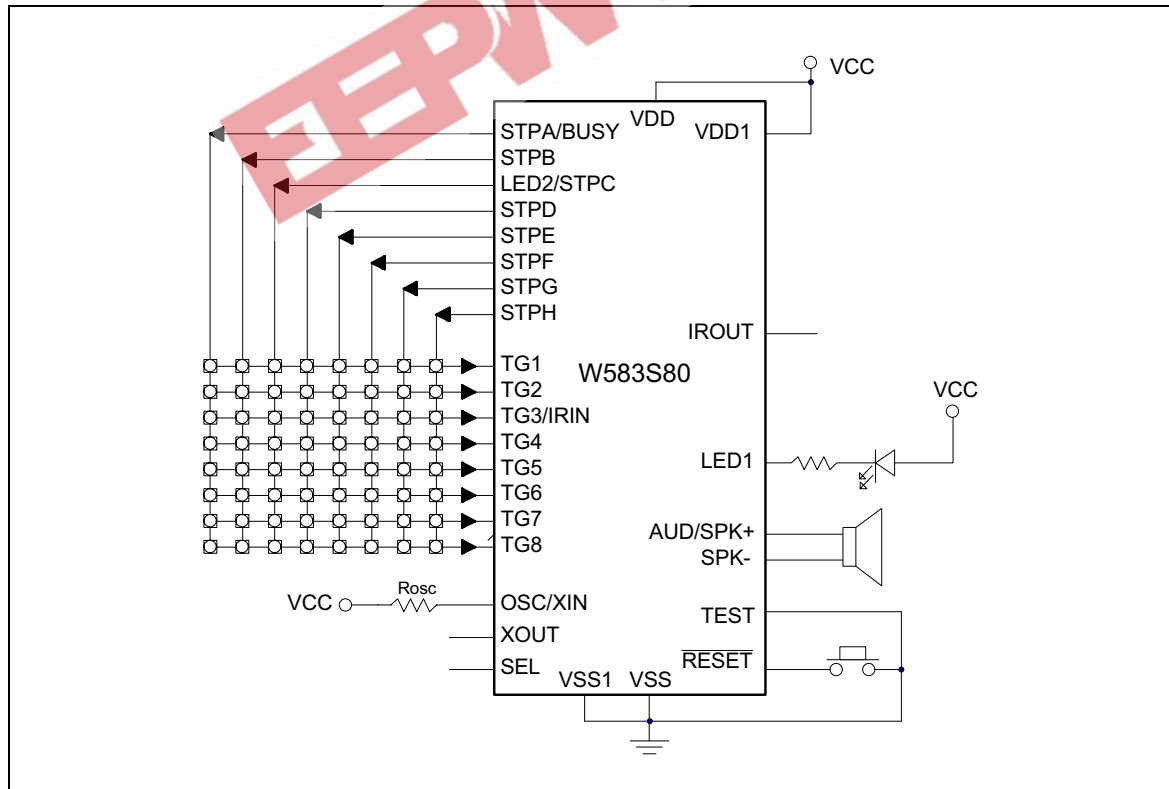
BONDING PAD DIAGRAM

(For W583S10 only)

PAD NO.	PAD NAME	PAD NO.	PAD NAME
1	V$_{DD}$	12	LED1
2	OSC	13	STPA/BUSY
3	OSCO	14	STPB
4	TEST	15	LED2/STPC
5	$\overline{RESET}$	16	STPD
6	TG1	17	STPE
7	TG2	18	V$_{SS1}$
8	TG3/IRIN	19	V$_{DD1}$
9	TG4	20	SPK-
10	V$_{SS}$	21	AUD/SPK+
11	IROUT	-	-

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(For W583S15 to W583M02)
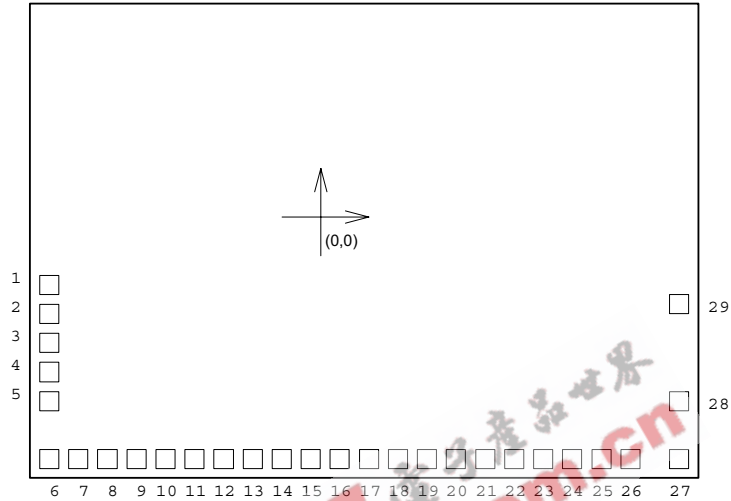
PAD NO.	PAD NAME	PAD NO.	PAD NAME
1	V_{DD}	16	IROUT
2	OSC/XIN	17	LED1
3	XOUT	18	STPA/BUSY
4	SEL	19	STPB
5	TEST	20	LED2/STPC
6	$\overline{RESET}$	21	STPD
7	TG1	22	STPE
8	TG2	23	STPF
9	TG3/IRIN	24	STPG
10	TG4	25	STPH
11	TG5	26	V_{SS1}
12	TG6	27	V_{DD1}
13	TG7	28	SPK-
14	TG8	29	AUD/SPK+
15	V_{SS}	-	-

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Note: All data and specifications are subject to change without notice.