

**W83176R-401**

**W83176G-401**

Winbond Current Mode  
Differential Buffer  
for PCI Express and SATA

Date: May,2006      Revision: 0.6

# W83176R-401, W83176G-401



## CURRENT MODE DIFFERENTIAL BUFFER FOR PCI EXPRESS AND SATA

### W83176R-401/W83176G-401 Datasheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1	n.a.	06/05/04	0.5	n.a.	All of the versions before 0.50 are for internal use.
2		05/16/06	0.6	n.a.	Add Pb-free part no : W83176G-401
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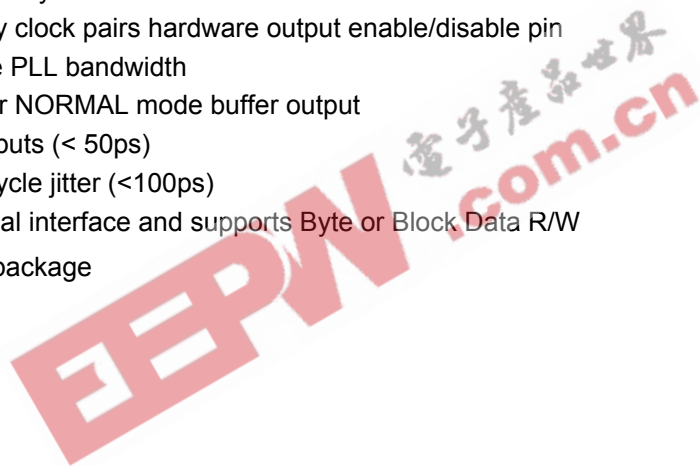
### 1. GENERAL DESCRIPTION

The W83176R-401 supports eight current mode differential Clock pair's buffer output companion devices to CK409 or CK410 clock generator.

The W83176R-401 provides I<sup>2</sup>C serial bus interface to program the registers to enable or disable each clock outputs. The W83176R-401 accepts a reference clock as its input current mode differential pair's clock.

### 2. PRODUCT FEATURES

- Eight current mode differential clock pairs clock outputs
- Support zero delay buffer mode and normal buffer mode
- Supports every clock pairs hardware output enable/disable pin
- Programmable PLL bandwidth
- Support PLL or NORMAL mode buffer output
- Low Skew outputs (< 50ps)
- Low cycle to cycle jitter (<100ps)
- I<sup>2</sup>C 2-Wire serial interface and supports Byte or Block Data R/W
- 48-pin SSOP package



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### 3. PIN CONFIGURATION

SRC_DIV #	1	48	VDDA
VDD	2	47	GND
GND	3	46	IREF
SRCT_IN	4	45	LOCK
SRCC_IN	5	44	OE_7*
OE_0*	6	43	OE_4*
OE_3*	7	42	DIFT7
DIFT0	8	41	DIFC7
DIFC0	9	40	GND
GND	10	39	VDD
VDD	11	38	DIFT6
DIFT1	12	37	DIFC6
DIFC1	13	36	OE_6*
OE_1*	14	35	OE_5*
OE_2*	15	34	DIFT5
DIFT2	16	33	DIFC5
DIFC2	17	32	GND
GND	18	31	VDD
VDD	19	30	DIFT4
DIFT3	20	29	DIFC4
DIFC3	21	28	HIGH_BW#
PLL/NORMAL#	22	27	SRC_STOP#
SCLK *	23	26	PD#
SDATA *	24	25	GND

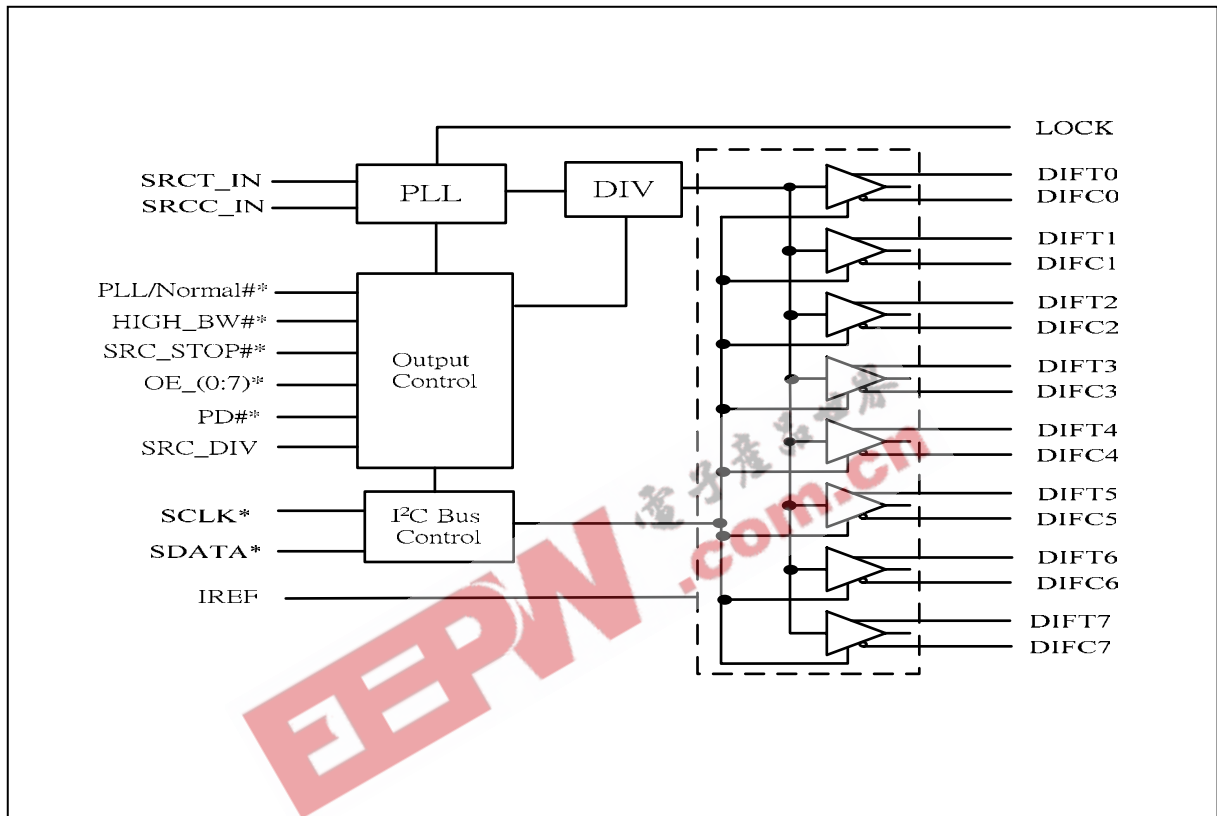
\*: Internal pull-up resistor 120K to VDD

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### 4. BLOCK DIAGRAM



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### 5. PIN DESCRIPTION

BUFFER TYPE SYMBOL	DESCRIPTION
IN	Input
OUT	Output
IN <sub>tp120k</sub>	Latched input at power up, internal 120kΩ pull up.
*	Internal 120kΩ pull-up
#	Low Active

#### 5.1 Clock Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
4,5	SRCT_IN SRCC_IN	IN	0.7V SRC Differential clock inputs.
8,9,12,13,16, 17,20,21,30, 29,34,33,38, 37,42,41	DIFT/C (0:7)	OUT	0.7V Differential clock pair outputs.
1	SRC_DIV	IN	For selecting input frequency divided by two, active low
6,14,15,7, 43,35,36,44	OE_(0:7)*	IN	DIFT/C (1:7) output control, 0=Tri-state, 1=Enable output, This is internal 120K pull up.
23	SCLK *	IN	Serial clock of I <sup>2</sup> C 2-wire control interface Internal pull-up resistor 120K to VDD
24	SDATA *	I/O	Serial data of I <sup>2</sup> C 2-wire control interface Internal pull-up resistor 120K to VDD
26	PD#*	IN	Active low to power down the device into low power state is stopped VCO and all output buffers, This is internal 120K pull up.
27	SRC_STOP#*	IN	Active low to stop differential output buffers, This is internal 120K pull up.
28	HIGH_BW#*	IN <sub>tp120k</sub>	Latched input at power up to selecting PLL Band Width 0=HIGH, 1=LOW, This is internal 120K pull up.
46	IREF	IN	Deciding the reference current for the Differential clock pairs. The pin was connected to the precision resistor tied to ground to decide the appropriate current; 475 ohm is the standard value for 0.7V differential clock output.
45	LOCK	OUT	Latched output, transitions high when PLL lock is achieved.
22	PLL/NORMAL#	IN	1= PLL mode, 0=NORMAL buffer mode.

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### 5.2 Power Pins

PIN	PIN NAME	DESCRIPTION
3,10,18,25,32,40,47	GND	Ground
2,11,19,31,39	VDD	Power Supply 3.3V
48	VDDA	Analog power supply, 3.3V

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### 6. I<sup>2</sup>C CONTROL AND STATUS REGISTERS

#### 6.1 Register 0: Control Register (Default: 07h)

BIT	NAME	PWD	DESCRIPTION
7	PD_DM	0	PD# Drive mode, 0:driven, 1:Hi-Z
6	SRC_ST_DM	0	SRC_STOP Drive mode, 0:driven, 1:Hi-Z
5	SEL_SRCDIV	0	0:control by pin, 1:control by I2C
4	SEL_NORMAL	0	0:control by pin, 1:control by I2C
3	SEL_PLLBW	0	0:control by pin, 1:control by I2C
2	PLL_BW_ADJ	1	0:High BW, 1:Low BW
1	NORMAL#/PLL	1	0:Normal buffer, 1:PLL mode
0	SRC_DIV#	1	0:Divided by 2 mode, 1:Normal (output=input)

#### 6.2 Register 1: Control Register (Default: FFh)

BIT	NAME	PWD	DESCRIPTION
7	DIF7_EN	1	0:Disabled (Hi-Z), 1:Enable
6	DIF6_EN	1	0:Disabled (Hi-Z), 1:Enable
5	DIF5_EN	1	0:Disabled (Hi-Z), 1:Enable
4	DIF4_EN	1	0:Disabled (Hi-Z), 1:Enable
3	DIF3_EN	1	0:Disabled (Hi-Z), 1:Enable
2	DIF2_EN	1	0:Disabled (Hi-Z), 1:Enable
1	DIF1_EN	1	0:Disabled (Hi-Z), 1:Enable
0	DIF0_EN	1	0:Disabled (Hi-Z), 1:Enable

#### 6.3 Register 2: Control Register (Default: 00h)

BIT	NAME	PWD	DESCRIPTION
7	DIF7STOP_EN	0	0:Free-run, 1:Stoppable
6	DIF6STOP_EN	0	0:Free-run, 1:Stoppable
5	DIF5STOP_EN	0	0:Free-run, 1:Stoppable
4	DIF4STOP_EN	0	0:Free-run, 1:Stoppable
3	DIF3STOP_EN	0	0:Free-run, 1:Stoppable
2	DIF2STOP_EN	0	0:Free-run, 1:Stoppable
1	DIF1STOP_EN	0	0:Free-run, 1:Stoppable
0	DIF0STOP_EN	0	0:Free-run, 1:Stoppable

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### 6.4 Register 3: Reserved Register (Default: 00h)

BIT	NAME	PWD	DESCRIPTION
7	Reserved	0	Reserved
6	Reserved	0	Reserved
5	Reserved	0	Reserved
4	Reserved	0	Reserved
3	Reserved	0	Reserved
2	Reserved	0	Reserved
1	Reserved	0	Reserved
0	Reserved	0	Reserved

### 6.5 Register 4: Winbond Chip ID – Project Code Register (Default: 11h)

BIT	NAME	PWD	DESCRIPTION
7	CHPI_ID [7]	0	Winbond Chip ID. W83176R-401 (SA5911).
6	CHPI_ID [6]	0	Winbond Chip ID.
5	CHPI_ID [5]	0	Winbond Chip ID.
4	CHPI_ID [4]	1	Winbond Chip ID.
3	CHPI_ID [3]	0	Winbond Chip ID.
2	CHPI_ID [2]	0	Winbond Chip ID.
1	CHPI_ID [1]	0	Winbond Chip ID.
0	CHPI_ID [0]	1	Winbond Chip ID.

### 6.6 Register 5: Test Register (Default: 00h)

BIT	NAME	PWD	DESCRIPTION
7	TEST1	0	Reserved
6	TEST0	0	Reserved
5	Reserved	0	Reserved
4	Reserved	0	Reserved
3	Reserved	0	Reserved
2	Reserved	0	Reserved
1	Reserved	0	Reserved
0	Reserved	0	Reserved

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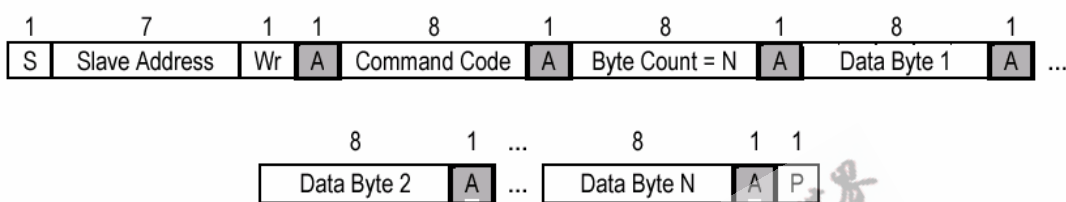


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### 7. ACCESS INTERFACE

The W83176R-401 provides I<sup>2</sup>C Serial Bus for microprocessor to read/write internal registers. In the W83176R-401 is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I<sup>2</sup>C write address is defined at 0xDC. The I<sup>2</sup>C read address is defined at 0xDD.

#### 7.1 Block Write protocol

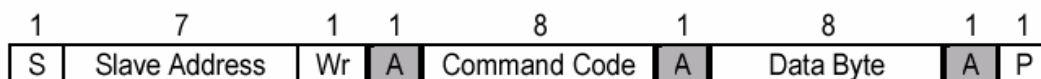


#### 7.2 Block Read protocol

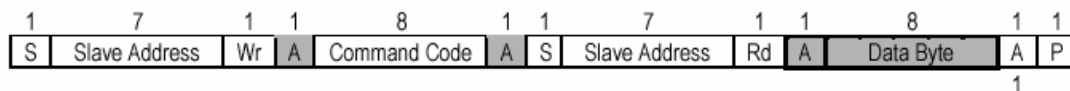


## In block mode, the command code must filled '00h'

#### 7.3 Byte Write protocol



#### 7.4 Byte Read protocol



## In Byte Mode, the index No= (Register No) + 1

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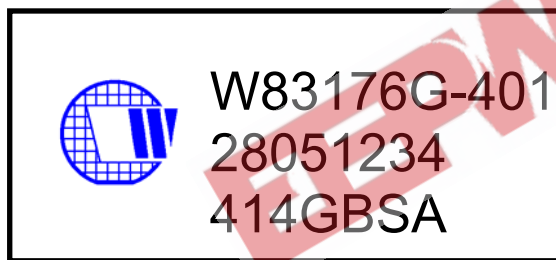
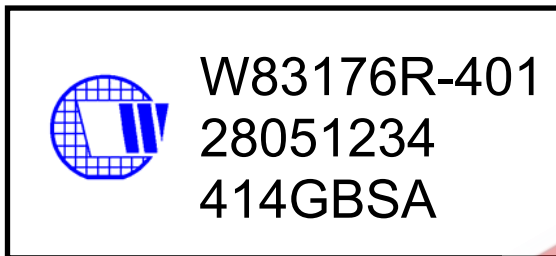


## CURRENT MODE DIFFERENTIAL BUFFER FOR PCI EXPRESS AND SATA

### 8. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83176R-401	48 PIN SSOP	Commercial, 0°C to +70°C
W83176G-401	48 PIN SSOP (Pb-free package)	Commercial, 0°C to +70°C

### 9. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83176R-401, W83176G-401(Pb-free part no)

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 414 G B SA

414: packages made in '2004, week 14

G: assembly house ID; O means OSE, G means GR

B: IC revision

SA: For internal use

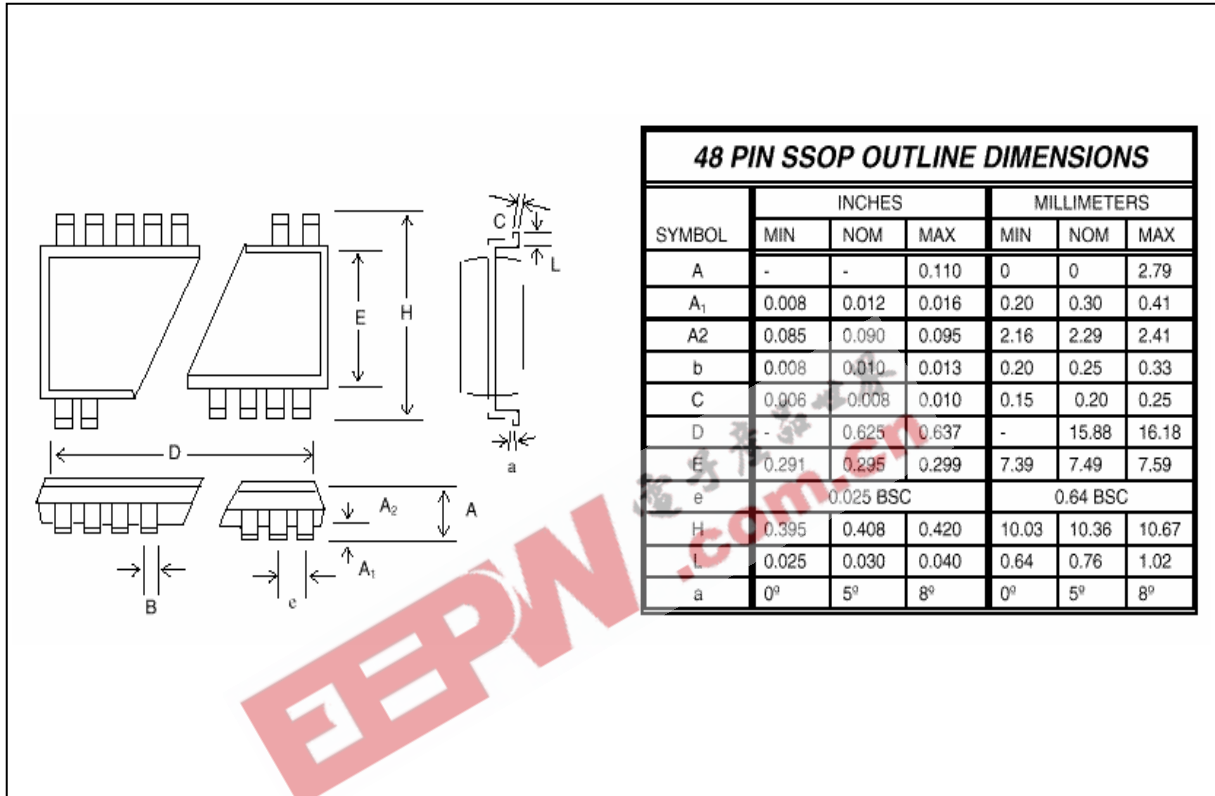
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## CURRENT MODE DIFFERENTIAL BUFFER FOR PCI EXPRESS AND SATA

### 10. PACKAGE DRAWING AND DIMENSIONS



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