W83176R-732
Data Sheet

WINBOND
2 DIMM DDR ZERO DELAY BUFFER FOR SIS CHIPSET

Publication Release Date: April 13, 2005
Revision 1.1

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1. GENERAL DESCRIPTION

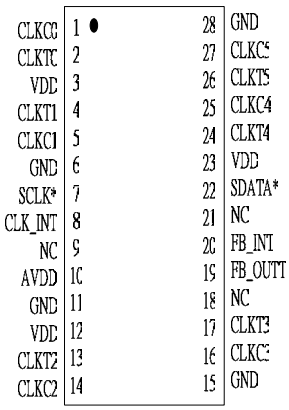
The W83176R-732 is a 2.5V Zero-delay D.D.R. Clock buffer designed for SiS chipset. W83176R-732 can support 2 D.D.R. DRAM DIMMs.

The W83176R-732 provides I^2C serial bus interface to program the registers to enable or disable each clock outputs. The W83176R-732 accepts a reference clock as its input and runs on 2.5V supply.

2. FEATURES

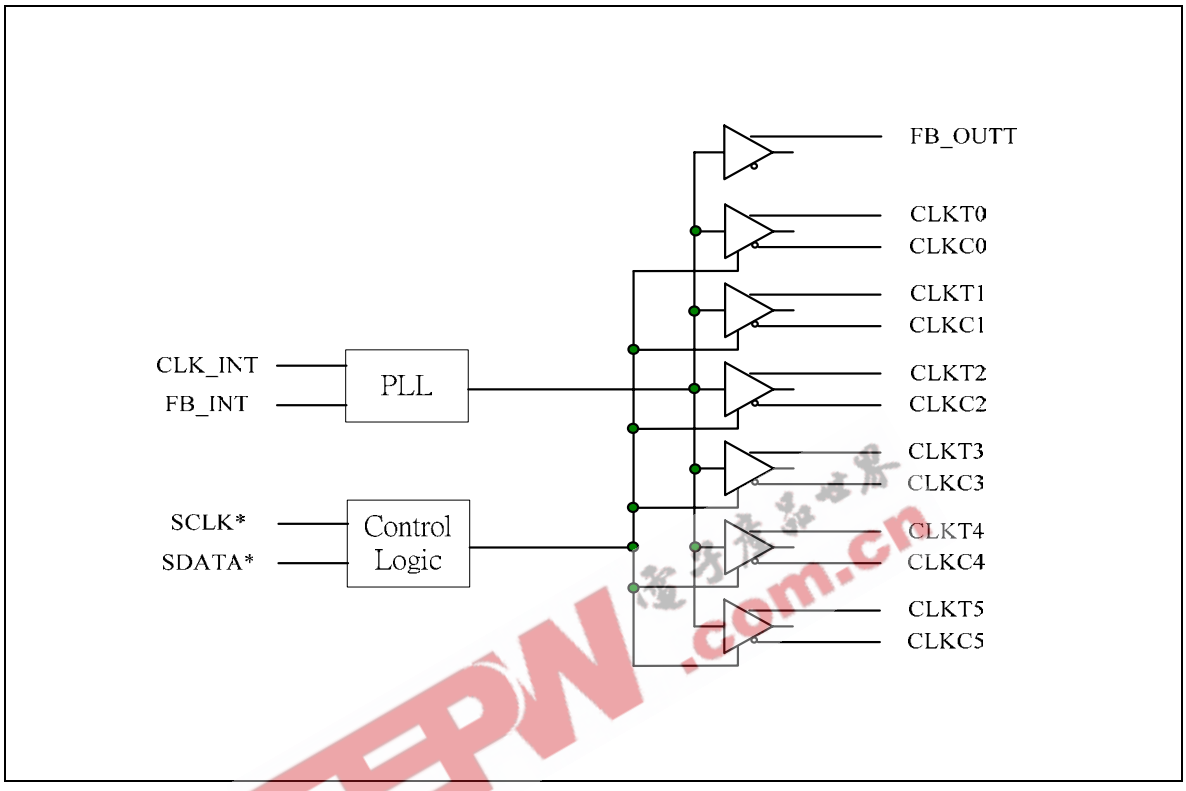
- Zero-delay clock outputs
- Feedback pins for synchronous
- Supports up to 2 D.D.R. DIMMs
- One pairs of additional outputs for feedback
- Low Skew outputs (< 100 pS)
- Supports 400 MHz D.D.R. SDRAM
- ^2C 2-Wire serial interface and supports Byte or Block Date RW
- Packaged in 28-pin SSOP

3. PIN CONFIGURATION



*: Internal pull-up resistor 120K to VDD

4. BLOCK DIAGRAM



5. PIN DESCRIPTION

BUFFER TYPE SYMBOL	DESCRIPTION
IN	Input
OUT	Output
I/O	Bi-directional Pin
*	Internal 120KΩ pull-up
NC	Not connect

5.1 Clock Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
27, 25, 16, 14, 5, 1	CLKC [5:0]	OUT	Complementary Clocks of differential pair outputs
26, 24, 17, 13, 4, 2	CLKT [5:0]	OUT	True Clocks of differential pair outputs
22	SDATA *	I/O	Serial data of I^2C 2-wire control interface Internal pull-up resistor 120K to VDD
7	SCLK *	IN	Serial clock of I^2C 2-wire control interface Internal pull-up resistor 120K to VDD
8	CLK_INT	IN	True reference clock input, 3.3V tolerant input
9, 18, 21	N/C	NC	Not connected
19	FB_OUTT	OUT	True Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT.
20	FB_INT	IN	True Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error.

5.2 Power Pins

PIN	PIN NAME	DESCRIPTION
6, 11, 15, 28	GND	Ground
3, 12, 23	VDD	Power supply 2.5V
10	AVDD	Analog power supply, 2.5V

6. REGISTER 0 ~ REGISTER 4 RESERVED

6.1 Register 5: Output Control (1 = Active, 0 = Inactive) (Default = FFh)

BIT	@POWERUP	PIN	DESCRIPTION
7	1	1, 2	CLKC0, CLKT0 (Active/Inactive)
6	1	5, 4	CLKC1, CLKT1 (Active/Inactive)
5	1	-	Reserved
4	1	-	Reserved
3	1	14, 13	CLKC2, CLKT2 (Active/Inactive)
2	1	16, 17	CLKC3, CLKT3 (Active/Inactive)
1	1	-	Reserved
0	1	-	Reserved

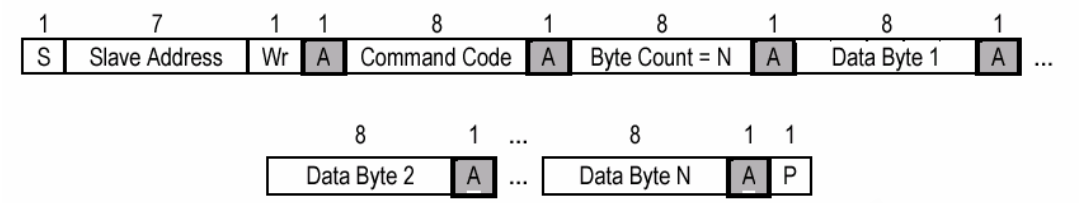
6.2 Register 6: Output Control (1 = active, 0 = inactive) (Default = FFh)

BIT	@POWERUP	PIN	DESCRIPTION
7	1	-	Reserved
6	1	-	Reserved
5	1	-	Reserved
4	1	-	Reserved
3	1	25, 24	CLKC4, CLKT4 (Active/Inactive)
2	1	-	Reserved
1	1	27, 26	CLKC5, CLKT5 (Active/Inactive)
0	1	-	Reserved

7. ACCESS INTERFACE

The W83176R-732 provides I^{2}C Serial Bus for microprocessor to read/write internal registers. In the W83176R-732 is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I^{2}C write address is defined at 0xD4. The I^{2}C read address is defined at 0xD5.

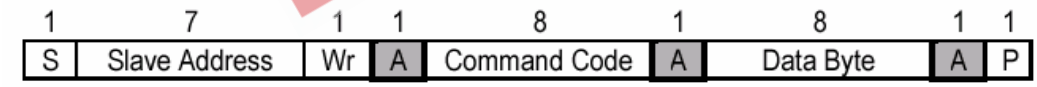
7.1 Block Write Protocol



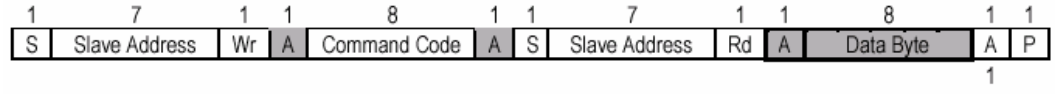
7.2 Block Read Protocol

In block mode, the command code must filled '00h'

7.3 Byte Write Protocol



7.4 Byte Read Protocol



8. SPECIFICATIONS

8.1 Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD).

SYMBOL	PARAMETER	RATING
VDD, AVDD	Voltage on any pin with respect to GND	-0.5V to +3.6V
T_{STG}	Storage Temperature	-65°C to +150°C
T_B	Ambient Temperature	-55°C to +125°C
T_A	Operating Temperature	0°C to +70°C

8.2 A.C. Characteristics

VDD = AVDD = 2.5V ±5 %, T_A = 0°C to +70°C, Test load = 10 pF

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Operating Clock Frequency	F_{IN}	100		200	MHz	
Input Clock Duty Cycle	Dtin	40		60	%	
Dynamic Supply Current	Idd			300	mA	Fin = 100 to 200 MHz
Cycle to Cycle Jitter	C-Cjitter			200	pS	Fout = 100 to 200 MHz
Output to Output Skew	Tskew			100	pS	Fout = 100 to 200 MHz
Output Clock Rise Time	Tor	650		950	pS	Fout = 100 to 200 MHz
Output Clock Fall Time	Tof	650		950	pS	Fout = 100 to 200 MHz
Output Clock Duty Cycle	Dtot	45		55	%	Fout = 100 to 200 MHz
Output Differential-pair Crossing Voltage	Voc	(VDD/2) -0.2	VDD/ 2	(VDD/2) + 0.2	V	Fout = 100 to 200 MHz

8.3 D.C. Characteristics

VDD = AVDD= 2.5V ±5 %, T_A = 0°C to +70°C

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
SDATA, SCLK Input Low Voltage	SV_{IL}			1.0	V_{dc}	
SDATA, SCLK Input High Voltage	SV_{IH}	2.2			V_{dc}	

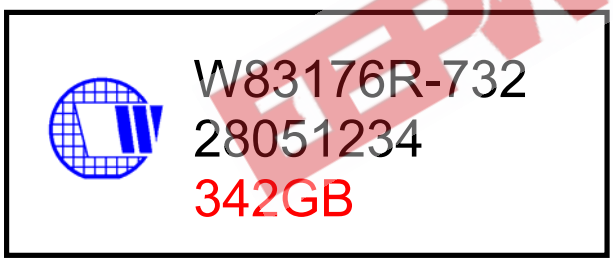
D.C. Characteristics, continued.

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
CLKIN, FBIN Input Voltage Low	V_{IL}			0.4	V_{dc}	Fin = 100 to 200 MHz
CLKIN, FBIN Input Voltage High	V_{IH}	2.1			V_{dc}	Fin = 100 to 200 MHz
Input Pin Capacitance	C_{IN}			5	pF	
Output Pin Capacitance	C_{OUT}			6	pF	
Input Pin Inductance	L_{IN}			7	nH	

9. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83176R_732	28-pin SSOP	Commercial, 0°C to +70°C

10. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83176R-732

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 342 G B

342: packages made in '2003, week 42

G: assembly house ID; O means OSE, G means GR

B: IC revision

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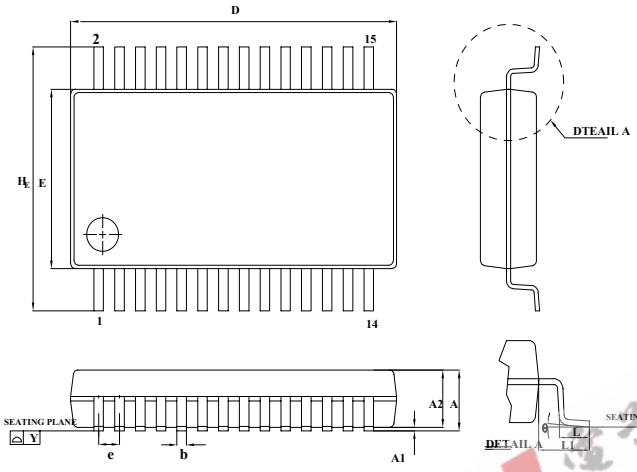
11. PACKAGE DRAWING AND DIMENSIONS

28-pin 209 mil



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	—	—	2.00	—	—	0.079
A1	0.05	—	—	0.002	—	—
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	—	0.38	0.009	—	0.015
c	0.09	—	0.25	0.004	—	0.010
D	9.90	10.20	10.50	0.389	0.401	0.413
E	5.00	5.30	5.60	0.197	0.209	0.220
H_E	7.40	7.80	8.20	0.291	0.307	0.323
e	—	0.65	—	—	0.0256	—
L	0.55	0.75	0.95	0.021	0.030	0.037
L1	—	1.25	—	—	0.050	—
Y	—	—	0.10	—	—	0.004
θ	0	—	8	0	—	8

12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
			All of the versions before 0.50 are for internal use.
0.5	12/18/03	n.a.	First published preliminary version
1.0	05/06/04		Update on web
1.1	04/13/2005	9	Add disclaimer

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