16MB (4x512Kx72) SYNC BURST-PIPELINE, DUAL KEY DIMM

FEATURES

- 4x512Kx72 Synchronous, Synchronous Burst
- Pipeline Architecture; Single Cycle Deselect
- Linear and Sequential Burst Support via MODE pin
- Clock Controlled Registered Module Enable (EM#)
- Clock Controlled Registered Bank Enables (E_1#, E_2#, E_3#, E_4#)
- Clock Controlled Byte Write Mode Enable (BWE#)
- Clock Controlled Byte Write Enables (BW_1# - BW_8#)
- Clock Controlled Registered Address
- Clock Controlled Registered Global Write (GW#)
- Asynchronous Output Enable (G#)
- Internally Self-Timed Write
- Individual Bank Sleep Mode Enables (ZZ_1, ZZ_2, ZZ_3, ZZ_4)
- Gold Lead Finish
- 3.3V ± 10% Operation
- Frequency(s): 200, 166, 150, and 133MHz
- Access Speed(s): t_{KHQV} = 3.0, 3.5, 3.7, and 4.0ns
- Common Data I/O
- High Capacitance (30pF) Drive, at Rated Access Speed
- Single Total Array Clock
- Multiple V_{CC} and G_{ND} for Improved Noise Immunity

DESCRIPTION

The WED2DG472512V is a Synchronous/Synchronous Burst SRAM, 84 position Dual Key; Double High DIMM (168 contacts) Module, organized as 4x512Kx72. The Module contains sixteeen (16) Synchronous Burst RAM devices, packaged in the industry standard JEDEC 14mmx20mm TQFP placed on a Multilayer FR4 Substrate. The Module Architecture is defined as a Sync/SyncBurst, Pipeline, with support for either linear or sequential burst. This Module provides high performance, 3-1-1-1 accesses when used in Burst Mode, and when used in Synchronous Only Mode, provides a high performance, data access every second cycle.

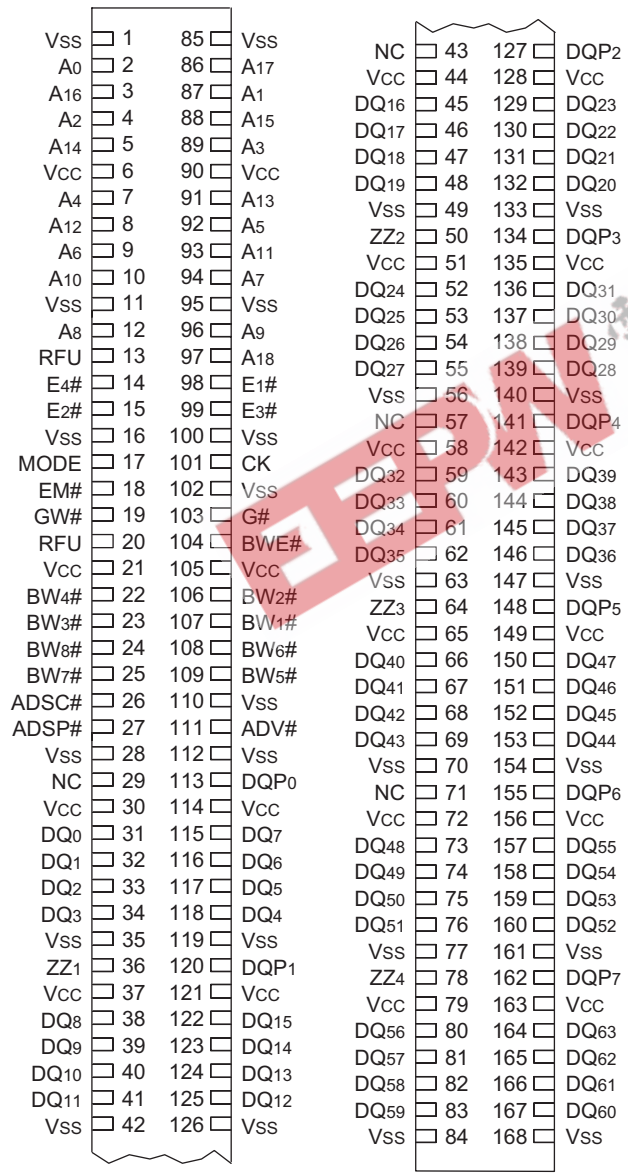
Synchronous Only operations are performed via strapping ADSC# Low, and ADSP#/ADV# High, which provides for Ultra Fast Accesses in Read Mode while providing for internally self-timed Early Writes.

Synchronous/Synchronous Burst operations are in relation to an externally supplied clock, Registered Address, Registered Global Write, Registered Enables as well as an Asynchronous Output Enable. This Module has been defined with full flexibility, which allows individual control of each of the eight bytes, as well as Quad Words in both Read and Write Operations.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

FIG. 1 PIN CONFIGURATION

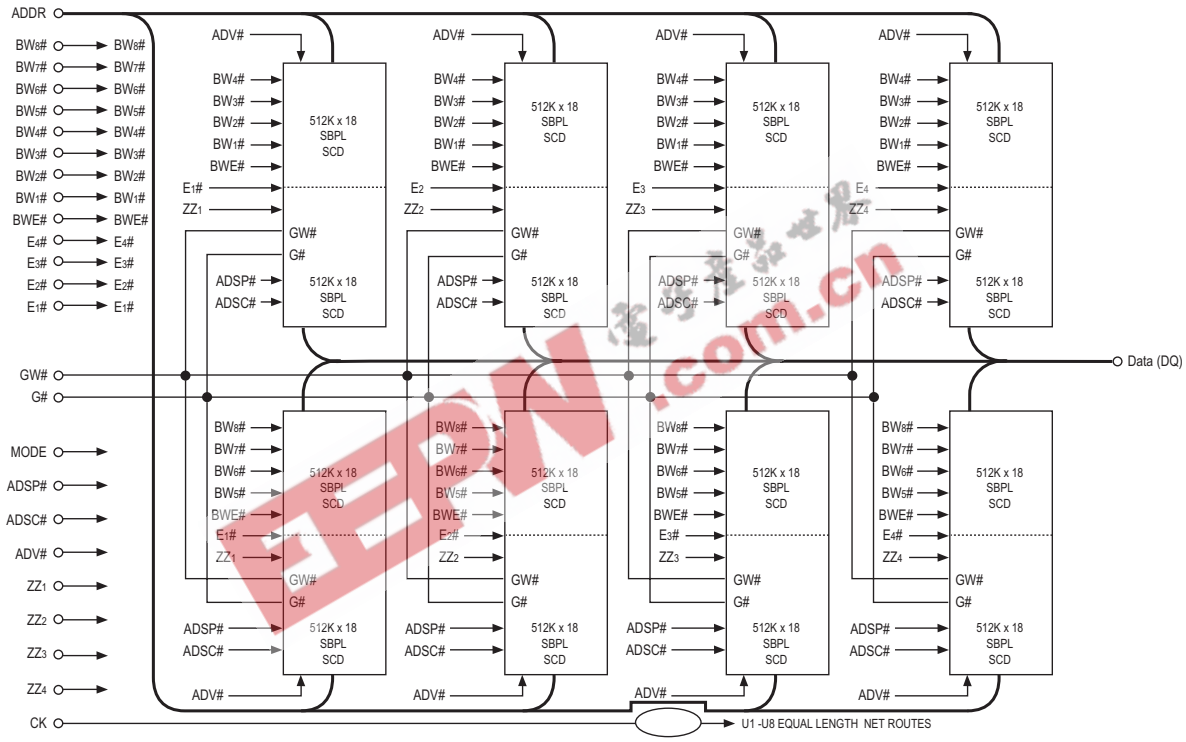
PIN IDENTIFIER



PIN DESCRIPTION

DQ_0 - DQ_{63}	Input/Output Bus
DQP_0 - DQP_7	Parity Bits
A_0 - A_{18}	Address Bus
EM#	Module Enable
E_1#, E_2#, E_3#, E_4#	Synchronous Bank Enables
BWE#	Byte Write Mode Enable
BW_1# - BW_8#	Byte Write Enables
CK	Array Clock
GW#	Synchronous Global Write Enable
G#	Asynchronous Output Enable
ZZ_1, ZZ_2, ZZ_3, ZZ_4	Bank Sleep Mode Enables
Vcc	3.3V Power Supply
Vss	Gnd

FIG. 2 FUNCTIONAL BLOCK DIAGRAM



SYNC BURST – TRUTH TABLE

Operation	E_1#	E_2#	E_3#	E_4#	ADSP#	ADSC#	ADV#	GW#	G#	CK	DQ	Addr. Used
Deselected Cycle, Power Down; Bank 1	H	X			X	L	X	X	X	L-H	High-Z	None
Deselected Cycle, Power Down; Bank 2	X	H			X	L	X	X	X	L-H	High-Z	None
Read Cycle, Begin Burst; Bank 1	L	H			L	X	X	X	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	H			L	X	X	X	H	L-H	High-Z	External
Read Cycle, Begin Burst, Bank 2	H	L			L	X	X	X	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	H	L			L	X	X	X	H	L-H	High-Z	External
Write Cycle, Begin Burst; Bank 1	L	H			H	L	X	L	X	L-H	D	External
Write Cycle, Begin Burst; Bank 2	H	L			H	L	X	L	X	L-H	D	External
Read Cycle, Begin Burst; Bank 1	L	H			H	L	X	H	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	H			H	L	X	H	H	L-H	High-Z	External
Read Cycle, Begin Burst; Bank 2	H	L			H	L	X	H	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	H	L			H	L	X	H	H	L-H	High-Z	External
Read Cycle, Continue Burst; Bank 1	X	H			X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	X	H			X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	H	X			X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	H	X			X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 1	H	H			X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	H	H			X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	H	H			X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	H	H			X	H	L	H	H	L-H	High-Z	Next
Write Cycle, Continue Burst; Bank 1	X	H			H	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 1	H	H			X	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	H	X			H	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	H	H			X	H	L	L	X	L-H	D	Next
Read Cycle, Suspend Burst; Bank 1	X	H			H	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	X	H			H	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	H	X			H	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	H	X			H	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 1	H	H			X	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	H	H			X	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	H	H			X	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	H	H			X	H	H	H	H	L-H	High-Z	Current
Write Cycle, Suspend Burst; Bank 1	X	H			H	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 1	H	H			X	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	H	X			H	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	H	H			X	H	H	L	X	L-H	D	Current

Note A: All truth Table Functions Repeat for Bank 3 (E_3#) and Bank 4 (E_4#).

SYNCHRONOUS ONLY – TRUTH TABLE

Operation	E_1#	E_2#	E_3#	E_4#	GW#	G#	ZZ	CK	DQ
Synchronous Write - Bank 1	L	H	H	H	L	H	L	↑	High-Z
Synchronous Read - Bank 1	L	H	H	H	H	L	L	↑	
Synchronous Write - Bank 2	H	L	H	H	L	H	L	↑	High-Z
Synchronous Read - Bank 2	H	L	H	H	H	L	L	↑	
Synchronous Write - Bank 3	H	H	L	H	L	H	L	↑	High-Z
Synchronous Read - Bank 3	H	H	L	H	H	L	L	↑	
Synchronous Write - Bank 4	H	H	H	L	L	H	L	↑	High-Z
Synchronous Read - Bank 4	H	H	H	L	H	L	L	↑	
Snooze Mode	X	X	X	X	X	X	H	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Relative to V_{SS}	-0.3V to +4.6V
V_{IN}	-0.3V to V_{CC} +0.5V
Storage Temperature	-55°C to + 125°C
Operating Temperature (Commercial)	0°C to +70°C
Operating Temperature (Industrial)	-40°C to +85°C
Short Circuit Output Current	100mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

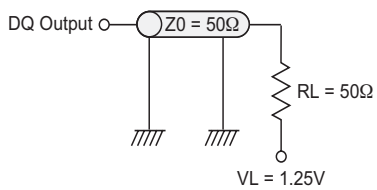
RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	3.3	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V
Input High	V_{IH}	2.0	3.0	V_{CC}+0.3	V
Input Low	V_{IL}	-0.3	0	0.3	V
Input Leakage	I_{LI}	-2	1	2	mA
Output Leakage	I_{LO}	-2	1	2	mA

DC ELECTRICAL CHARACTERISTICS READ CYCLE

Description	Sym	Typ	Max 5.0	Max 6.0	Max 6.5	Max 7.0	Units
Power Supply Current	$I_{CC}1$	1.9	2.7	2.5	2.4	2.3	A
Power Supply Current Device Selected, No Operation	I_{CC}	875	1.8	1.8	1.3	1.3	A
Snooze Mode	$I_{CC}ZZ$	270	350	350	350	350	mA
CMOS Standby	$I_{CC}3$	500	700	700	700	700	mA
Clock Running-Deselect	$I_{CC}K$	900	1.1	1.1	1.0	1.0	A

AC TEST LOAD



Output Test Equivalencies

AC TEST CONDITIONS

Input Pulse Levels	Vss to 3.0V
Input and Output Timing Ref.	1.25V
Output Test Equivalencies	See figure at left

SYNC-BURST READ CYCLE PARAMETERS

Description	Sym	3.0ns		3.5ns		3.7ns		4.0ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Frequency	f_{MAX}		200		166		150		133	MHz
Clock Cycle Time	t_{KC}	5.0		6.0		6.5		7.0		ns
Clock High Time	t_{KH}	2		2.4		2.5		3		ns
Clock Low Time	t_{KL}	2		2.4				3		ns
Clock to Output Valid	t_{KQ}		3		3.5		3.7		4	ns
Clock to Output Invalid	t_{KQX}	1.25		1.25		1.25		1.25		ns
Clock to Output Low-Z	t_{KQLZ}	0		0		0		0		ns
Output Enable to Output Valid	t_{OEQ}	1.25	3	1.25	4	1.25	4	1.25	5	ns
Output Enable to Output Low-Z	t_{OELZ}	0		0		0		0		ns
Output Enable to Output High-Z	t_{OEHZ}		2.5		3.5		3.5		4	ns
Address Setup	t_S	1.5		1.5		1.8		2.0		ns
Bank Enable Setup	t_S	1.5		1.5		1.8		2.0		ns
Address Hold	t_H	0.5		0.5		0.5		0.5		ns
Bank Enable Hold	t_H	0.5		0.5		0.5		0.5		ns

SYNC-BURST WRITE CYCLE PARAMETERS

Description	Sym	3.0ns		3.5ns		3.7ns		4.0ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Frequency	f_{MAX}		200		166		150		133	MHz
Clock Cycle Time	t_{KC}	5.0		6.0		6.5		7.0		ns
Clock High Time	t_{KH}	2		2.4		2.7		3		ns
Clock Low Time	t_{KL}	2		2.4		2.7		3		ns
Address Setup	t_S	1.5		1.5		1.8		2.0		ns
Address Hold	t_H	0.5		0.5		0.5		0.5		ns
Bank Enable Setup	t_S	1.5		1.5		1.8		1.8		ns
Bank Enable Hold	t_H	0.5		0.5		0.5		0.5		ns
Global Write Enable Setup	t_S	1.5		1.5		1.8		2.0		ns
Global Write Enable Hold	t_H	0.5		0.5		0.5		0.5		ns
Data Setup	t_S	1.5		1.5		1.8		2.0		ns
Data Hold	t_H	0.5		0.5		0.5		0.5		ns

FIG. 3 SYNC-BURST READ CYCLE

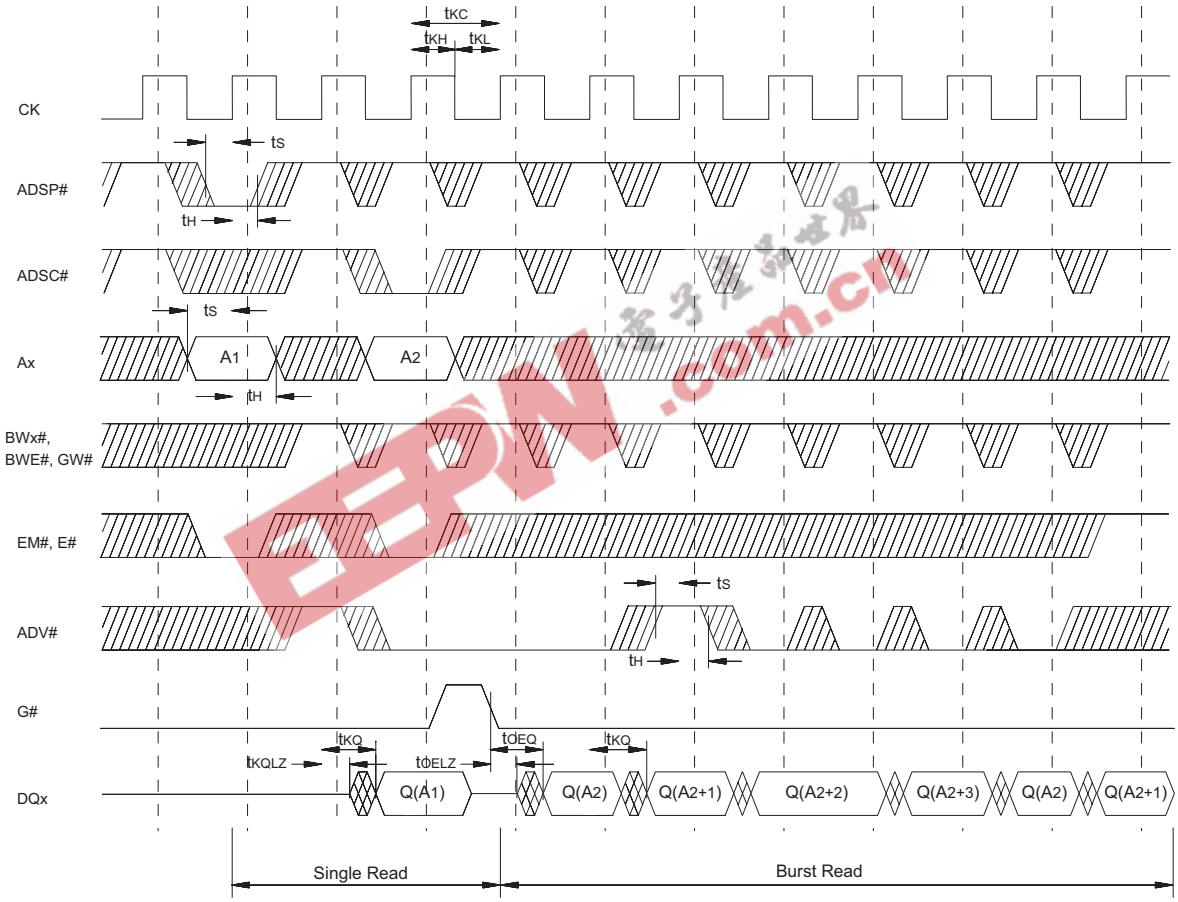


FIG. 4 **SYNC-BURST WRITE CYCLE**

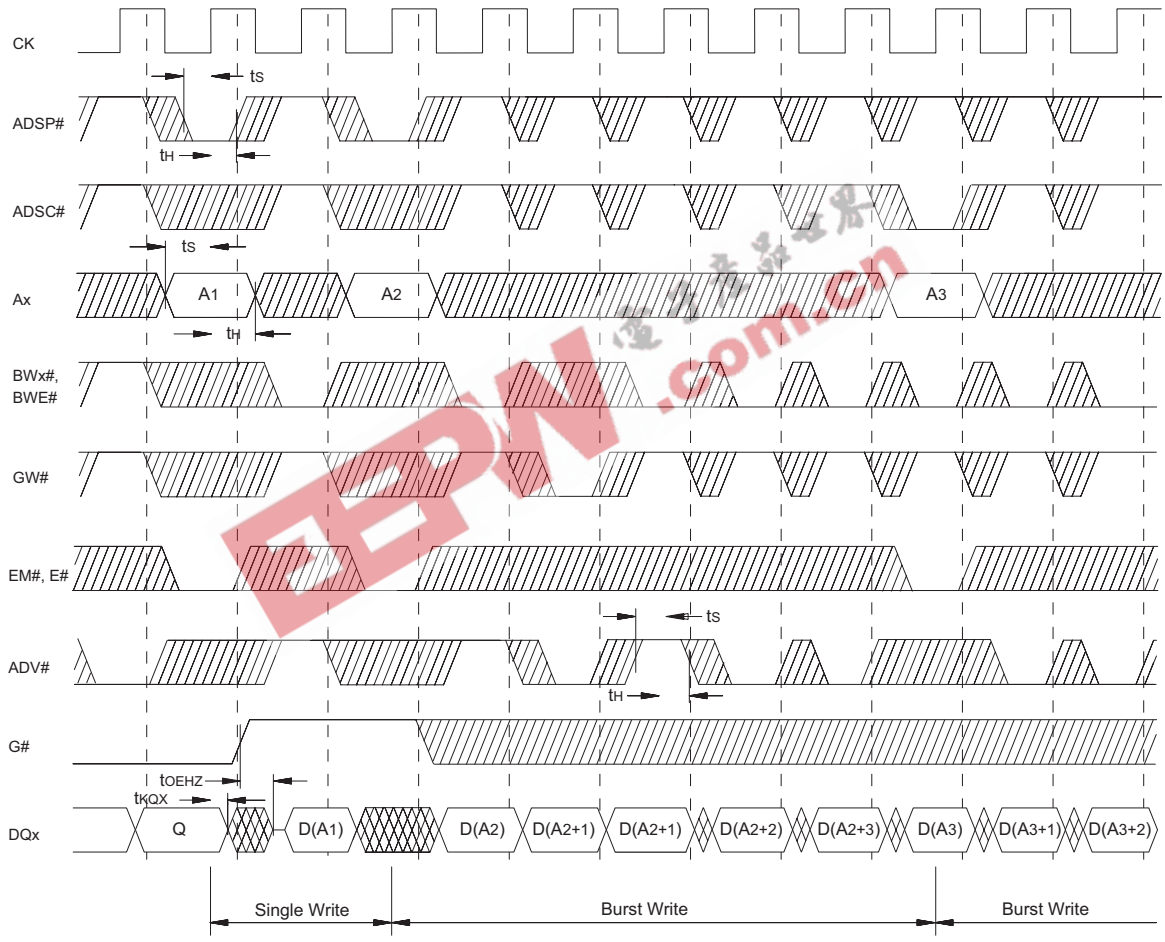
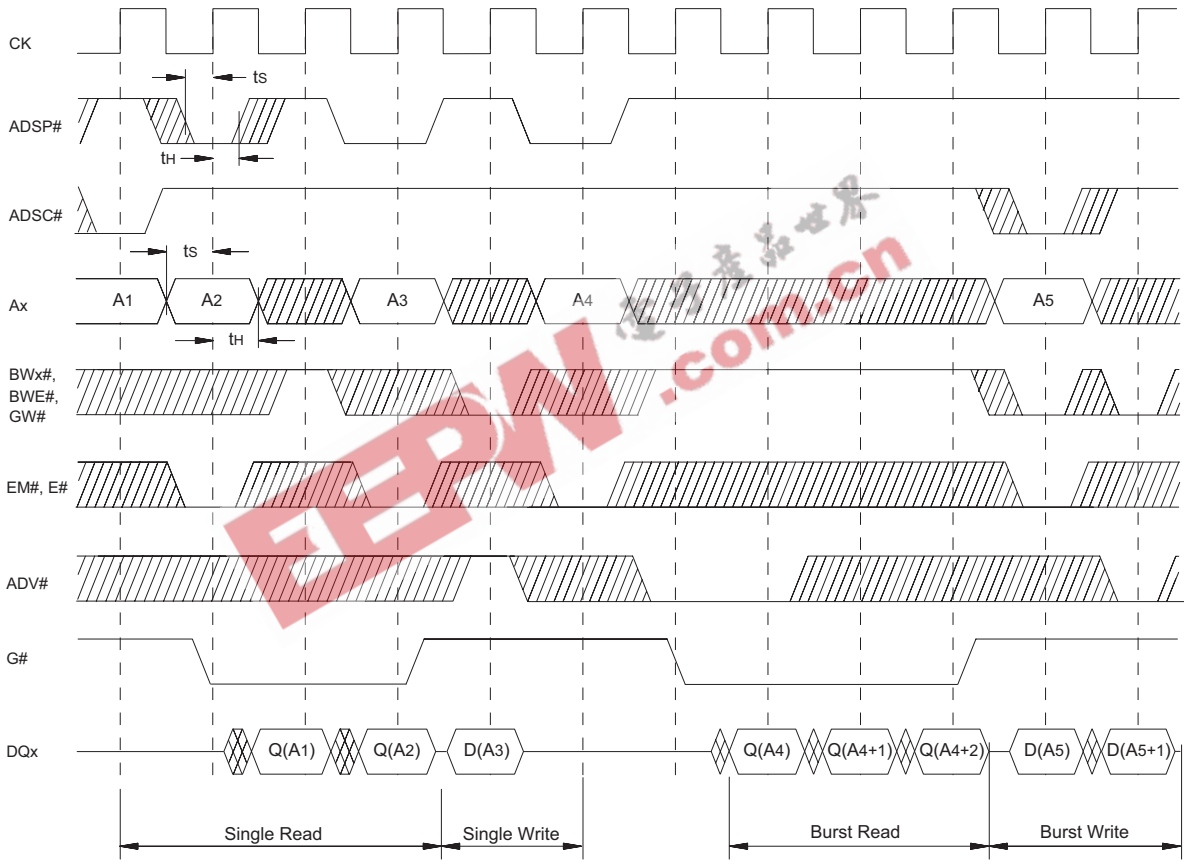
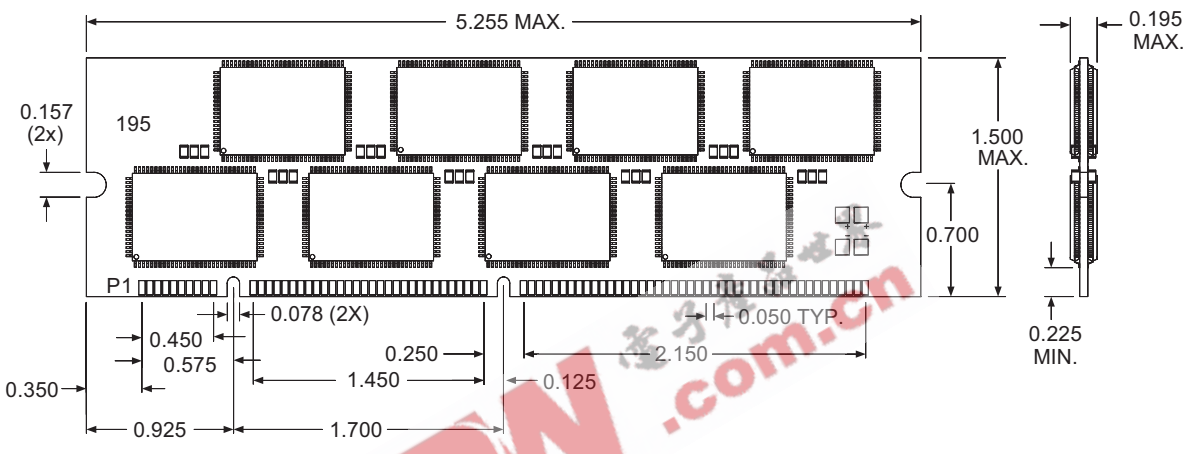


FIG. 5 **SYNC-BURST READ/WRITE CYCLE**



PACKAGE DIMENSIONS: 168 DUAL KEY DIMM



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

Part Number	Configuration	Description	Voltage (V)	Frequency	Package
WED2DG472512V5D2	16 MB (4 x 512K x 72)	Sync-Burst Pipeline	3.3V	200MHz	168 Dual Key DIMM
WED2DG472512V6D2	16 MB (4 x 512K x 72)	Sync-Burst Pipeline	3.3V	166MHz	168 Dual Key DIMM
WED2DG472512V65D2	16 MB (4 x 512K x 72)	Sync-Burst Pipeline	3.3V	150MHz	168 Dual Key DIMM
WED2DG472512V7D2	16 MB (4 x 512K x 72)	Sync-Burst Pipeline	3.3V	133MHz	168 Dual Key DIMM