Winbond Electronics Corp.

STEP-LESS CLOCK FOR SIS CHIPSET

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1. GENERAL DESCRIPTION

The W83194BR-63S is a Clock Synthesizer which provides all clocks required for high-speed RISC or CISC microprocessor such as Intel Pentium II or Pentium III. W83194BR-63S provides 64 CPU/PCI frequencies which are selectable with smooth transitions by hardware or software. W83194BR-63S also provides 13 SDRAM clocks.

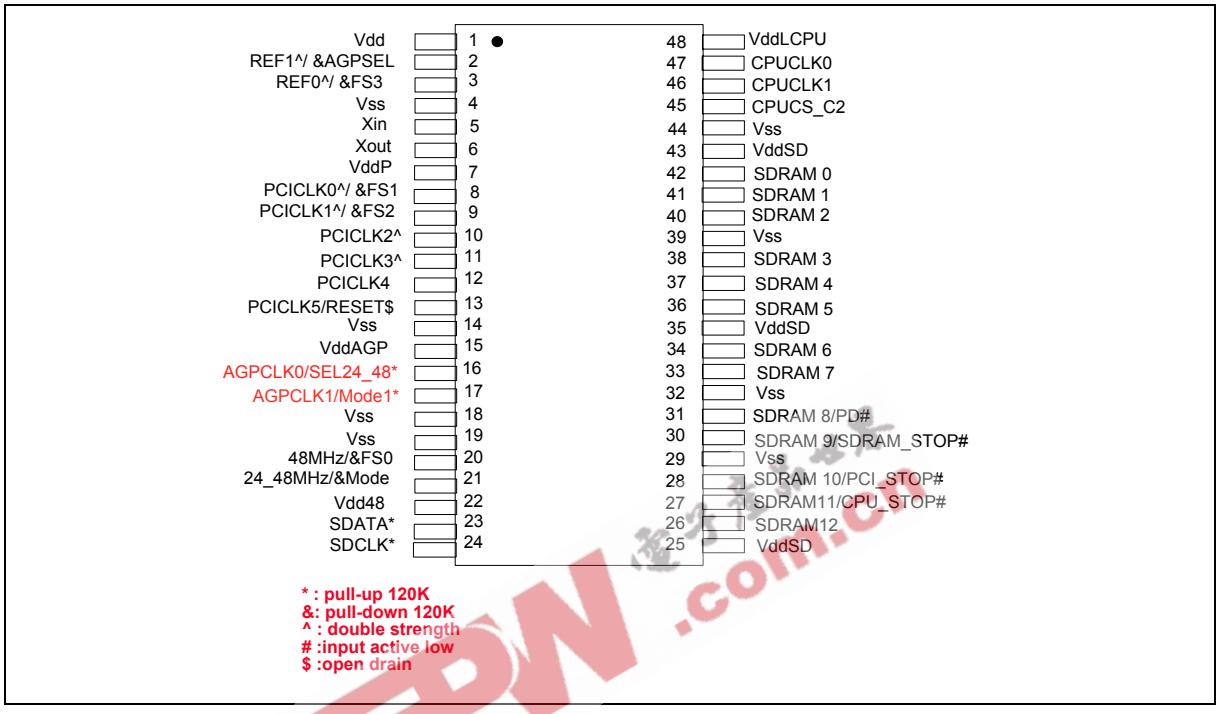
The W83194BR-63S provides step-less frequency programming by controlling the VCO freq. and the programmable PCI clock output divisor ratio. A watch dog timer is quipped and when time out, the RESET# pin will output 4ms pulse signal.

The W83194BR-63S accepts a 14.318 MHz reference crystal as its input. Spread spectrum built in at 0~-0.5% or ±0.25% to reduce EMI. Programmable stopping individual clock outputs and frequency selection through I^2C interface. The device meets the Pentium power-up stabilization, which requires CPU and PCI clocks be stable within 2 ms after power-up. Using dual function pin for the slots(ISA, PCI, CPU, DIMM) is not recommend.

2. PRODUCT FEATURES

- Supports Pentium™ II and Pentium™ III CPU with I^2C.
- 3 CPU clocks (one free-running CPU clock)
- 13 SDRAM clocks for 3 DIMMs
- 6 PCI synchronous clocks
- 2 AGP clocks
- 2 REF clocks as 14.318MHz outputs
- < 250ps skew among CPU and SDRAM clocks
- < 250ps skew among PCI clocks
- Skew from CPU(earlier) to PCI clock 1 to 4ns, center 2.6ns.
- Smooth frequency switch with selections from 66 MHz to 200 MHz CPU
- Stepless frequency programming by controlling the VCO freq. and the clock output divisor ratio
- Programmable skew for CPU to SDRAM and CPU to AGP clock outputs
- I^2C 2-Wire serial interface and I^2C read back
- 0~-0.25% or ±0.5% spread spectrum function to reduce EMI
- Programmable registers to enable/stop each output and select modes
- MODE pin for power Management and RESET# out when system hang
- One 48 MHz for USB & one 24_48 MHz for super I/O
- 48-pin SSOP package

3. PIN CONFIGURATION



4. PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

- Active Low

* - Internal 120kΩ pull-up

4.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	5	IN	Crystal input with internal loading capacitors and feedback resistors.
Xout	6	OUT	Crystal output at 14.318MHz nominally.

4.2 CPU, SDRAM, PCI ,AGP Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPUCLK[0:1]	47,46	OUT	Low skew (< 250ps) clock outputs for host frequencies such as CPU, Chipset and Cache. Powered by VddLCPU. Stopped if CPU_STOP# is low.
CPUCS_C2	45	OUT	Low skew (< 250ps) clock outputs for host frequencies such as CPU, Chipset and Cache. Powered by VddLCPU. Stopped if CPU_STOP# is low and Register7 bit7=0.
SDRAM [0:7],12	42,41,40,38,37,36,34,33	OUT	SDRAM clock outputs.
SDRAM 8/PD#	31	OUT	Pin21 &Mode=0, SDRAM clock outputs. Pin21 &Mode=1, PD# input
SDRAM9/ SDRAM_STOP#	30	OUT	Pin21 &Mode=0, SDRAM clock outputs. Pin21 &Mode=1, SDRAM_STOP# input
SDRAM 10/ PCI_STOP#	28	OUT	Pin21 &Mode=0, SDRAM clock outputs. Pin21 &Mode=1, PCI_STOP# input
SDRAM 11/ CPU_STOP#	27	OUT	Pin21 &Mode=0, SDRAM clock outputs. Pin21 &Mode=1, CPU_STOP# input
PCICLK0^/&FS1	8	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
PCICLK1^/&FS2	9	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
PCICLK [2:4]^	10,11,12	I/O	Low skew (< 250ps) PCI clock outputs. Latched Input. SEL24_48&=0, Pin 21 is 24MHz; SEL24_48&=1, Pin21 is 48MHz
PCICLK5/ RESET#	13	I/O	PCI clock during normal operation. (pin17 Mode1*=1) If pin17 Mode1*=0, RESET# (open drain, 4ms low active pulse when Watch Dog time out)
AGPCLK0/ SEL24#_48*	16	I/O	Low skew (< 250ps) AGP clock output. Latched Input. SEL24#_48*=1, Pin 21 is 24MHz; SEL24_48*=0, Pin21 is 48MHz
AGPCLK1/ Mode1*	17	OUT	AGP clock outputs Latched Input. Mode1*=1, Pin 13 is PCICLK; Mode1*=0, Pin2 is RESET#

4.3 I2C Control Interface

SYMBOL	PIN	I/O	FUNCTION
SDATA*	23	I/O	Serial data of I^2C 2-wire control interface
SDCLK*	24	IN	Serial clock of I^2C 2-wire control interface

4.4 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
REF0^ / &AGPSEL	2	I/O	14.318MHz reference clock. This REF output is the atched input for &AGPSEL at initial power up for H/W selecting the output frequency of AGP clocks.
REF1 ^/ &FS3	3	I/O	14.318MHz reference clock. Latched input for FS3 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
24_48MHz / &Mode	21	I/O	24_48MHz output clock, selected by pin16. Latched Input. &Mode=0, Pin 27,28,30,31 are SDRAM clocks; &Mode=1, Pin27,28,29,31 are CPU_STOP#,SDRAM_STOP#,PCI_STOP#,PD#
48MHz / &FS0	20	I/O	48MHz output for USB during normal operation. Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.

4.5 Power Pins

SYMBOL	PIN	FUNCTION
Vdd	1	Power supply for Ref [0:1] crystal and core logic.
VddAGP	15	Power supply for AGP output, 3.3V.
VddLCPU	48	Power supply for CPUCLK[0:3], either 2.5V or 3.3V.
VddP	7	Power supply for PCICLK_F, PCICLK[0:4], 3.3V.
VddSD	43,35,29,25	Power supply for SDRAM[0:12], and CPU PLL core, nominal 3.3V.
Vdd48	19	Power for 24 & 48MHz output buffers and fixed PLL core.
Vss	4,14,18,19,29,32,39, 44	Circuit Ground.

5. FREQUENCY SELECTION BY HARDWARE

				VCO	CPU	SDRAM	PCI	AGPSEL=0	AGPSEL=1
FS3	FS2	FS1	FS0	(MHz)	(MHz)	(MHz)	(MHz)	(MHz)	(MHz)
0	0	0	0	400	66.6	66.6	33.3	66.6	50
0	0	0	1	400	100	100	33.3	66.6	50
0	0	1	0	498	166	166	31.25	62.5	50
0	0	1	1	400	133.3	133.3	33.3	66.6	50
0	1	0	0	400	66.6	100	33.3	66.6	50
0	1	0	1	400	100	66.6	33.3	66.6	50
0	1	1	0	400	100	133	33.3	66.6	50
0	1	1	1	400	133.3	100	33.3	66.6	50
1	0	0	0	336	112	112	33.6	67.2	56
1	0	0	1	372	124	124	31	62	46.5
1	0	1	0	414	138	138	34.5	69	51.8
1	0	1	1	300	150	150	30	60	50
1	1	0	0	399.6	66.6	133	33.3	66.6	50
1	1	0	1	300	100	150	30	60	50
1	1	1	0	300	150	100	30	60	50
1	1	1	1	480	160	120	30	60	48

6. SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the default state at true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the sequence described below (Register 0, Register 1, Register 2, ...) will be valid and acknowledged.

Bytes sequence order for I^2C controller :

Clock Address A(6:0) & R/W	**Ack**	**8 bits dummy Command code**	**Ack**	**8 bits dummy Byte count**	**Ack**	**Byte0,1,2... until Stop**

Set R/W to 1 when Read back", the data sequence is as follows :

Clock Address A(6:0) & R/W	**Ack**	**Byte 0**	**Ack**	**Byte 1**	**Ack**	**Byte2, 3, 4... until Stop**

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Frequency by software

						VCO	CPU	SDRAM	PCI	AGPSEL=0	AGPSEL=1
SSEL5	SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	(MHz)	(MHz)	(MHz)	(MHz)	(MHz)	(MHz)
0	0	0	0	0	0	400	66.6	66.6	33.3	66.6	50
0	0	0	0	0	1	400	100	100	33.3	66.6	50
0	0	0	0	1	0	498	166	166	31.25	62.5	50
0	0	0	0	1	1	400	133.3	133.3	33.3	66.6	50
0	0	0	1	0	0	400	66.6	100	33.3	66.6	50
0	0	0	1	0	1	400	100	66.6	33.3	66.6	50
0	0	0	1	1	0	400	100	133	33.3	66.6	50
0	0	0	1	1	1	400	133.3	100	33.3	66.6	50
0	0	1	0	0	0	336	112	112	33.6	67.2	56
0	0	1	0	0	1	372	124	124	31	62	46.5
0	0	1	0	1	0	414	138	138	34.5	69	51.8
0	0	1	0	1	1	300	150	150	30	60	50
0	0	1	1	0	0	400	66.6	133.3	33.3	66.6	50
0	0	1	1	0	1	300	100	150	30	60	50
0	0	1	1	1	0	300	150	100	30	60	50
0	0	1	1	1	1	480	160	120	30	60	48
0	1	0	0	0	0	420	70	105	35	70	52.5
0	1	0	0	0	1	432	72	108	36	72	54
0	1	0	0	1	0	333.2	83.3	111.07	33.3	66.6	55.5
0	1	0	0	1	1	388	97	129.33	32.335	64.67	48.5
0	1	0	1	0	0	408	102	136	34	68	51
0	1	0	1	0	1	416	104	138.67	34.665	69.33	52
0	1	0	1	1	0	420	105	140	35	70	52.5
0	1	0	1	1	1	428	107	142.67	35.665	71.33	53.5
0	1	1	0	0	0	412	103	68.67	34.335	68.67	51.5
0	1	1	0	0	1	420	105	70	35	70	52.5
0	1	1	0	1	0	424	106	106	35.335	70.67	53
0	1	1	0	1	1	428	107	107	35.665	71.33	53.5
0	1	1	1	0	0	412	103	103	34.335	68.67	51.5
0	1	1	1	0	1	420	105	105	35	70	52.5
0	1	1	1	1	0	424	106	106	35.335	70.67	53
0	1	1	1	1	1	432	108	108	36	72	54

Frequency by software, continued

SSEL5	SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	VCO (MHz)	CPU (MHz)	SDRAM (MHz)	PCI (MHz)	AGPSEL=0 (MHz)	AGPSEL=1 (MHz)
1	0	0	0	0	0	390	130	130	32.5	65	48.75
1	0	0	0	0	1	405	135	135	33.75	67.5	50.63
1	0	0	0	1	0	408	136	136	34	68	51
1	0	0	0	1	1	417	139	139	34.75	69.5	52.13
1	0	0	1	0	0	420	140	140	35	70	52.5
1	0	0	1	0	1	426	142	142	35.5	71	53.25
1	0	0	1	1	0	429	143	143	35.75	71.5	53.63
1	0	0	1	1	1	435	145	145	36.25	72.5	54.38
1	0	1	0	0	0	390	130	130	32.5	65	48.75
1	0	1	0	0	1	405	135	135	33.75	67.5	50.63
1	0	1	0	1	0	414	138	138	34.5	69	51.75
1	0	1	0	1	1	426	142	142	35.5	71	53.25
1	0	1	1	0	0	411	137	137	34.25	68.5	51.38
1	0	1	1	0	1	417	139	139	34.75	69.5	52.13
1	0	1	1	1	0	423	141	141	35.25	70.5	52.88
1	0	1	1	1	1	426	142	142	35.5	71	53.25
1	1	0	0	0	0	390	130	97.5	32.5	65	48.75
1	1	0	0	0	1	396	132	99	33	66	49.5
1	1	0	0	1	0	408	136	102	34	68	51
1	1	0	0	1	1	411	137	102.75	34.25	68.5	51.38
1	1	0	1	0	0	414	138	103.5	34.5	69	51.75
1	1	0	1	0	1	426	142	106.5	26.625	53.25	42.6
1	1	0	1	1	0	432	144	108	27	54	43.2
1	1	0	1	1	1	438	146	109.5	27.375	54.75	43.8
1	1	1	0	0	0	450	150	112.5	28.125	56.25	45
1	1	1	0	0	1	459	153	114.75	28.69	57.38	45.9
1	1	1	0	1	0	468	156	117	29.25	58.5	46.8
1	1	1	0	1	1	489	163	122.25	30.565	61.13	48.9
1	1	1	1	0	0	498	166	124.5	31.125	62.25	49.8
1	1	1	1	0	1	525	175	131.25	32.815	65.63	52.5
1	1	1	1	1	0	534	178	133.5	33.375	66.75	53.4
1	1	1	1	1	1	549	183	137.25	34.315	68.63	54.9

6.1 Register 0: Frequency Select Register

Bit	@PowerUp	Pin	Description
7	0	-	SSEL5 (Frequency table selection by software via I^2C)
6	0	-	SSEL4 (Frequency table selection by software via I^2C)
5	0	-	SSEL3 (Frequency table selection by software via I^2C)
4	0	-	SSEL2 (Frequency table selection by software via I^2C)
3	0	-	SSEL1 (Frequency table selection by software via I^2C)
2	0	-	SSEL0 (Frequency table selection by software via I^2C)
1	0	-	0 = Selection by hardware 1 = Selection by software I^2C - Bit (7:2)
0	0	-	0 = Running 1 = Tristate all outputs

6.2 Register 1 : CPU Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	-	CPUCS_C2 free running control 1=can be stopped by CPU_STOP# 0= CPUCS_C2 is free running
6	1	27	SDRAM11 (Active / Inactive)
5	0	-	0 = Normal 1 = Spread spectrum enable
4	0	-	0 = ±0.25% Center type Spread Spectrum Modulation 1 =0 ~ (-0.5%) Down type Spread Spectrum Modulation
3	1	26	SDRAM12 (Active / Inactive)
2	1	45	CPUCS_C2(Active / Inactive)
1	1	46	CPUCLK1(Active / Inactive)
0	1	47	CPUCLK0(Active / Inactive)

6.3 Register 2: PCI Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	17	AGPCLK1(Active / Inactive)
6	1	16	AGPCLK0(Active / Inactive)
5	1	13	PCICLK5 (Active / Inactive)
4	1	12	PCICLK4 (Active / Inactive)
3	1	11	PCICLK3 (Active / Inactive)
2	1	10	PCICLK2 (Active / Inactive)
1	1	9	PCICLK1 (Active / Inactive)
0	1	8	PCICLK0 (Active / Inactive)

6.4 Register 3: SDRAM Clock Additional Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	33	SDRAM7 (Active / Inactive)
6	1	34	SDRAM6 (Active / Inactive)
5	1	36	SDRAM5 (Active / Inactive)
4	1	37	SDRAM4 (Active / Inactive)
3	1	38	SDRAM3 (Active / Inactive)
2	1	40	SDRAM2 (Active / Inactive)
1	1	41	SDRAM1 (Active / Inactive)
0	1	42	SDRAM0 (Active / Inactive)

6.5 Register 4: PCI Clock Additional Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	**X**	-	**AGPSEL#**
6	**X**	-	**FS3#**
5	**X**	-	**FS2#**
4	**X**	-	**FS1#**
3	**X**	-	**FS0#**
2	1	28	SDRAM10 (Active / Inactive)
1	1	30	SDRAM9 (Active / Inactive)
0	1	31	SDRAM8 (Active / Inactive)

6.6 Register 5: Skew Register

Bit	@PowerUp	Pin	Description
7	**1**	-	**CSkew2 (SDRAM to CPU skew program bit)**
6	**0**	-	**CSkew1 (SDRAM to CPU skew program bit)**
5	**0**	-	**CSkew0 (SDRAM to CPU skew program bit)**
4	1	-	**CAkew2 (AGP to CPU skew program bit)**
3	0	-	**CAkew1 (AGP to CPU skew program bit)**
2	0	-	**CAkew0 (AGP to CPU skew program bit)**
1	1	21	24_48MHz(Active / Inactive)
0	1	20	48MHz(Active / Inactive)

6.7 Register 6: Watchdog Timer Register

Bit	@PowerUp	Pin	Description
7	0	-	Enable Count 1 = start timer 0 = stop timer
6	X	-	Second timeout status (READ ONLY)
5	0	-	Second count 5
4	0	-	Second count 4
3	0	-	Second count 3
2	0	-	Second count 2
1	0	-	Second count 1
0	0	-	Second count 0

6.8 Register 7: M/N Program Register and Divisor

Bit	@PowerUp	Pin	Description
7	0	-	N value bit 8
6	1	-	Test 1 (Internal test use)
5	0	-	Test 0 (Internal test use)
4	0	-	M value bit 4
3	0	-	M value bit 3
2	0	-	M value bit 2
1	0	-	M value bit 1
0	0	-	M value bit 0

6.9 Register 8: M/N Program Register

Bit	@PowerUp	Pin	Description
7	0	-	N value bit 7
6	0	-	N value bit 6
5	0	-	N value bit 5
4	0	-	N value bit 4
3	0	-	N value bit 3
2	0	-	N value bit 2
1	0	-	N value bit 1
0	0	-	N value bit 0

6.10 Register 9: Divisor Register

Bit	@PowerUp	Pin	Description
7	0	-	Spread spectrum up count 3
6	0	-	Spread spectrum up count 2
5	0	-	Spread spectrum up count 1
4	0	-	Spread spectrum up count 0
3	0	-	Spread spectrum down count 3
2	0	-	Spread spectrum down count 2
1	0	-	Spread spectrum down count 1
0	0	-	Spread spectrum down count 0

6.11 Register 10: Divisor Register

Bit	@PowerUp	Pin	Description
7	0	-	0: use frequency table 1: use M/N register to program frequency The equation is **VCO freq. = 14.318MHz * (N+4)/ M**
6	X	-	Ratio SEL3 (See ratio selection table)
5	X	-	Ratio SEL2 (See ratio selection table)
4	X	-	Ratio SEL1 (See ratio selection table)
3	X	-	Ratio SEL0 (See ratio selection table)
2	X	-	AGP Ratio SEL2 (See ratio selection table1)
1	X	-	AGP Ratio SEL1 (See ratio selection table1)
0	X	-	AGP Ratio SEL0 (See ratio selection table1)

6.12 Register 11: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	0	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	0	-	Winbond Chip ID
3	0	-	Winbond Chip ID
2	1	-	Winbond Chip ID
1	0	-	Winbond Chip ID
0	1	-	Winbond Chip ID

6.13 Register 12: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	0	-	Winbond Chip ID
5	1	-	Winbond Chip ID
4	0	-	Winbond Chip ID
3	0	-	Version ID
2	0	-	Version ID
1	0	-	Version ID
0	1	-	Version ID

Ratio selection table

Reg10 bit6	Reg10 bit5	Reg10 bit4	Reg10 bit3	VCO/ CPU	VCO/ SDRAM	VCO/ PCI
SSEL3	SSEL2	SSEL1	SSEL0	ratio	ratio	ratio
0	0	0	0	2	2	10
0	0	0	1	2	3	10
0	0	1	0	3	2	10
0	0	1	1	3	3	10
0	1	0	0	3	3	12
0	1	0	1	3	3	16
0	1	1	0	3	4	12
0	1	1	1	3	4	16
1	0	0	0	4	3	10
1	0	0	1	4	3	12
1	0	1	0	4	3	16
1	0	1	1	4	4	12
1	1	0	0	4	6	12
1	1	0	1	6	3	12
1	1	1	0	6	4	12
1	1	1	1	6	6	12

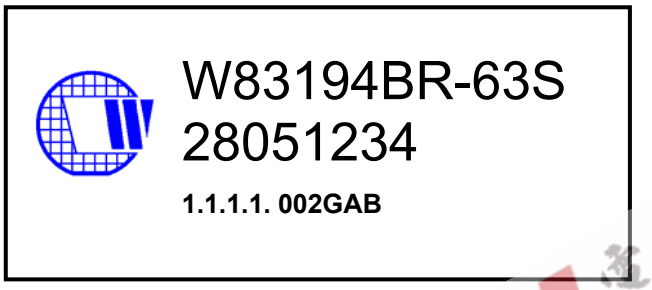
Ratio Selection Table 1

Reg10 bit2	Reg10 bit1	Reg10 bit0	VCO/AGP
AGP2	AGP1	AGP0	ratio
0	0	0	3
0	0	1	5
0	1	0	6
0	1	1	8
1	0	0	4
1	0	1	-
1	1	0	-
1	1	1	10

7. ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83194BR-63S	48 PIN SSOP	Commercial, 0°C to +70°C

8. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194BR-63S

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

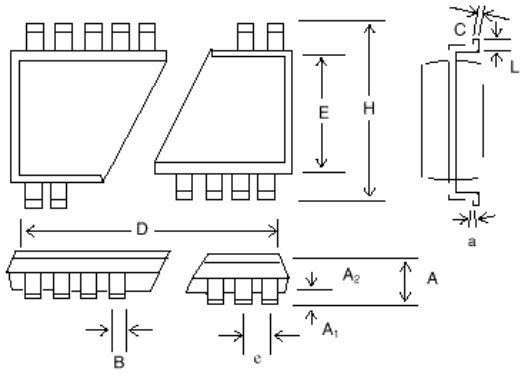
002: packages made in '00, week 02

G: assembly house ID; O means OSE, G means GR

A: Internal use code

B: IC revision

9. PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

10. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
		n.a.	All of the versions before 0.50 are for internal use.
1.0	02/Apr	n.a.	Change version and version on web site to 1.0
2.0	May 19, 2005	16	ADD Important Notice

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

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