



## 512MB - 64Mx64 SDRAM UNBUFFERED

### FEATURES

- PC100 and PC133 compatible
- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3V ± 0.3V Power Supply
- 144 Pin SO-DIMM JEDEC
  - Ultra-low package height:  
AD1: 27.94 mm (1.1")

### DESCRIPTION

The WED3DG6466V is a 64Mx64 synchronous DRAM module which consists of eight 64Mx8 SDRAM components in TSOP II package, and one 2K EEPROM in an 8 pin TSSOP package for Serial Presence Detect which are mounted on a 144 pin SO-DIMM multilayer FR4 Substrate.

\* This product is subject to change without notice.

NOTE: Because of the low package height, there are no termination resistors.

### PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

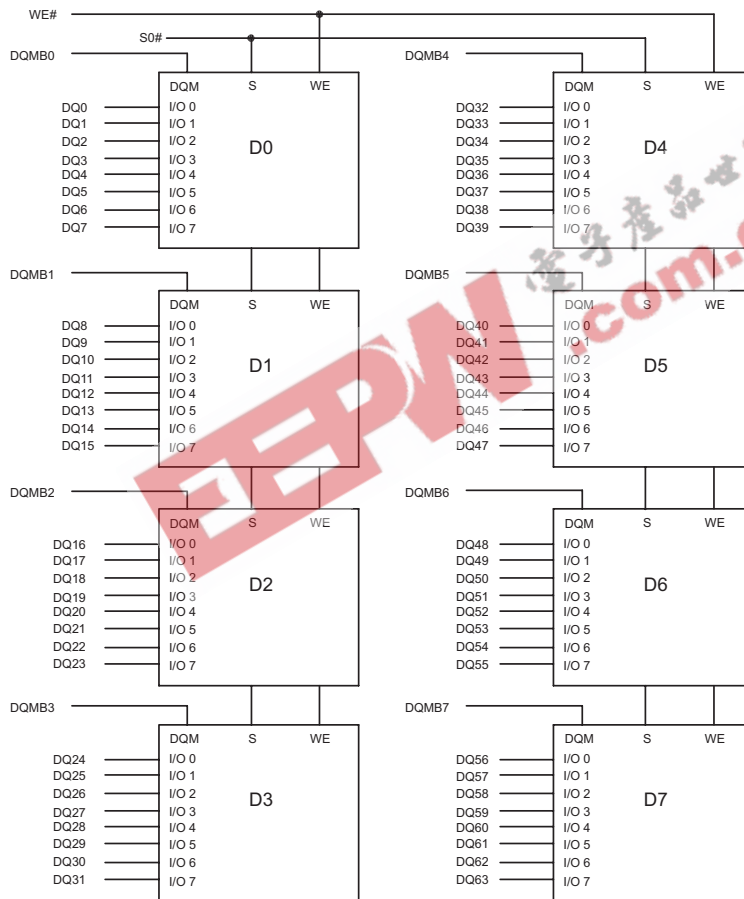
| PINOUT |                 |     |                 |     |                 |     |                 |     |                 |     |                 |
|--------|-----------------|-----|-----------------|-----|-----------------|-----|-----------------|-----|-----------------|-----|-----------------|
| PIN    | FRONT           | PIN | BACK            | PIN | FRONT           | PIN | BACK            | PIN | BACK            | PIN | BACK            |
| 1      | V <sub>ss</sub> | 2   | V <sub>ss</sub> | 49  | DQ13            | 50  | DQ45            | 97  | DQ22            | 98  | DQ54            |
| 3      | DQ0             | 4   | DQ32            | 51  | DQ14            | 52  | DQ46            | 99  | DQ23            | 100 | DQ55            |
| 5      | DQ1             | 6   | DQ33            | 53  | DQ15            | 54  | DQ47            | 101 | V <sub>cc</sub> | 102 | V <sub>cc</sub> |
| 7      | DQ2             | 8   | DQ34            | 55  | V <sub>ss</sub> | 56  | V <sub>ss</sub> | 103 | A6              | 104 | A7              |
| 9      | DQ3             | 10  | DQ35            | 57  | NC              | 58  | NC              | 105 | A8              | 106 | BA0             |
| 11     | V <sub>cc</sub> | 12  | V <sub>cc</sub> | 59  | NC              | 60  | NC              | 107 | V <sub>ss</sub> | 108 | V <sub>ss</sub> |
| 13     | DQ4             | 14  | DQ36            | 61  | CKL0            | 62  | CKE0            | 109 | A9              | 110 | BA1             |
| 15     | DQ5             | 16  | DQ37            | 63  | V <sub>cc</sub> | 64  | V <sub>cc</sub> | 111 | A10             | 112 | A11             |
| 17     | DQ6             | 18  | DQ38            | 65  | RAS#            | 66  | CAS#            | 113 | V <sub>cc</sub> | 114 | V <sub>cc</sub> |
| 19     | DQ7             | 20  | DQ39            | 67  | WE#             | 68  | NC              | 115 | DQMB2           | 116 | DQMB6           |
| 21     | V <sub>ss</sub> | 22  | V <sub>ss</sub> | 69  | CS0#            | 70  | A12             | 117 | DQMB3           | 118 | DQMB7           |
| 23     | DQMB0           | 24  | DQMB4           | 71  | NC              | 72  | NC              | 119 | V <sub>ss</sub> | 120 | V <sub>ss</sub> |
| 25     | DQMB1           | 26  | DQMB5           | 73  | NC              | 74  | CK1             | 121 | DQ24            | 122 | DQ56            |
| 27     | V <sub>cc</sub> | 28  | V <sub>cc</sub> | 75  | V <sub>ss</sub> | 76  | V <sub>ss</sub> | 123 | DQ25            | 124 | DQ57            |
| 29     | A0              | 30  | A3              | 77  | NC              | 78  | NC              | 125 | DQ26            | 126 | DQ58            |
| 31     | A1              | 32  | A4              | 79  | NC              | 80  | NC              | 127 | DQ27            | 128 | DQ59            |
| 33     | A2              | 34  | A5              | 81  | V <sub>cc</sub> | 82  | V <sub>cc</sub> | 129 | V <sub>cc</sub> | 130 | V <sub>cc</sub> |
| 35     | V <sub>ss</sub> | 36  | V <sub>ss</sub> | 83  | DQ16            | 84  | DQ48            | 131 | DQ28            | 132 | DQ60            |
| 37     | DQ8             | 38  | DQ40            | 85  | DQ17            | 86  | DQ49            | 133 | DQ29            | 134 | DQ61            |
| 39     | DQ9             | 40  | DQ41            | 87  | DQ18            | 88  | DQ50            | 135 | DQ30            | 136 | DQ62            |
| 41     | DQ10            | 42  | DQ42            | 89  | DQ19            | 90  | DQ51            | 137 | DQ31            | 138 | DQ63            |
| 43     | DQ11            | 44  | DQ43            | 91  | V <sub>ss</sub> | 92  | V <sub>ss</sub> | 139 | V <sub>ss</sub> | 140 | V <sub>ss</sub> |
| 45     | V <sub>cc</sub> | 46  | V <sub>cc</sub> | 93  | DQ20            | 94  | DQ52            | 141 | SDA             | 142 | SCL             |
| 47     | DQ12            | 48  | DQ44            | 95  | DQ21            | 96  | DQ53            | 143 | V <sub>cc</sub> | 144 | V <sub>cc</sub> |

### PIN NAMES

|                 |                             |
|-----------------|-----------------------------|
| A0 – A12        | Address Input (Multiplexed) |
| BA0-1           | Select Bank                 |
| DQ0-63          | Data Input/Output           |
| CK0, CK1        | Clock Input                 |
| CKE0            | Clock Enable Input          |
| CS0             | Chip Select Input           |
| RAS#            | Row Address Strobe          |
| CAS#            | Column Address Strobe       |
| WE#             | Write Enable                |
| DQMB0-7         | DQM                         |
| V <sub>cc</sub> | Power Supply (3.3V)         |
| V <sub>ss</sub> | Ground                      |
| SDA             | Serial Data I/O             |
| SCL             | Serial Clock                |
| DNU             | Do Not Use                  |
| NC              | No Connect                  |



FUNCTIONAL BLOCK DIAGRAM



NOTE: DQ writing may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

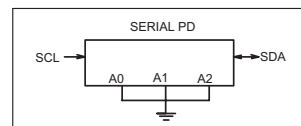
RAS# → RAS#: SDRAM D0-D7  
 CAS# → CAS#: SDRAM D0-D7  
 CKE0 → CKE: SDRAM D0-D7

BA0-BA1 → BA0-BA1: SDRAM D0-D7  
 A0-A12 → A0-A12: SDRAM D0-D7

VDD → D0-D7  
 VSS → D0-D7

| *CLOCK WIRING |            |
|---------------|------------|
| CLOCK INPUT   | SDRAMS     |
| *CK0          | 4 - SDRAMs |
| *CK1          | 4 - SDRAMs |

\*Wire per Clock Loading Table/Wiring Diagrams





## ABSOLUTE MAXIMUM RATINGS

| Parameter                             | Symbol                             | Value      | Units |
|---------------------------------------|------------------------------------|------------|-------|
| Voltage on any pin relative to Vss    | V <sub>IN</sub> , V <sub>OUT</sub> | -1.0 ~ 4.6 | V     |
| Voltage on Vcc supply relative to Vss | V <sub>CC</sub> , V <sub>CCQ</sub> | -1.0 ~ 4.6 | V     |
| Storage Temperature                   | T <sub>STG</sub>                   | -55 ~ +150 | °C    |
| Power Dissipation                     | P <sub>D</sub>                     | 9          | W     |
| Short Circuit Current                 | I <sub>OS</sub>                    | 50         | mA    |

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## RECOMMENDED DC OPERATING CONDITIONS

Voltage Referenced to: V<sub>SS</sub> = 0V, 0°C ≤ T<sub>A</sub> ≤ +70°C

| Parameter             | Symbol          | Min  | Typ | Max                   | Unit | Note                   |
|-----------------------|-----------------|------|-----|-----------------------|------|------------------------|
| Supply Voltage        | V <sub>CC</sub> | 3.0  | 3.3 | 3.6                   | V    |                        |
| Input High Voltage    | V <sub>IH</sub> | 2.0  | 3.0 | V <sub>CCQ</sub> +0.3 | V    | 1                      |
| Input Low Voltage     | V <sub>IL</sub> | -0.3 | —   | 0.8                   | V    | 2                      |
| Output High Voltage   | V <sub>OH</sub> | 2.4  | —   | —                     | V    | I <sub>OH</sub> = -2mA |
| Output Low Voltage    | V <sub>OL</sub> | —    | —   | 0.4                   | V    | I <sub>OL</sub> = -2mA |
| Input Leakage Current | I <sub>LI</sub> | -10  | —   | 10                    | μA   | 3                      |

Note: 1. V<sub>IH</sub> (max)= 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V<sub>IL</sub> (min)= -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V<sub>IN</sub> ≤ V<sub>CCQ</sub>

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

## CAPACITANCE

T<sub>A</sub> = 25°C, f = 1MHz, V<sub>CC</sub> = 3.3V, V<sub>REF</sub> = 1.4V ± 200mV

| Parameter                                | Symbol           | Max | Unit |
|--|------------------|-----|------|
| Input Capacitance (A0-A12)               | C <sub>IN1</sub> | 35  | pF   |
| Input Capacitance (RAS#,CAS#,WE#)        | C <sub>IN2</sub> | 35  | pF   |
| Input Capacitance (CKE0)                 | C <sub>IN3</sub> | 35  | pF   |
| Input Capacitance (CK0)                  | C <sub>IN4</sub> | 16  | pF   |
| Input Capacitance (CS0#)                 | C <sub>IN5</sub> | 35  | pF   |
| Input Capacitance (DQM0-DQM7)            | C <sub>IN6</sub> | 7   | pF   |
| Input Capacitance (BA0-BA1)              | C <sub>IN7</sub> | 35  | pF   |
| Data Input/Output Capacitance (DQ0-DQ63) | C <sub>OUT</sub> | 10  | pF   |

**OPERATING CURRENT CHARACTERISTICS** $V_{CC} = 3.3V$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ 

| Parameter  | Symbol            | Conditions   | Version |       |      |
|--|-------------------|--|---------|-------|------|
|  |                   |  | 100/133 | Units | Note |
| Operating Current<br>(One bank active)           | I <sub>CC1</sub>  | Burst Length = 1<br>$t_{RC} \leq t_{RC(min)}$<br>$I_{OL} = 0mA$  | 1080    | mA    | 1    |
| Precharge Standby Current<br>in Power Down Mode  | I <sub>CC2P</sub> | $CKE \leq V_{IL(max)}$ , $t_{CC} = 10ns$   | 16      | mA    |      |
| Active Standby Current in<br>Non-Power Down Mode | I <sub>CC3N</sub> | $CKE \geq V_{IH(min)}$ , $CS \geq V_{IH(min)}$ , $t_{CC} = 10ns$ Input<br>signals are changed one time during 20ns | 360     | mA    |      |
| Operating Current (Burst mode)                   | I <sub>CC4</sub>  | $I_O = mA$<br>Page burst<br>4 Banks activated<br>$t_{CCD} = 2CK$   | 1,200   | mA    | 1    |
| Refresh Current                                  | I <sub>CC5</sub>  | $t_{RC} \geq t_{RC(min)}$  | 2,280   | mA    | 2    |
| Self Refresh Current                             | I <sub>CC6</sub>  | $CKE \leq 0.2V$  | 24      | mA    |      |

## Notes:

1. Measured with outputs open.
2. Refresh period is 64ms.



**AC TIMING PARAMETERS**

| Symbol             | Parameter  | Speed Grade<br>100MHz  |     | Speed Grade<br>133MHz          |                                | Units           | Notes |
|--------------------|--|--|-----|--------------------------------|--------------------------------|-----------------|-------|
|                    |  | Min  | Max | Min                            | Max                            |                 |       |
| t <sub>CK</sub>    | Clock Period   | 10   |     | 7.5                            |                                | ns              |       |
| t <sub>CH</sub>    | Clock High Time Rated @1.5V                          | 3  |     | 2.5                            |                                | ns              |       |
| t <sub>CL</sub>    | Clock Low Time                                       | 3  |     | 2.5                            |                                | ns              |       |
| t <sub>IS</sub>    | Input Setup Times                                    | Address/ Command & CKE   | 2   |                                | 1.5                            | ns              |       |
|                    |  | Data   | 2   |                                | 1.5                            | ns              |       |
| t <sub>IH</sub>    | Input Hold Times                                     | Address/Command & CKE  | 1   |                                | 0.8                            | ns              |       |
|                    |  | Data   | 1   |                                | 0.8                            | ns              |       |
| t <sub>AC</sub>    | Output Valid From Clock                              | CAS# Latency = 2 or 3, LVTTL levels, Rated @ 50 pF all outputs switching |     | 6.0<br>(t <sub>CO</sub> = 5.2) | 5.4<br>(t <sub>CO</sub> = 4.6) | ns              | 1     |
| t <sub>OH</sub>    | Output Hold From Clock Rated @ 50 pF (1.8 ns @ 0 pF) | 3  |     | 2.7                            |                                | ns              |       |
| t <sub>OHZ</sub>   | Output Valid to Z                                    | 3  | 9   | 2.7                            | 7                              | ns              |       |
| t <sub>CCD</sub>   | CAS to CAS Delay                                     | 1  |     | 1                              |                                | t <sub>CK</sub> |       |
| t <sub>CBD</sub>   | CAS Bank Delay                                       | 1  |     | 1                              |                                | t <sub>CK</sub> |       |
| t <sub>CKE</sub>   | CKE to Clock Disable                                 | 1  |     | 1                              |                                | t <sub>CK</sub> |       |
| t <sub>RP</sub>    | RAS Precharge Time                                   | 20   |     | 20                             |                                | ns              |       |
| t <sub>RAS</sub>   | RAS Active Time                                      | 50   |     | 45                             |                                | ns              |       |
| t <sub>RCD</sub>   | Activate to Command Delay (RAS to CAS Delay)         | 20   |     | 20                             |                                | ns              |       |
| t <sub>RRD</sub>   | RAS to RAS Bank Activate Delay                       | 20   |     | 15                             |                                | ns              |       |
| t <sub>RC</sub>    | RAS Cycle Time                                       | 70   |     | 67.5                           |                                | ns              |       |
| t <sub>DQD</sub>   | DQM to Input Data Delay                              | 0  |     | 0                              |                                | t <sub>CK</sub> |       |
| t <sub>DWD</sub>   | Write Cmd. to Input Data Delay                       | 0  |     | 0                              |                                | t <sub>CK</sub> |       |
| t <sub>MRD</sub>   | Mode Register set to Active delay                    | 3  |     | 3                              |                                | t <sub>CK</sub> |       |
| t <sub>ROH</sub>   | Precharge to O/P in High Z                           |  | CL  |                                | CL                             | t <sub>CK</sub> | 2     |
| t <sub>DQZ</sub>   | DQM to Data in High Z for read                       | 2  |     | 2                              |                                | t <sub>CK</sub> |       |
| t <sub>DQM</sub>   | DQM to Data mask for write                           | 0  |     | 0                              |                                | t <sub>CK</sub> | 3     |
| t <sub>DPL</sub>   | Data-in to PRE Command Period                        | 20   |     | 15                             |                                | ns              |       |
| t <sub>DAL</sub>   | Data-in to ACT (PRE) Command period (Auto precharge) | 5  |     | 5                              |                                | t <sub>CK</sub> |       |
| t <sub>SB</sub>    | Power Down Mode Entry                                |  | 1   |                                | 1                              | t <sub>CK</sub> |       |
| t <sub>SRX</sub>   | Self Refresh Exit Time                               | 10   |     | 10                             |                                | ns              | 4     |
| t <sub>PDE</sub>   | Power Down Exit Set up Time                          | 1  |     | 1                              |                                | t <sub>CK</sub> | 5     |
| t <sub>CKSTP</sub> | Clock Stop During Self Refresh or Power Down         | 200  |     | 200                            |                                | t <sub>CK</sub> | 6     |
| t <sub>REF</sub>   | Refresh Period                                       |  | 64  |                                | 64                             | ms              |       |
| t <sub>RFC</sub>   | Row Refresh Cycle Time                               | 80.0   |     | 75.0                           |                                | ns              |       |

- Access times to be measured w/input signals of 1 V/ns edge rate, 0.8 V to 2.0 V, t<sub>CO</sub> is clock to output with no load.
- CL = CAS Latency
- Data Masked on the same clock
- Self refresh Exit is asynchronous, requiring 10 ns to ensure initiation. Self refresh exit is complete in 10 ns + t<sub>RC</sub>.
- Timing is asynchronous. If t<sub>IS</sub> is not met by rising edge of CK then CKE is assumed latched on next cycle.
- If the clock is stopped during self refresh or power down, 200 clocks are required before CKE is high.

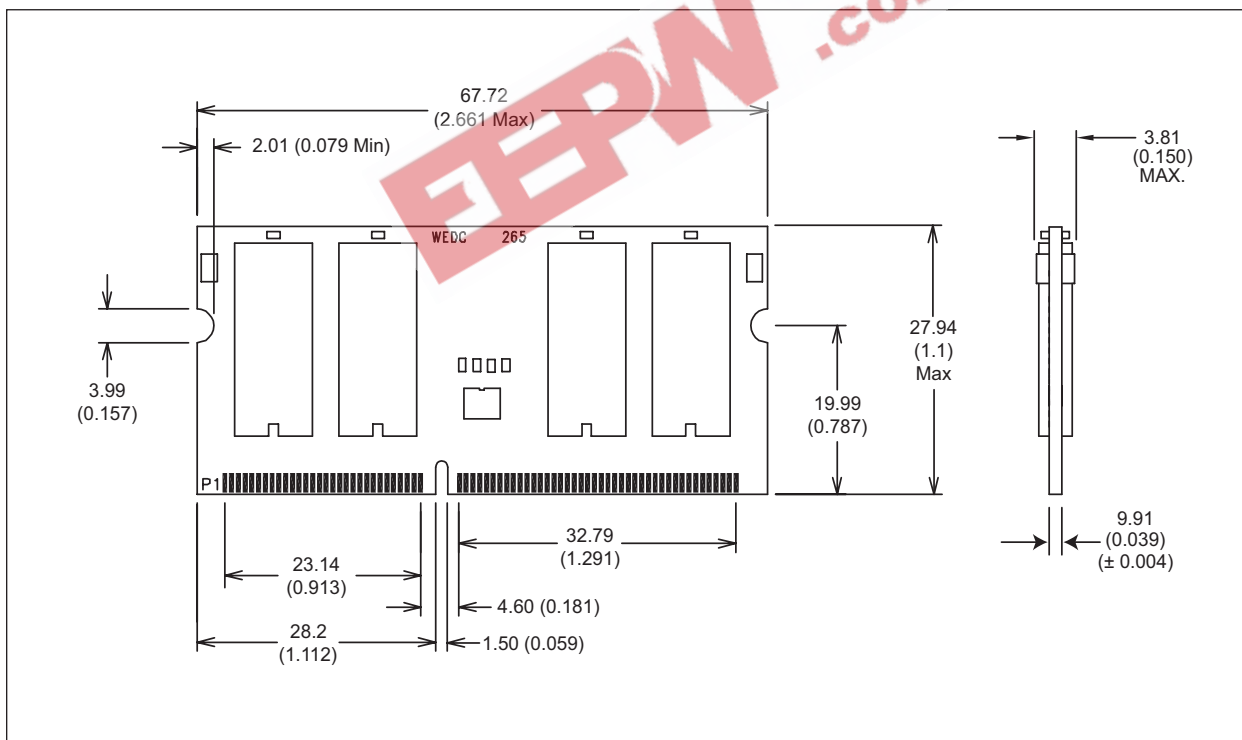


**PACKAGE DIMENSIONS FOR AD1**

| Ordering Information | Speed  | CAS Latency | Height*          |
|----------------------|--------|-------------|------------------|
| WED3DG6466V10AD1     | 100MHz | CL=2        | 27.94 (1.1") MAX |
| WED3DG6466V7AD1      | 133MHz | CL=2        | 27.94 (1.1") MAX |
| WED3DG6466V75AD1     | 133MHz | CL=3        | 27.94 (1.1") MAX |

Note: For industrial temperature range product, add an "I" to the end of the part number.

**PACKAGE DIMENSIONS FOR AD1**



\* All Dimensions are in millimeters and (inches).

**Document Title**

512MB - 64Mx64 SDRAM UNBUFFERED

**Revision History**

| <b>Rev #</b> | <b>History</b>  | <b>Release Date</b> | <b>Status</b> |
|--------------|---|---------------------|---------------|
| Rev 0        | Created Datasheet   | 6-4-03              | Advanced      |
| Rev 1        | 1.1 Updated Datasheet<br>1.2 Added AD1 package option           | 4-04                | Preliminary   |
| Rev 2        | 2.1 Added AC Timing Spec<br>2.2 Moved from Preliminary to Final | 9-04                | Final         |
| Rev 3        | 3.1 Added "ED" to part number                                   | 7-05                | Final         |