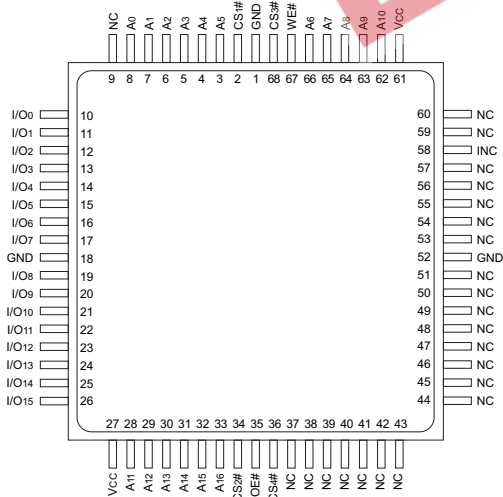




## 512Kx16 CMOS EEPROM MODULE FEATURES

- Access Time of 140, 150, 200ns
- Packaging:
  - 68 lead, 40mm Hermetic CQFP (Package 501)
- Organized as 4 banks of 128Kx16
- Write Endurance 10,000 Cycles
- Data Retention Ten Years Minimum
- Military Temperature Range
- Low Power CMOS
- Automatic Page Write Operation
- Page Write Cycle Time: 10ms Max
- Data Polling for End of Write Detection
- Hardware and Software Data Protection
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- 8 Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight - 20 grams typical

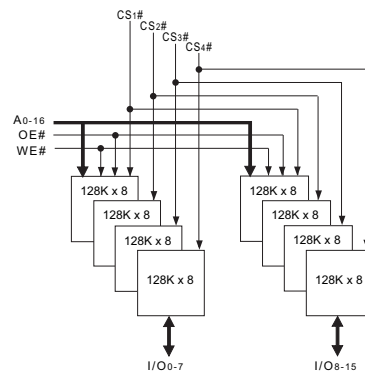
**FIGURE 1 – PIN CONFIGURATION  
Top View**



**Pin Description**

I/O0-15	Data Input/Output
A0-16	Address Inputs
WE#	Write Enable
CS1-4#	Chip Selects
OE#	Output Enable
Vcc	+5.0V Power
GND	Ground
NC	Not Connected

**Block Diagram**



NOTE: CS1-4# are used as bank selects. During reads, only one CSx# can be active at one time.



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol		Unit
Operating Temperature	T <sub>A</sub>	-55 to +125	°C
Storage Temperature	T <sub>STG</sub>	-65 to +150	°C
Signal Voltage Relative to GND	V <sub>G</sub>	-0.6 to +6.25	V
Voltage on OE# and A9		-0.6 to +13.5	V

NOTE:  
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TRUTH TABLE**

CS#	OE#	WE#	Mode	Data I/O
H	X	X	Standby	High Z
L	L	H	Read	Data Out
L	H	L	Write	Data In
X	H	X	Out Disable	High Z/Data Out
X	X	H	Write	
X	L	X	Inhibit	

**CAPACITANCE**

T<sub>A</sub> = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE capacitance	COE	V <sub>IN</sub> = 0 V, f = 1.0 MHz	50	pF
WE capacitance	CWE	V <sub>IN</sub> = 0 V, f = 1.0 MHz	50	pF
CS1-4 capacitance	CCS	V <sub>IN</sub> = 0 V, f = 1.0 MHz	25	pF
Data I/O capacitance	CI/O	V <sub>I/O</sub> = 0 V, f = 1.0 MHz	40	pF
Address input capacitance	CAD	V <sub>IN</sub> = 0 V, f = 1.0 MHz	70	pF

This parameter is guaranteed by design but not tested.

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Input High Voltage	V <sub>IH</sub>	2.0	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	+0.8	V
Operating Temp. (Mil.)	T <sub>A</sub>	-55	+125	°C

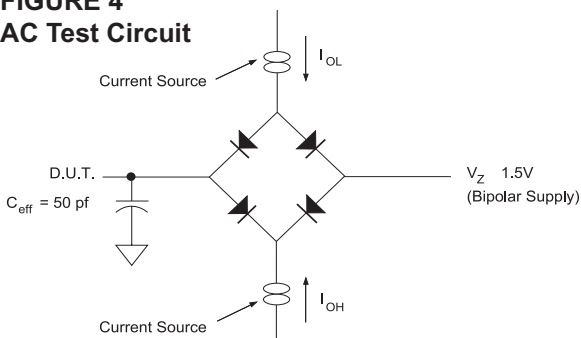
**DC CHARACTERISTICS**

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10	μA
Output Leakage Current	I <sub>LO</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , V <sub>out</sub> = GND to V <sub>CC</sub>		10	μA
Operating Supply Current (x16)	I <sub>CCx16</sub>	CS1# = V <sub>IL</sub> , OE# = CS2-4# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		160	mA
Chip Erase Current	I <sub>CC1</sub>	CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		250	mA
Standby Current	I <sub>SB</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		5	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1mA, V <sub>CC</sub> = 4.5V		0.45	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -400μA, V <sub>CC</sub> = 4.5V	2.4		V

NOTE: DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V

**FIGURE 4  
AC Test Circuit**



**AC TEST CONDITIONS**

Parameter	Typ	Unit
Input Pulse Levels	V <sub>IL</sub> = 0, V <sub>IH</sub> = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes: V<sub>Z</sub> is programmable from -2V to +7V.  
I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.  
Tester Impedance Z<sub>0</sub> = 75Ω.  
V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.  
I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.  
ATE tester includes jig capacitance.



## WRITE

A write cycle is initiated when OE# is high and a low pulse is on WE# or CS# with CS# or WE# low. The address is latched on the falling edge of CS# or WE# whichever occurs last. The data is latched by the rising edge of CS# or WE#, whichever occurs first. A word write operation will automatically continue to completion.

## WRITE CYCLE TIMING

Figures 3 and 4 show the write cycle timing relationships. A write cycle begins with address application, write enable and chip select. Chip select is accomplished by placing the CS# line low. Write enable consists of setting the WE# line low. The write cycle begins when the last of either CS# or WE# goes low.

The WE# line transition from high to low also initiates an internal 150  $\mu$ sec delay timer to permit page mode operation. Each subsequent WE# transition from high to low that occurs before the completion of the 150  $\mu$ sec time out will restart the timer from zero. The operation of the timer is the same as a retriggerable one-shot.

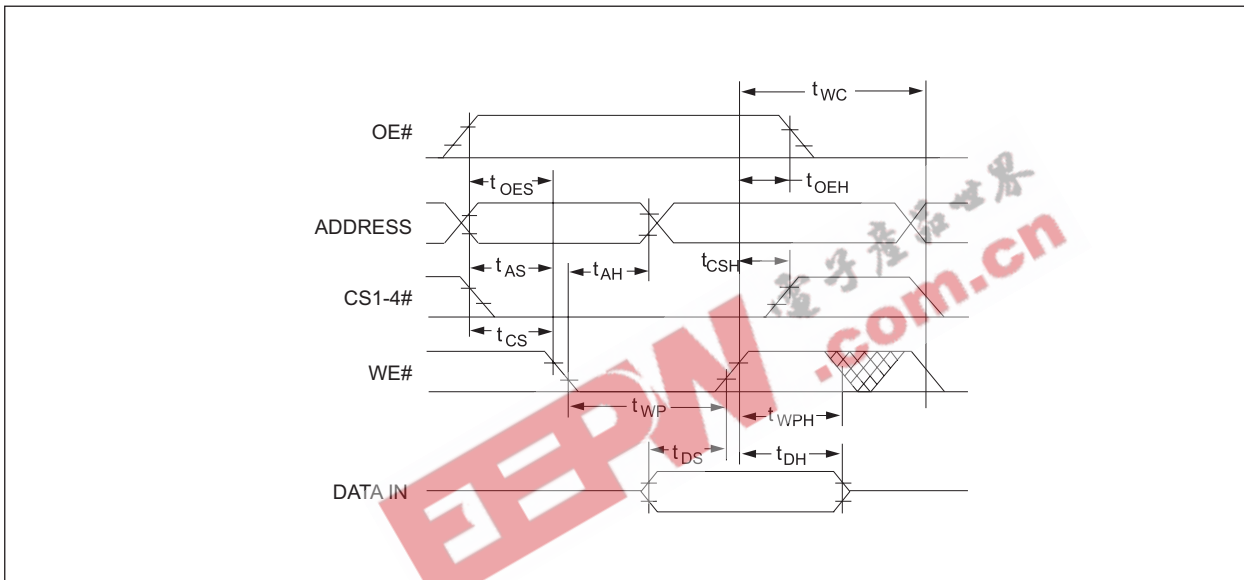
## AC WRITE CHARACTERISTICS

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

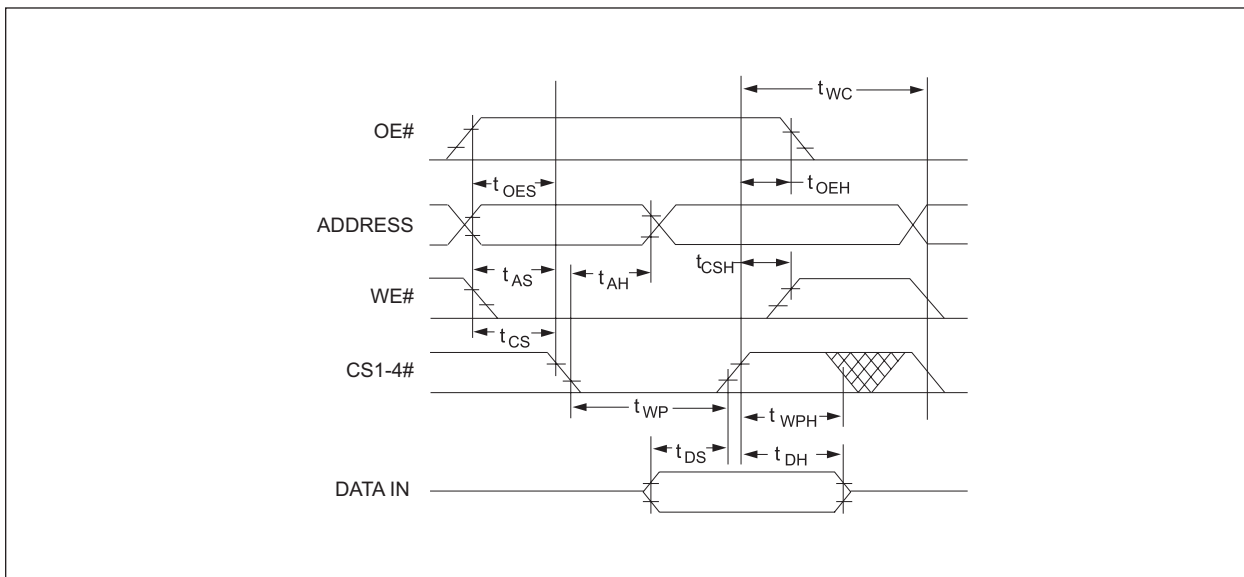
Write Cycle Parameter	Symbol	Min	Max	Unit
Write Cycle Time, TYP = 6ms	t <sub>wc</sub>		10	ms
Address Set-up Time	t <sub>AS</sub>	10		ns
Write Pulse Width (WE# or CS#)	t <sub>WP</sub>	120		ns
Chip Select Set-up Time	t <sub>CS</sub>	0		ns
Address Hold Time	t <sub>AH</sub>	100		ns
Data Hold Time	t <sub>DH</sub>	10		ns
Chip Select Hold Time	t <sub>CSH</sub>	0		ns
Data Set-up Time	t <sub>DS</sub>	100		ns
Output Enable Set-up Time	t <sub>OES</sub>	10		ns
Output Enable Hold Time	t <sub>OEH</sub>	10		ns
Write Pulse Width High	t <sub>WPH</sub>	50		ns



**FIGURE 3 – WRITE WAVEFORM WE# CONTROLLED**



**FIGURE 4 – WRITE WAVEFORM CS# CONTROLLED**





**READ**

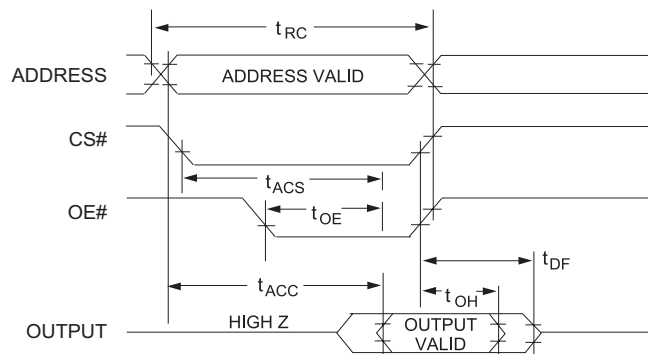
The module stores data at the memory location determined by the address pins. When CS# and OE# are low and WE# is high, this data is present on the outputs. When CS# and OE# are high, the outputs are in a high impedance state. This two line control prevents bus contention.

**AC READ CHARACTERISTICS**

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol	-140		-150		-200		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	140		150		200		ns
Address Access Time	t <sub>ACC</sub>		140		150		200	ns
Chip Select Access Time	t <sub>ACS</sub>		140		150		200	ns
Output Hold from Address Change, OE# or CS#	t <sub>OH</sub>	0		0		0		ns
Output Enable to Output Valid	t <sub>OE</sub>	0	50	0	55	0	55	ns
Chip Select or OE# to High Z Output	t <sub>DF</sub>		50		70		70	ns

**FIGURE 5 – READ WAVEFORMS**



Notes:  
 OE# may be delayed up to t<sub>ACS</sub> - t<sub>OE</sub> after the falling edge of CS# without impact on t<sub>OE</sub> or by t<sub>ACC</sub> - t<sub>OE</sub> after an address change without impact on t<sub>ACC</sub>.  
 CS1-4# are used as bank selects.  
 During reads, only one CSx# can be active at one time.



### DATA POLLING

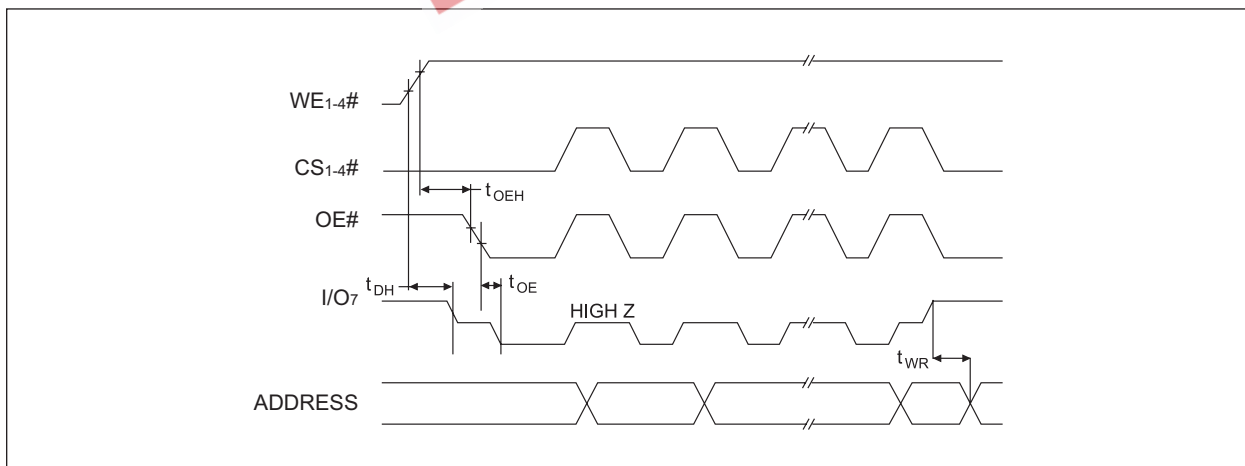
The module offers a data polling feature which allows a faster method of writing to the device. Figure 6 shows the timing diagram for this function. During a word or page write cycle, an attempted read of the last word written will result in the complement of the written data on I/O7 and I/O15. Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. Data polling may begin at any time during the write cycle.

#### DATA POLLING CHARACTERISTICS

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol	Min	Max	Unit
Data Hold Time	t <sub>DH</sub>	10		ns
OE# Hold Time	t <sub>OEH</sub>	10		ns
OE# To Output Valid	t <sub>OE</sub>		55	ns
Write Recovery Time	t <sub>WR</sub>	0		ns

FIGURE 6 – DATA POLLING WAVEFORM





**PAGE WRITE OPERATION**

The module has a page write operation that allows one to 128 words of data to be written into the device and consecutively loads during the internal programming period. Successive words may be loaded in the same manner after the first data word has been loaded. An internal timer begins a time out operation at each write cycle. If another write cycle is completed within 150µs or less, a new time out period begins. Each write cycle restarts the delay period. The write cycles can be continued as long as the interval is less than the time out period.

The usual procedure is to increment the least significant address lines from A0 through A6 at each write cycle. In this manner a page of up to 128 words can be loaded in to the EEPROM in a burst mode before beginning the relatively long interval programming cycle.

After the 150µs time out is completed, the EEPROM begins an internal write cycle. During this cycle the entire page of words will be written at the same time. The internal programming cycle is the same regardless of the number of words accessed.

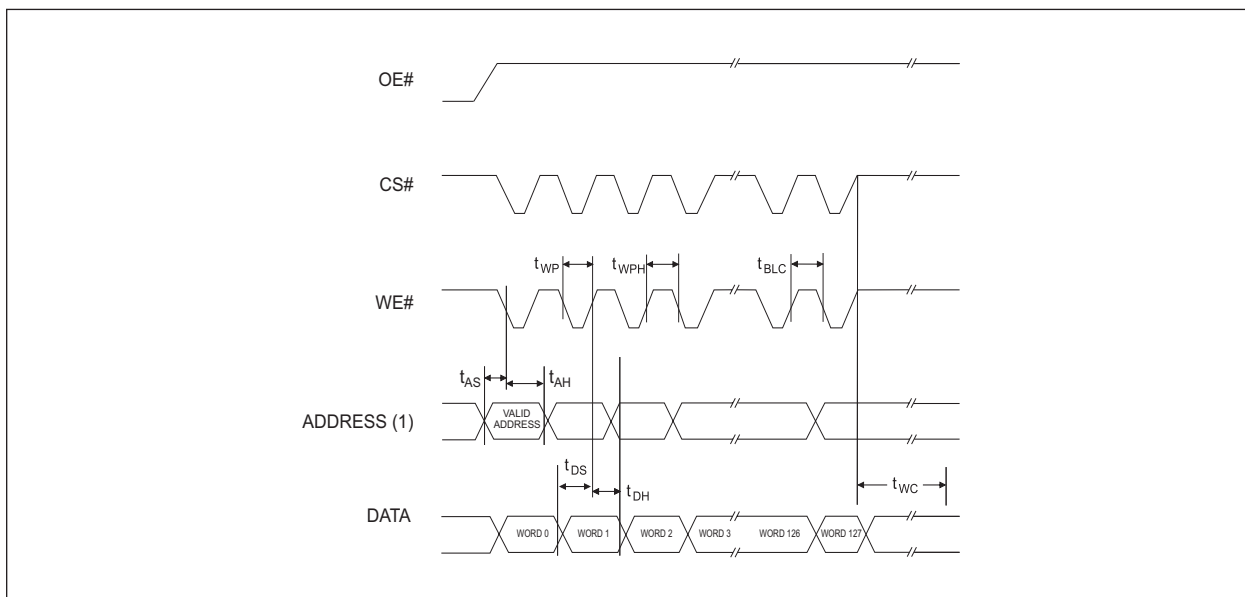
**PAGE WRITE CHARACTERISTICS**

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Page Mode Write Characteristics		Symbol	Min	Max	Unit
Write Cycle Time, TYP = 6ms		t <sub>wc</sub>		10	ms
Address Set-up Time		t <sub>AS</sub>	0		ns
Address Hold Time (1)		t <sub>AH</sub>	50		ns
Data Set-up Time		t <sub>DS</sub>	50		ns
Data Hold Time		t <sub>DH</sub>	0		ns
Write Pulse Width		t <sub>WP</sub>	100		ns
Word Load Cycle Time		t <sub>BLC</sub>		150	µs
Write Pulse Width High		t <sub>WPH</sub>	50		ns

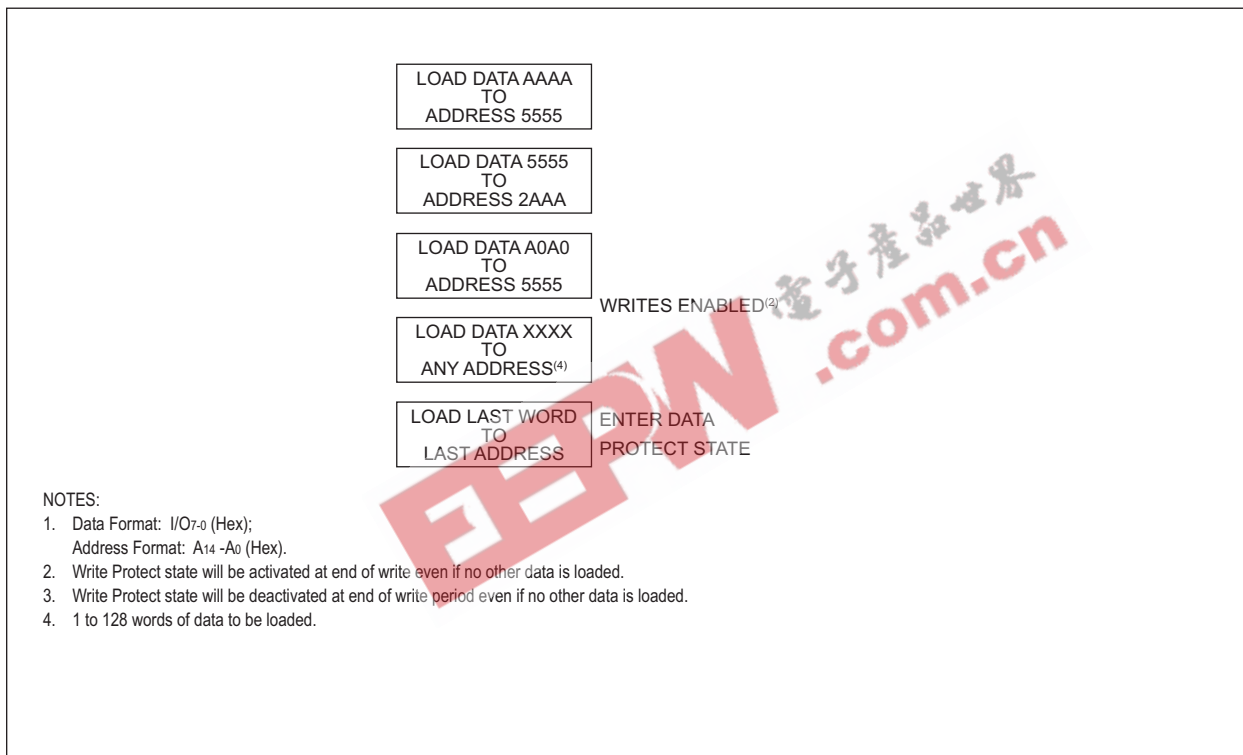
1. Page address must remain valid for duration of write cycle.

**FIGURE 7 – PAGE MODE WRITE WAVEFORM**





**FIGURE 8 – SOFTWARE BLOCK DATA PROTECTION ENABLE ALGORITHM<sup>(1)</sup>**



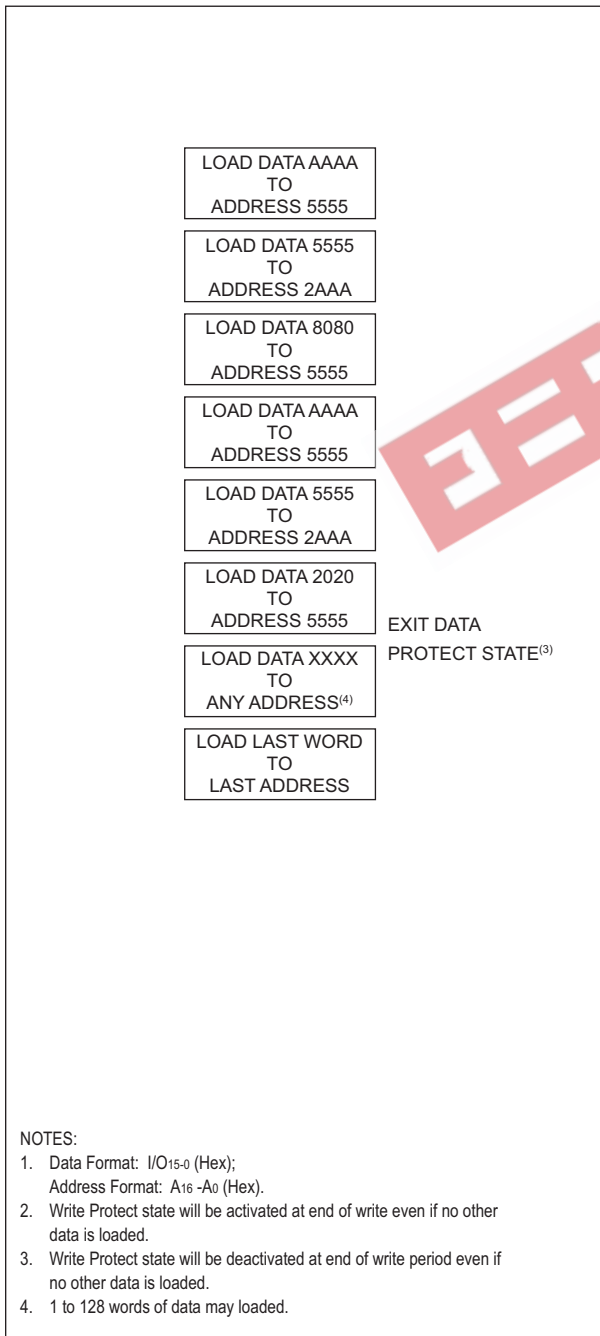
NOTES:

1. Data Format: I/O7-0 (Hex);  
Address Format: A14 -A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 words of data to be loaded.





**FIGURE 9 –  
SOFTWARE BLOCK DATA PROTECTION  
DISABLE ALGORITHM<sup>(1)</sup>**



NOTES:

1. Data Format: I/O<sub>15-0</sub> (Hex);  
Address Format: A<sub>16</sub>-A<sub>0</sub> (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 words of data may loaded.

### SOFTWARE DATA PROTECTION

A software write protection feature may be enabled or disabled by the user. When shipped by White Microelectronics, the module has the feature disabled. Write access to the device is unrestricted.

To enable software write protection, the user writes three access code words to three special internal locations. Once write protection has been enabled, each write to the EEPROM must use the same three-word write sequence to permit writing. After setting software data protection, any attempt to write to the device without the three-word command sequence will start the internal write timers. No data will be written to the device, however, for the duration of *t<sub>wc</sub>*. The write protection feature can be disabled by a six-word write sequence of specific data to specific locations. Power transitions will not reset the software write protection.

Each 128K-word block of the EEPROM has independent write protection. One or more blocks may be enabled and the rest disabled in any combination. The software write protection guards against inadvertent writes during power transitions, or unauthorized modification using a PROM programmer.

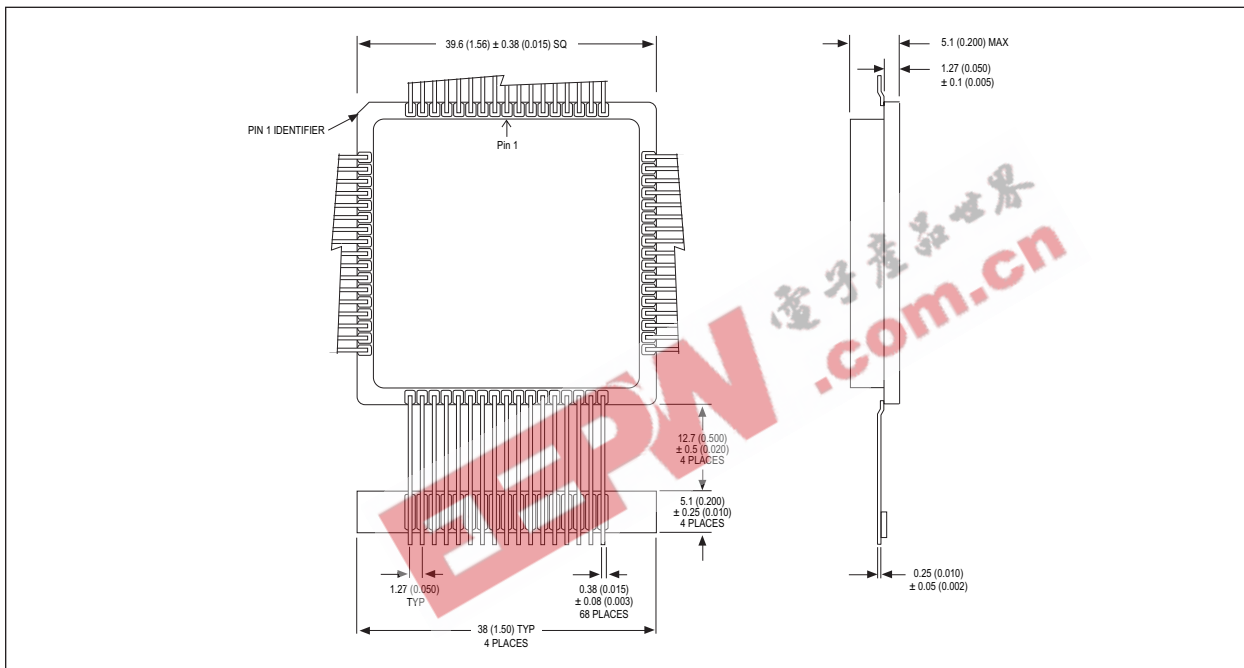
### HARDWARE DATA PROTECTION

These features protect against inadvertent writes to the module. These are included to improve reliability during normal operation:

- a) V<sub>cc</sub> power on delay**  
As V<sub>cc</sub> climbs past 3.8V typical the device will wait 5 msec typical before allowing write cycles.
- b) V<sub>cc</sub> sense**  
While below 3.8V typical write cycles are inhibited.
- c) Write inhibiting**  
Holding OE# low and either CS# or WE# high inhibits write cycles.
- d) Noise filter**  
Pulses of <8ns (typ) on WE# or CS# will not initiate a write cycle.

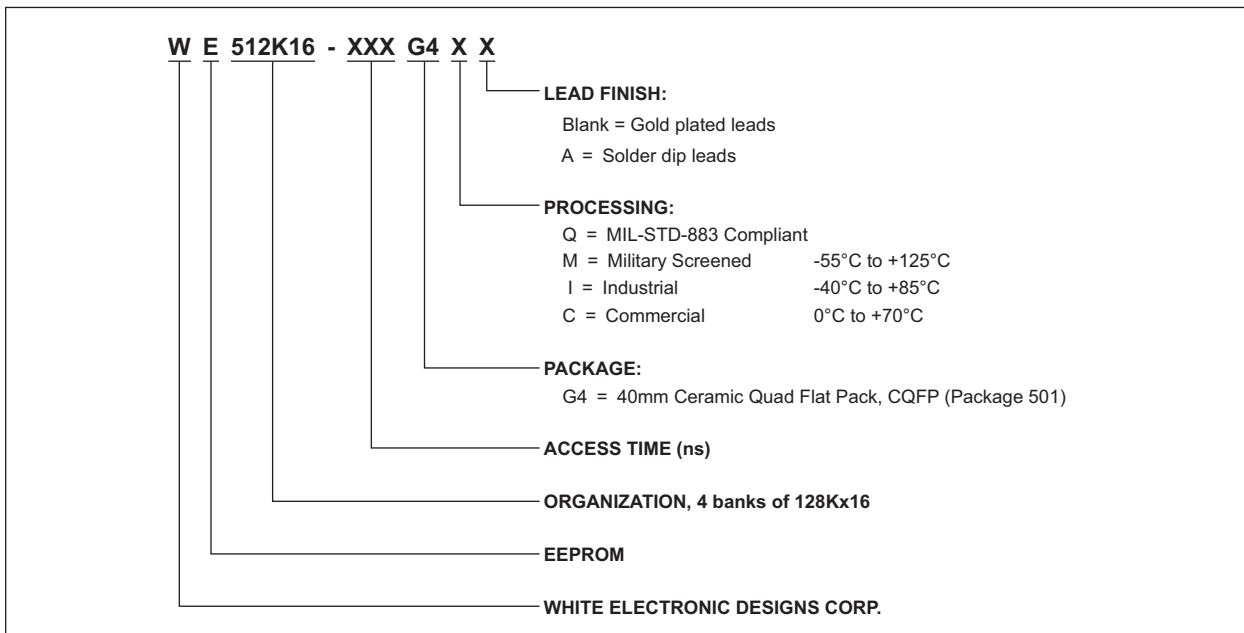


**PACKAGE 501: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G4)**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

**ORDERING INFORMATION**



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