Winbond Electronics Corp.

64K × 16 HIGH-SPEED CMOS STATIC RAM

GENERAL DESCRIPTION

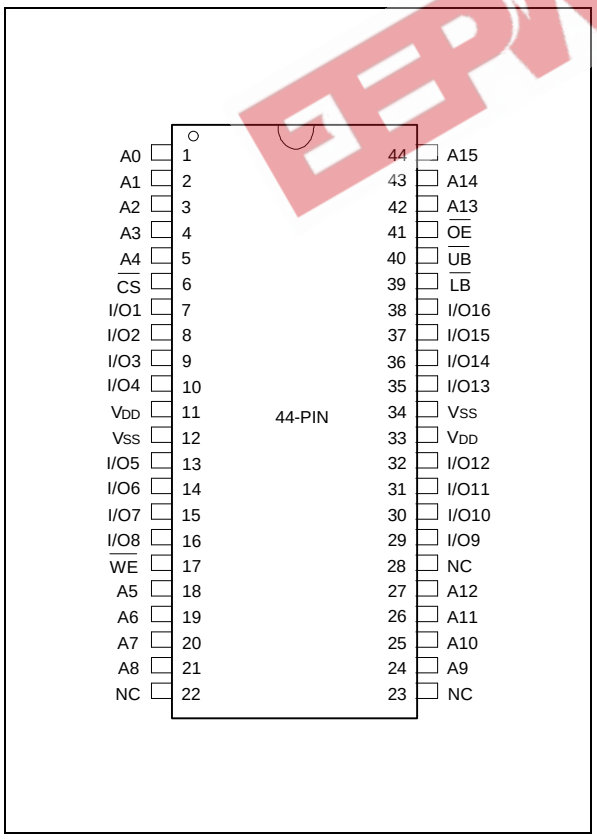
The W26L010A is a high-speed, low-power CMOS static RAM organized as 65,536 × 16 bits that operates on a single 3.3-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

The W26L010A has an active low chip select, separate upper and lower byte selects, and a fast output enable. No clock or refreshing is required. Separate byte select controls ($\overline{LB}$ and $\overline{UB}$) allow individual bytes to be written and read. $\overline{LB}$ controls I/O1-I/O8, the lower byte. $\overline{UB}$ controls I/O9–I/O16, the upper byte. This device is well suited for use in high-density, high-speed system applications.

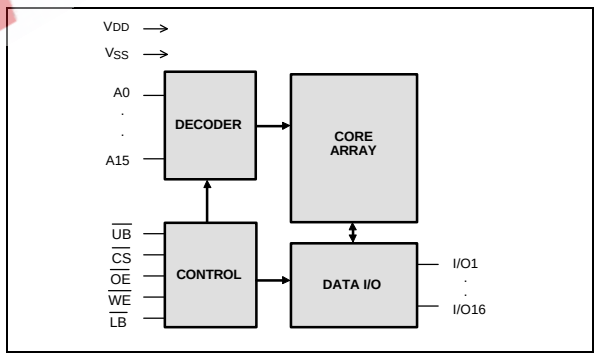
FEATURES

- High speed access time: 10/12 nS (max.)
- Low power consumption:
  - Active: 530 mW (max.)
- Single +3.3V power supply
- Fully static operation
  - No clock or refreshing
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Data byte control
  - $\overline{LB}$ (I/O1–I/O8), $\overline{UB}$ (I/O9–I/O16)
- Available packages: 44-pin 400 mil SOJ and 44-pin TSOP(II)

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A15	Address Inputs
I/O1–I/O16	Data Inputs/Outputs
$\overline{CS}$	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower Byte Select I/O1–I/O8
$\overline{UB}$	Upper Byte Select I/O9–I/O16
VDD	Power Supply
VSS	Ground
NC	No Connection

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	MODE	I/O1- I/O8	I/O9- I/O16	V_{DD} CURRENT
H	X	X	X	X	Not Selected	High Z	High Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High Z	High Z	I_{DD}
L	L	H	L	L	2 Bytes Read	D_{OUT}	D_{OUT}	I_{DD}
L	L	H	L	H	Lower Byte Read	D_{OUT}	High Z	I_{DD}
L	L	H	H	L	Upper Byte Read	High Z	D_{OUT}	I_{DD}
L	X	L	L	L	2 Bytes Write	D_{IN}	D_{IN}	I_{DD}
L	X	L	L	H	Lower Byte Write	D_{IN}	High Z	I_{DD}
L	X	L	H	L	Upper Byte Write	High Z	D_{IN}	I_{DD}
L	X	X	H	H	Output Disable	High Z	High Z	I_{DD}

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to V_{SS} Potential	-0.5 to +4.6	V
Input/Output to V_{SS} Potential	-0.5 to V_{DD} +0.5	V
Allowable Power Dissipation	1.5	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 3.3V ±5%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V_{IL}	-	-0.5	-	+0.8	V
Input High Voltage	V_{IH}	-	+2.0	-	V_{DD} +0.3	V
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}	-10	-	+10	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = V_{SS} to V_{DD} Output Pins in High Z, See Truth Table	-10	-	+10	µA
Output Low Voltage	V_{OL}	I_{OL} = +8.0 mA	-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0 mA	2.4	-	-	V
Operating Power Supply Current	I_{DD}	$\overline{CS}$ = V_{IL} (max.), Cycle = min. 10	-	-	160	mA
		I/O = open, Duty = 100% 12	-	-	140	
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH} (min.), Cycle = min.	-	-	30	mA
	I_{SB1}	$\overline{CS}$ = V_{DD} -0.2V, I/O = open All other pins = V_{DD} -0.2V/GND	-	-	10	mA

Note: Typical characteristics are evaluated at V_{DD} = 3.3V, T_A = 25° C.

CAPACITANCE

(V_{DD} = 3.3V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	8	pF

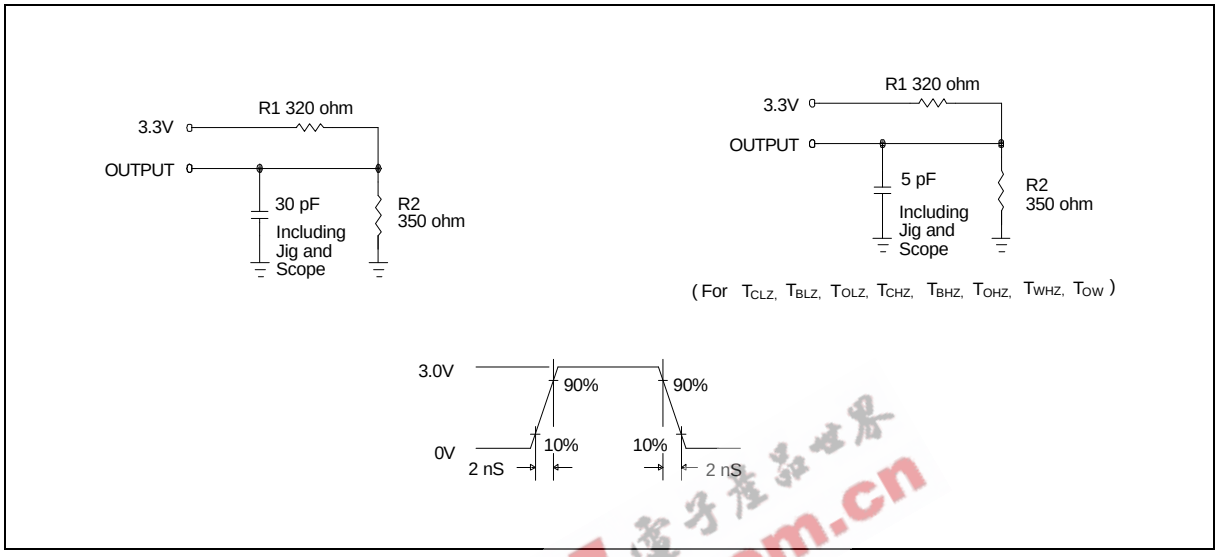
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	2 nS
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 30 pF, I_{OH}/I_{OL} = -4 mA/8 mA

AC Test Loads and Waveform



(V_{DD} = 3.3V ±5%, V_{SS} = 0V, T_A = 0 to 70° C)

(1) Read Cycle

PARAMETER	SYM.	W26L010A-10		W26L010A-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	10	-	12	-	nS
Address Access Time	T_{AA}	–	10	–	12	nS
Chip Select Access Time	T_{ACS}	–	10	–	12	nS
Output Enable to Output Valid	T_{OE}	–	5	–	6	nS
$\overline{UB}$, $\overline{LB}$ Access Time	T_{BA}	–	5	–	6	nS
Output Hold from Address Change	T_{OH}	3	–	3	–	nS
Chip Select to Output in Low Z	T_{CLZ}*	3	–	3	–	nS
Chip Deselect to Output in High Z	T_{CHZ}*	–	5	–	6	nS
Output Enable to Output in Low Z	T_{OLZ}*	0	–	0	–	nS
Output Disable to Output in High Z	T_{OHZ}*	–	5	–	6	nS
$\overline{UB}$, $\overline{LB}$ Select to Output in Low Z	T_{BLZ}*	0	–	0	–	nS
$\overline{UB}$, $\overline{LB}$ Deselect to Output in High Z	T_{BHZ}*	–	5	–	6	nS

* These parameters are sampled but not 100% tested.

AC Characteristics, continued

(2) Write Cycle

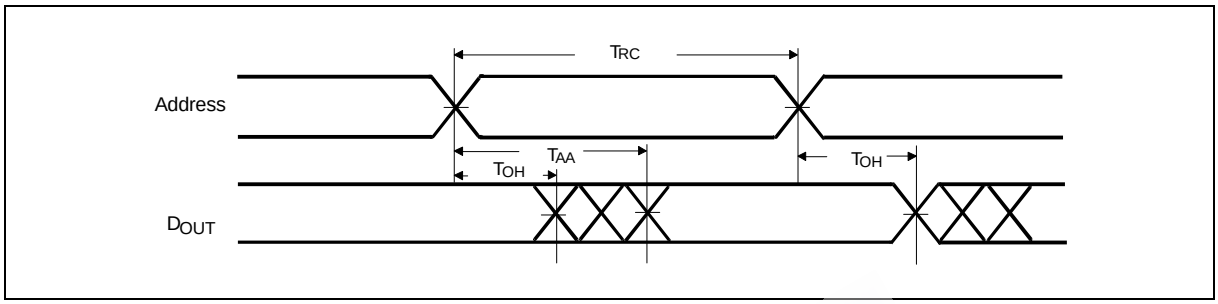
PARAMETER	SYM.	W26L010A-10		W26L010A-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	T_{WC}	10	–	12	–	nS
Chip Select to End of Write	T_{CW}	9	–	10	–	nS
Address Valid to End of Write	T_{AW}	9	–	10	–	nS
Address Setup Time	T_{AS}	0	–	0	–	nS
$\overline{UB}$, $\overline{LB}$ Select to End of Write	T_{BW}	9	–	10	–	nS
Write Pulse Width	T_{WP}	9	–	10	–	nS
Write Recovery Time ($\overline{CS}$, $\overline{WE}$)	T_{WR}	0	–	0	–	nS
Data Valid to End of Write	T_{DW}	6	–	7	–	nS
Data Hold from End of Write	T_{DH}	0	–	0	–	nS
Write to Output in High Z	T_{WHZ}*	–	6	–	7	nS
End of Write to Output Active	T_{OW}*	3	–	3	–	nS

* These parameters are sampled but not 100% tested.

Timing Waveforms

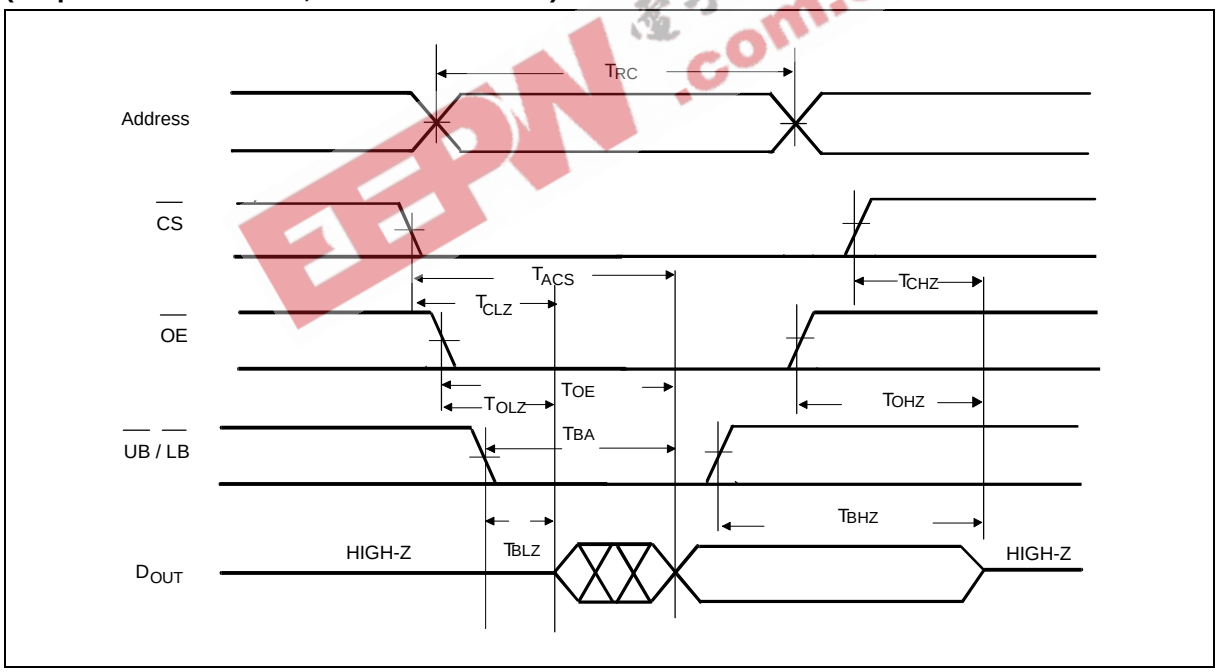
Read Cycle 1

(Address Controlled, $\overline{CS}$ = $\overline{OE}$ = $\overline{UB}$ = $\overline{LB}$ = VIL, $\overline{WE}$ = VIH)



Read Cycle 2

(Chip Select Controlled, $\overline{OE}$ = VIL, $\overline{WE}$ = VIH)



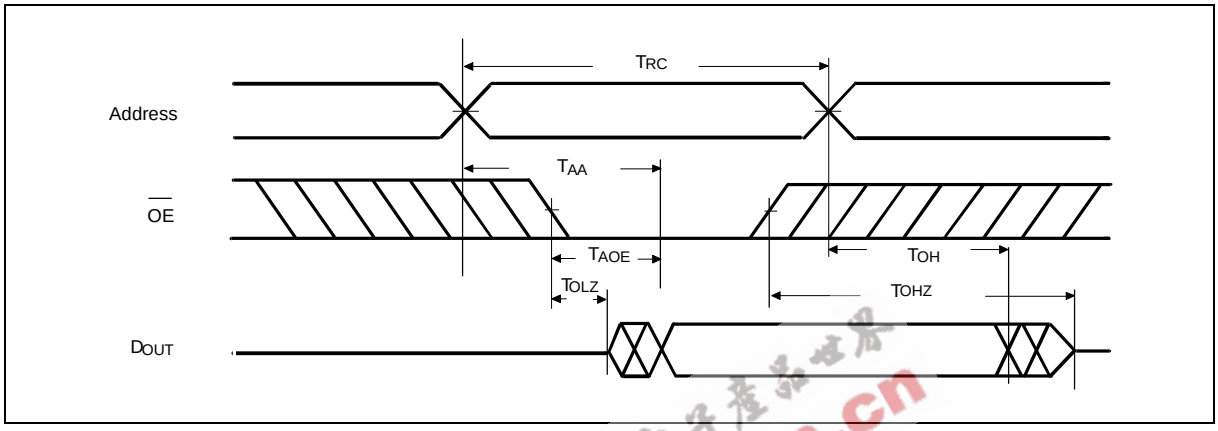
Notes:

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected.
   $\overline{CS}$ = $\overline{OE}$ = $\overline{LB}$ = Low
   $\overline{CS}$ = $\overline{OE}$ = $\overline{LB}$ = Low
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Timing Waveforms, continued

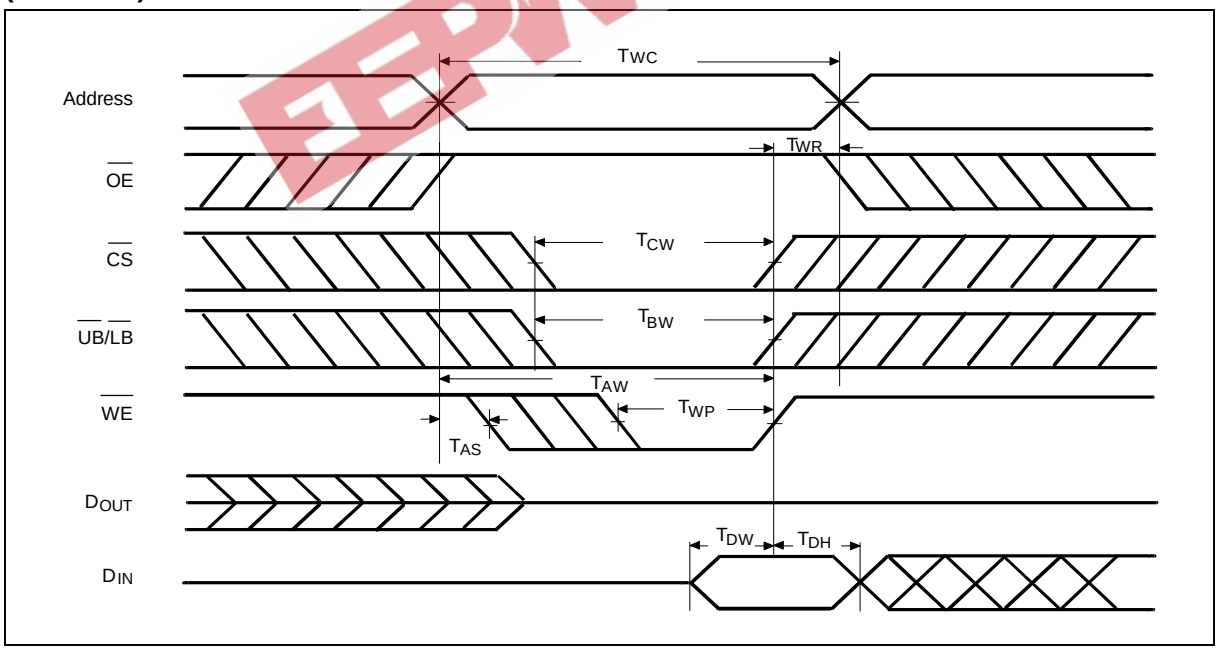
Read Cycle 3

(Output Enable Controlled, $\overline{CS}$ = $\overline{UB}$ = $\overline{LB}$ = VIL, $\overline{WE}$ = VIH)



Write Cycle 1

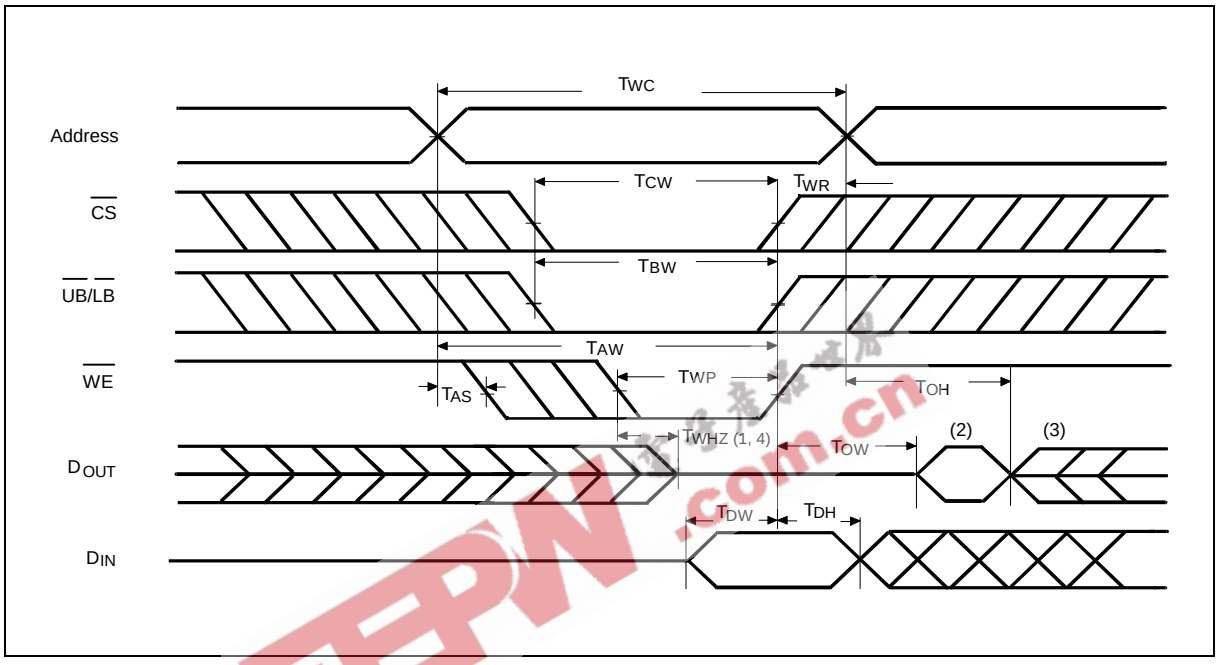
($\overline{OE}$ Clock)



Timing Waveforms, continued

Write Cycle 2

($\overline{OE}$ = V_{IL} Fixed)



Notes:
1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from D_{OUT} are the same as the data written to D_{IN} during the write cycle.
3. D_{OUT} provides the read data for the next address.
4. Transition is measured ±500 mV from steady state with C_L = 5 pF. This parameter is guaranteed but not 100% tested.

ORDERING INFORMATION

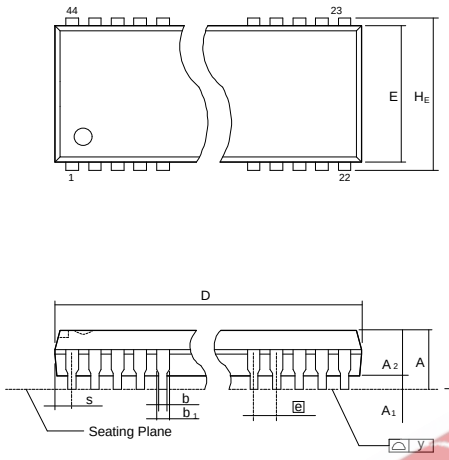
PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W26L010AJ-10	10	160	10	44-pin 400 mil SOJ
W26L010AJ-12	12	140	10	44-pin 400 mil SOJ
W26L010AT-10	10	160	10	44-pin TSOP
W26L010AT-12	12	140	10	44-pin TSOP

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

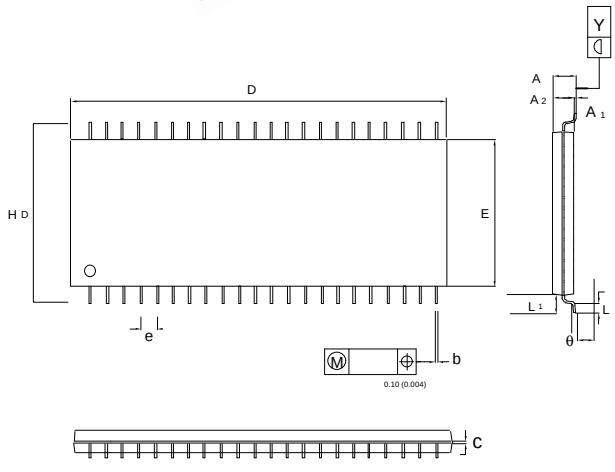
PACKAGE DIMENSIONS

44-pin Small Outline J Band



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.128	0.138	0.148	3.251	3.585	3.759
A_1	0.025	—	—	0.635	—	—
A_2	0.105	0.110	0.115	2.41	2.54	2.67
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.015	—	0.020	0.381	—	0.508
c	0.007	—	0.013	0.178	—	0.330
D	1.120	1.125	1.130	28.45	28.58	28.70
E	0.395	0.400	0.405	10.03	10.16	10.29
e	0.044	0.050	0.056	1.12	1.27	1.42
e_1	—	0.37	—	—	9.40	—
H_E	0.435	0.440	0.445	11.05	11.18	11.30
L	0.082	—	—	2.06	—	—
S	—	—	0.045	—	—	1.14
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

44-pin Standard Type Two TSOP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A_1	0.002	—	—	0.05	—	—
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.010	0.014	0.018	0.25	0.35	0.45
c	0.005	0.006	0.007	0.12	0.15	0.17
D	0.721	0.725	0.729	18.31	18.41	18.51
E	0.396	0.400	0.404	10.06	10.16	10.26
H_D	0.455	0.463	0.471	11.56	11.76	11.96
e	—	0.031	—	—	0.80	—
L	0.016	0.020	0.024	0.40	0.50	0.60
L_1	—	0.031	—	—	0.80	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	5°	0°	—	5°

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	May 1995		Initial Issued
A2	Feb. 1998	1, 3, 4, 5, 8	Change the relative specification from 15/20 nS to 10/12 nS
		1, 8, 9	Add TSOP package
		6, 7	Modify timing waveforms
A3	Jul. 1998	3, 4	Revise Vcc from 3.3V ±10% to 3.3V ±5%

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