Winbond Electronics Corp.

200MHZ 3-DIMM CLOCK FOR WHITNEY CHIPSET

1.0 GENERAL DESCRIPTION

The W83195AR-We is a Clock Synthesizer for Intel Solano chipset. W83195AR-We provides all clocks required for high-speed RISC or CISC microprocessor and also provides 64 different frequencies of CPU, SDRAM, PCI, 3V66, IOAPIC clocks frequency setting. All clocks are externally selectable with smooth transitions.

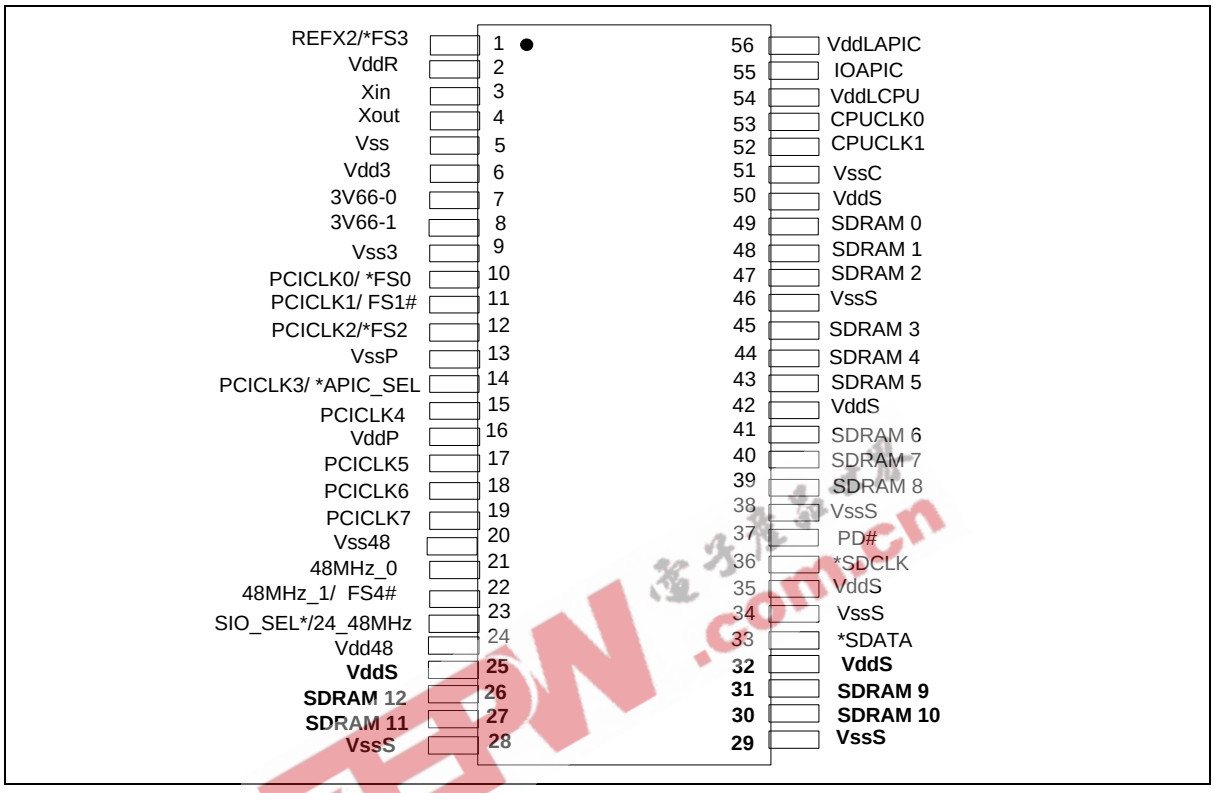
The W83195AR-We provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and provides 0.5% and 0.75% center type spread spectrum to reduce EMI.

The W83195AR-We accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI and SDRAM CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads as maintaining 50± 5% duty cycle. The fixed frequency outputs as REF, 24MHz, and 48 MHz provide better than 0.5V /ns slew rate.

2.0 PRODUCT FEATURES

- 2 CPU clocks
- 12 SDRAM clocks for 3 DIMMs
- 8 PCI synchronous clocks.
- Optional single or mixed supply:
  (VddR = VddP=VddS = Vdd48 = Vdd3 = 3.3V, VddLAPIC=VddLCPU=2.5V)
- Skew form CPU to PCI clock -1 to 4 ns, center 2.6 ns
- Smooth frequency switch with selections from 66.8 to 200 MHz
- I^2C 2-Wire serial interface and I^2C read back
- 0.5% and 0.75% center type spread spectrum
- Programmable registers to enable/stop each output and select modes
  (mode as Tri-state or Normal)
- Two 48 MHz pins for USB
- 24 MHz for super I/O
- 56-pin SSOP package

3.0 PIN CONFIGURATION



4.0 FREQUENCY SELECTION BY HARDWARE

SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	CPU (MHz)	SDRAM (MHz)	CPU /SDRAM	3V66 (MHz)	PCI(MHz)	IOAPIC (MHz) APIC_SEL=1	IOAPIC (MHz) APIC_SEL=0
0	0	0	0	0	83.3	124.95	**2/3**	83.30	41.65	20.83	41.65
0	0	0	0	1	90	90	1	60.00	30.00	15.00	30.00
0	0	0	1	0	75	112.5	**2/3**	75.00	37.50	18.75	37.50
0	0	0	1	1	**72**	**108**	**2/3**	**72.00**	36.00	18.00	36.00
0	0	1	0	0	**89.07**	**133.6**	**2/3**	**89.07**	44.53	22.27	44.53
0	0	1	0	1	95.25	95.25	1	63.50	31.75	15.88	31.75
0	0	1	1	0	121	121	1	80.67	40.33	20.17	40.33
0	0	1	1	1	124	124	1	82.67	41.33	20.67	41.33
0	1	0	0	0	119	119	1	79.33	39.67	19.83	39.67
0	1	0	0	1	114	114	1	76.00	38.00	19.00	38.00
0	1	0	1	0	110	110	1	73.33	36.67	18.33	36.67
0	1	0	1	1	105	105	1	70.00	35.00	17.50	35.00
0	**1**	**1**	**0**	**0**	**66.8**	**100.2**	**2/3**	66.80	33.40	16.70	33.40
0	**1**	**1**	**0**	**1**	**100.2**	**100.2**	**1**	66.80	33.40	16.70	33.40
0	**1**	**1**	**1**	**0**	**133.6**	**133.6**	**1**	66.80	33.40	16.70	33.40
0	**1**	**1**	**1**	**1**	**133.6**	**100.2**	**4/3**	66.80	33.40	16.70	33.40
1	0	0	0	0	135	101.25	4/3	67.50	33.75	16.88	33.75
1	0	0	0	1	125	125	1	83.33	41.67	20.83	41.67
1	0	0	1	0	127	127	1	84.67	42.33	21.17	42.33
1	0	0	1	1	130	130	1	86.67	43.33	21.67	43.33
1	0	1	0	0	140	140	1	70.00	35.00	17.50	35.00
1	0	1	0	1	136	136	1	68.00	34.00	17.00	34.00
1	0	1	1	0	166	166.00	1	83.00	41.50	20.75	41.50
1	0	1	1	1	155	155	1	77.50	38.75	19.38	38.75
1	1	0	0	0	**150**	**112.5**	**4/3**	**75.00**	**37.50**	**18.75**	**37.50**
1	1	0	0	1	117	117	1	78.00	39.00	19.50	39.00
1	1	0	1	0	107	107	1	71.33	35.67	17.83	35.67
1	1	0	1	1	100.9	100.9	1	67.27	33.63	16.82	33.63
1	1	1	0	0	**145**	**108.75**	**4/3**	**72.50**	36.25	18.13	36.25
1	1	1	0	1	**140**	**105**	**4/3**	**70.00**	35.00	17.50	35.00
1	1	1	1	0	**138**	**103.5**	**4/3**	**69.00**	34.50	17.25	34.50
1	1	1	1	1	**137**	**102.75**	**4/3**	**68.50**	34.25	17.13	34.25

5.0 SERIAL CONTROL 0REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up. Registers are set to the values shown only on true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2, ...) will be valid and acknowledged.

Frequency Table Setting by I2C (SEL5 ~ SEL0)

SSEL5	SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	CPU (MHz)	SDRAM (MHz)	CPU/SDRAM	3V66 (MHz)	PCI(MHz)	IOAPIC (MHz) APIC_SEL=1	IOAPIC (MHz) APIC_SEL=0
0	0	0	0	0	0	83.3	124.95	**2/3**	83.30	41.65	20.83	41.65
0	0	0	0	0	1	90	90	1	60.00	30.00	15.00	30.00
0	0	0	0	1	0	75	112.5	**2/3**	75.00	37.50	18.75	37.50
0	0	0	0	1	1	**72**	**108**	**2/3**	**72.00**	36.00	18.00	36.00
0	0	0	1	0	0	**89.07**	**133.6**	**2/3**	**89.07**	44.53	22.27	44.53
0	0	0	1	0	1	95.25	95.25	1	63.50	31.75	15.88	31.75
0	0	0	1	1	0	121	121	1	80.67	40.33	20.17	40.33
0	0	0	1	1	1	124	124	1	82.67	41.33	20.67	41.33
0	0	1	0	0	0	119	119	1	79.33	39.67	19.83	39.67
0	0	1	0	0	1	114	114	1	76.00	38.00	19.00	38.00
0	0	1	0	1	0	110	110	1	73.33	36.67	18.33	36.67
0	0	1	0	1	1	105	105	1	70.00	35.00	17.50	35.00
0	**0**	**1**	**1**	**0**	**0**	**66.8**	**100.2**	**2/3**	66.80	33.40	16.70	33.40
0	**0**	**1**	**1**	**0**	**1**	**100.2**	**100.2**	**1**	66.80	33.40	16.70	33.40
0	**0**	**1**	**1**	**1**	**0**	**133.6**	**133.6**	**1**	66.80	33.40	16.70	33.40
0	**0**	**1**	**1**	**1**	**1**	**133.6**	**100.2**	**4/3**	66.80	33.40	16.70	33.40
0	1	0	0	0	0	135	101.25	4/3	67.50	33.75	16.88	33.75
0	1	0	0	0	1	125	125	1	83.33	41.67	20.83	41.67
0	1	0	0	1	0	127	127	1	84.67	42.33	21.17	42.33
0	1	0	0	1	1	130	130	1	86.67	43.33	21.67	43.33
0	1	0	1	0	0	140	140	1	70.00	35.00	17.50	35.00
0	1	0	1	0	1	136	136	1	68.00	34.00	17.00	34.00
0	1	0	1	1	0	166	166.00	1	83.00	41.50	20.75	41.50
0	1	0	1	1	1	155	155	1	77.50	38.75	19.38	38.75
0	1	1	0	0	0	**150**	**112.5**	**4/3**	**75.00**	**37.50**	**18.75**	**37.50**
0	1	1	0	0	1	117	117	1	78.00	39.00	19.50	39.00
0	1	1	0	1	0	107	107	1	71.33	35.67	17.83	35.67
0	1	1	0	1	1	100.9	100.9	1	67.27	33.63	16.82	33.63
0	1	1	1	0	0	**145**	**108.75**	**4/3**	**72.50**	36.25	18.13	36.25
0	1	1	1	0	1	**140**	**105**	**4/3**	**70.00**	35.00	17.50	35.00
0	1	1	1	1	0	**138**	**103.5**	**4/3**	**69.00**	34.50	17.25	34.50

0	1	1	1	1	1	137	102.75	4/3	68.50	34.25	17.13	34.25

SSEL5	SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	CPU (MHz)	SDRAM (MHz)	CPU/SDRAM	3V66 (MHz)	PCI(MHz)	IOAPIC (MHz) APIC_SEL=1	IOAPIC (MHz) APIC_SEL=0
1	0	0	0	0	0	136	102.00	4/3	68.00	34.00	17.00	34.00
1	0	0	0	0	1	138	138.00	1	69.00	34.50	17.25	34.50
1	0	0	0	1	0	139	104.25	4/3	69.50	34.75	17.38	34.75
1	0	0	0	1	1	141	141.00	1	70.50	35.25	17.63	35.25
1	0	0	1	0	0	142	142.00	1	71.00	35.50	17.75	35.50
1	0	0	1	0	1	142	106.50	4/3	71.00	35.50	17.75	35.50
1	0	0	1	1	0	143	143.00	1	71.50	35.75	17.88	35.75
1	0	0	1	1	1	143	107.25	4/3	71.50	35.75	17.88	35.75
1	0	1	0	0	0	144	144.00	1	72.00	36.00	18.00	36.00
1	0	1	0	0	1	144	108.00	4/3	72.00	36.00	18.00	36.00
1	0	1	0	1	0	146	146	1	73.00	36.50	18.25	36.50
1	0	1	0	1	1	146	109.50	4/3	73.00	36.50	18.25	36.50
1	0	1	1	0	0	147	147	1	73.50	36.75	18.38	36.75
1	0	1	1	0	1	147	110.25	4/3	73.50	36.75	18.38	36.75
1	0	1	1	1	0	148	148.00	1	74.00	37.00	18.50	37.00
1	0	1	1	1	1	148	111.00	4/3	74.00	37.00	18.50	37.00
1	1	0	0	0	0	149	111.75	4/3	74.50	37.25	18.63	37.25
1	1	0	0	0	1	152	152.00	1	76.00	38.00	19.00	38.00
1	1	0	0	1	0	153	114.75	4/3	76.50	38.25	19.13	38.25
1	1	0	0	1	1	156	156.00	1	78.00	39.00	19.50	39.00
1	1	0	1	0	0	157	117.75	4/3	78.50	39.25	19.63	39.25
1	1	0	1	0	1	158	158.00	1	79.00	39.50	19.75	39.50
1	1	0	1	1	0	159	119.25	4/3	79.50	39.75	19.88	39.75
1	1	0	1	1	1	160	160.00	1	80.00	40.00	20.00	40.00
1	1	1	0	0	0	162	121.5	4/3	81.00	40.50	20.25	40.50
1	1	1	0	0	1	164	164.00	1	82.00	41.00	20.50	41.00
1	1	1	0	1	0	170	170.00	1	85.00	42.50	21.25	42.50
1	1	1	0	1	1	175	175	1	87.5	43.75	21.88	43.75
1	1	1	1	0	0	180	90	4/3	60	30	15	30
1	1	1	1	0	1	185	92.5	2	61.67	30.83	15.42	30.83
1	1	1	1	1	0	190	126.67	3/2	63.33	31.67	15.83	31.67

1	1	1	1	1	1	**200.4**	**133.60**	**3/2**	**66.80**	33.40	16.70	33.40

5.1 Register 0: Control Register

Bit	@PowerUp	Pin	Description
7	1	26	SDRAM12(Active / Inactive)
6	1	1	REF2X(Active / Inactive)
5	1	27	SDRAM11(Active / Inactive)
4	1	30	SDRAM10(Active / Inactive)
3	1	31	SDRAM9(Active / Inactive)
2	1	23	24/48MHz(Active / Inactive)
1	1	21,22	48MHz_0, 48MHz_1(Active / Inactive)
0	1	39	SDRAM8(Active / Inactive)

5.2 Register 1 : SDRAM Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	40	SDRAM7 (Active / Inactive)
6	1	41	SDRAM6 (Active / Inactive)
5	1	43	SDRAM5 (Active / Inactive)
4	1	44	SDRAM4 (Active / Inactive)
3	1	45	SDRAM3 (Active / Inactive)
2	1	47	SDRAM2 (Active / Inactive)
1	1	48	SDRAM1 (Active / Inactive)
0	1	49	SDRAM0 (Active / Inactive)

5.3 Register 2: PCI Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	19	PCICLK7 (Active / Inactive)
6	1	18	PCICLK6 (Active / Inactive)
5	1	17	PCICLK5 (Active / Inactive)
4	1	15	PCICLK4 (Active / Inactive)
3	1	14	PCICLK3 (Active / Inactive)
2	1	13	PCICLK2 (Active / Inactive)

1	1	11	PCICLK1 (Active / Inactive)
0	1	10	PCICLK0 (Active / Inactive)

5.4 Register 3: CPU Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	X	-	FS0#
6	1	7	3V66_0(Active / Inactive)
5	1	8	3V66_1(Active / Inactive)
4	X	-	FS1#
3	1	55	IOAPIC(Active/ Inactive)
2	1	44	CPUCLK1 (Active / Inactive)
1	1	43	CPUCLK0 (Active / Inactive)
0	X	-	FS2#

5.5 Register 4: Control Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	0	-	SSEL3 (Frequency table selection by software via I^2C)
6	0	-	SSEL2 (Frequency table selection by software via I^2C)
5	0	-	SSEL1 (Frequency table selection by software via I^2C)
4	0	-	SSEL0 (Frequency table selection by software via I^2C)
3	0	-	0 = Selection by hardware 1 = Selection by software I^2C - Bit (1,2, 4:6)
2	0	-	SSEL4 (Frequency table selection by software via I^2C)
1	0	-	SSEL5 (Frequency table selection by software via I^2C)
0	X	-	APIC_SEL#

5.6 Register 5: Control Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	0	-	0 = ±0.5% Center type Spread Spectrum Modulation 1 = ±0.75% Center type Spread Spectrum Modulation
6	1	-	SKEW2(SDRAM to CPU Skew programming bit)
5	0	-	SKEW1(SDRAM to CPU Skew programming bit)
4	0	-	SKEW0(SDRAM to CPU Skew programming bit)
3	X	-	FS3#

2	X	-	FS4#
1	0	-	0 = Normal 1 = Spread Spectrum enabled
0	0	-	Reserved

5.7 Register 6: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	1	-	Winbond Chip ID
6	0	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	1	-	Winbond Chip ID
3	1	-	Winbond Chip ID
2	0	-	Winbond Chip ID
1	0	-	Winbond Chip ID
0	0	-	Winbond Chip ID

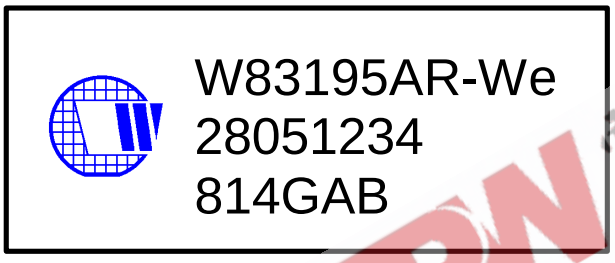
5.8 Register 7: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	0	-	Winbond Chip ID
5	1	-	Winbond Chip ID
4	1	-	Winbond Chip ID
3	0	-	Winbond Chip ID
2	0	-	Winbond Version ID
1	0	-	Winbond Version ID
0	1	-	Winbond Version ID

6.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83195AR-We	56 PIN SSOP	Commercial, 0°C to +70°C

7.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83195AR-We

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

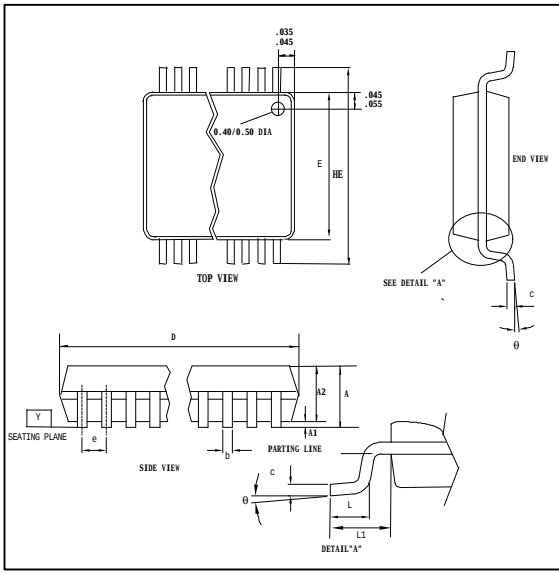
814: packages made in '98, week 14

G: assembly house ID; O means OSE, G means GR

A: Internal use code

B: IC revision

8.0 PACKAGE DRAWING AND DIMENSIONS



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	2.41	2.57	2.79	0.095	0.101	0.110
A1	0.20	0.30	0.41	0.008	0.012	0.016
A2	2.24	2.29	2.34	0.088	0.090	0.092
b	0.20	0.25	0.34	0.008	0.010	0.0135
c	0.13	—	0.25	0.005	—	0.010
D	18.2	18.42	18.54	0.720	0.725	0.730
H_E	10.16	10.31	10.41	0.400	0.406	0.410
E	7.42	7.52	7.59	0.292	0.296	0.299
e	0.51	0.64	0.76	0.020	0.025	0.030
L	0.61	0.81	1.02	0.024	0.032	0.040
L1	—	1.40	—	—	0.055	—
Y	—	—	0.08	—	—	0.003
q	0	—	8	0	—	8

Winbond Electronics Corp.

Headquarters
No. 4, Creation Rd. III
Science-Based Industrial Park
Hsinchu, Taiwan
TEL: 886-35-770066
FAX: 886-35-789467
www: http://www.winbond.com.tw/

Taipei Office
11F, No. 115, Sec. 3, Min-Sheng East Rd.
Taipei, Taiwan
TEL: 886-2-7190505
FAX: 886-2-7197502
TLX: 16485 WINTPE

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II
123 Hoi Bun Rd., Kwun Tong
Kowloon, Hong Kong
TEL: 852-27516023-7
FAX: 852-27552064

Winbond Electronics (North America) Corp.
2730 Orchard Parkway
San Jose, CA 95134 U.S.A.
TEL: 1-408-9436666
FAX: 1-408-9436668