2Mx32 5V Flash Module

FEATURES

- Access Time of 90, 120, 150ns
- Packaging:
  - 66 pin, PGA Type, 1.185" square, Hermetic Ceramic HIP (Package 401).
  - 68 lead, Hermetic CQFP (G2U), 22.4mm (0.880") square (Package 510) 3.56mm (0.140") height. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (FIGURE 3)
- Sector Architecture
  - 32 equal size sectors of 64KBytes per each 2Mx8 chip
  - Any combination of sectors can be erased. Also supports full chip erase.
- Minimum 100,000 Write/Erase Cycles Minimum
- Organized as 2Mx32
- Commercial, Industrial, and Military Temperature Ranges
- 5 Volt Read and Write. 5V ± 10% Supply.
- Low Power CMOS
- Data# Polling and Toggle Bit feature for detection of program or erase cycle completion.
- Supports reading or programming data to a sector not being erased.
- RESET# pin resets internal state machine to the read mode.
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation, Separate Power and Ground Planes to improve noise immunity

* This product is subject to change without notice.
Note: For programming information refer to Flash Programming 16M5 Application Note.

FIGURE 1 – PIN CONFIGURATION FOR WF2M32-XHX5

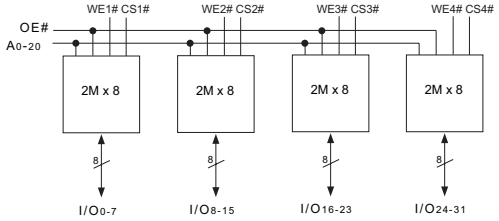
Top View

1	12	23	34	45	56
I/O8	WE2#	I/O15	I/O24	Vcc	I/O31
I/O9	CS2#	I/O14	I/O25	CS4#	I/O30
I/O10	GND	I/O13	I/O26	WE4#	I/O29
A14	I/O11	I/O12	A7	I/O27	I/O28
A16	A10	OE#	A12	A4	A1
A11	A9	A17	A20	A5	A2
A0	A15	WE1#	A13	A6	A3
A18	Vcc	I/O7	A8	WE3#	I/O23
I/O0	CS1#	I/O6	I/O16	CS3#	I/O22
I/O1	A19	I/O5	I/O17	GND	I/O21
I/O2	I/O3	I/O4	I/O18	I/O19	I/O20
11	22	33	44	55	66

Pin Description

I/O0-31	Data Inputs/Outputs
A0-20	Address Inputs
WE1-4#	Write Enables
CS1-4#	Chip Selects
OE#	Output Enable
VCC	Power Supply
GND	Ground

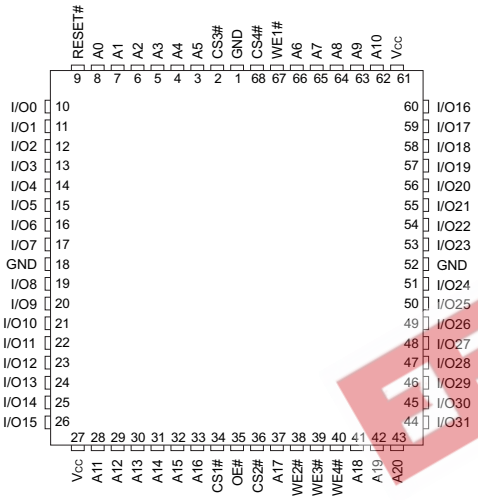
Block Diagram

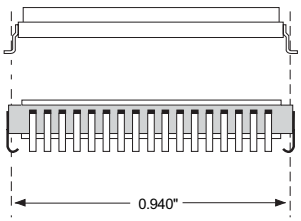


RESET# internally tied to Vcc in the HIP package for this pin configuration. See Alternate Pin Configuration with RESET# tied to pin 12 for system control of reset (FIGURE 10, page 11).

FIGURE 2 – PIN CONFIGURATION FOR WF2M32-XG2UX5

Top View

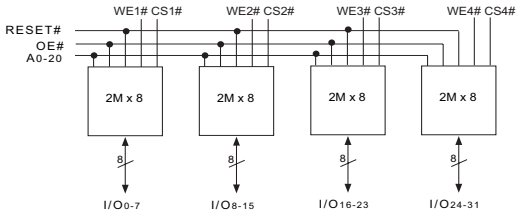




Pin Description

I/O0-31	Data Inputs/Outputs
A0-20	Address Inputs
WE1-4#	Write Enables
CS1-4#	Chip Selects
OE#	Output Enable
VCC	Power Supply
GND	Ground
RESET#	Reset

Block Diagram



The WEDC 68 lead G2U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2U has the TCE and lead inspection advantage of the CQFP form.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-2.0 to +7.0	V
Power Dissipation	P_T	8	W
Storage Temperature	T_{stg}	-65 to +125	°C
Short Circuit Output Current	I_{OS}	100	mA
Endurance – Write/Erase Cycles (Extended Temp)		100,000 min	cycles
Data Retention		20	years

CAPACITANCE

T_A = +25°C, f = 1.0MHz

Parameter	Symbol	Max	Unit
OE# capacitance	COE	50	pF
WE1-4# capacitance HIP (PGA)	CWE	20	pF
HIP (Alternate pinout)	CWE	50	pF
CQFP G4T	CWE	50	pF
CQFP G2U	CWE	20	pF
G2U (Alternate pinout)	CWE	50	pF
CS1-4# capacitance	CCS	20	pF
Data I/O capacitance	CI/O	20	pF
Address input capacitance	CAD	50	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.5	-	+0.8	V
Operating Temperature (Mil.)	T_A	-55	-	+125	°C
Operating Temperature (Ind.)	T_A	-40	-	+85	°C

DC CHARACTERISTICS – CMOS COMPATIBLE

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LOx32}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
V_{CC} Active Current for Read (1)	I_{CC1}	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz		160	mA
V_{CC} Active Current for Program or Erase (2)	I_{CC2}	CS# = V_{IL}, OE# = V_{IH}		240	mA
V_{CC} Standby Current	I_{CC3}	V_{CC} = 5.5, CS# = V_{IH}, f = 5MHz, RESET# = V_{CC} ± 0.3V		8.0	mA
Output Low Voltage	V_{OL}	I_{OL} = 12.0 mA, V_{CC} = 4.5		0.45	V
Output High Voltage	V_{OH}	I_{OH} = -2.5 mA, V_{CC} = 4.5	0.85xV_{CC}		V
Low V_{CC} Lock-Out Voltage	V_{LKO}		3.2	4.2	V

NOTES:
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 5MHz). The frequency component typically is less than 2mA/MHz, with OE# at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS - WE# CONTROLLED

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-90 Min	-90 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
Write Cycle Time	t_{AVAV}	t_{WC}	90		120		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	45		50		50		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		50		50		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase (2)	t_{WHWH2}			15		15		15	sec
Read Recovery Time before Write	t_{GHWL}		0		0		0		µs
V_{CC} Setup Time	t_{VCS}		50		50		50		µs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		t_{OEH}	10		10		10		ns
RESET# Pulse Width (5)		t_{RP}	500		500		500		ns

NOTES:
1. Typical value for t_{WHWH1} is 7µs.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.
5. RESET# internally tied to V_{CC} for the default pin configuration in the HIP package.

AC CHARACTERISTICS – READ-ONLY OPERATIONS

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-90 Min	-90 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
Read Cycle Time	t_{AVAV}	t_{RC}	90		120		150		ns
Address Access Time	t_{AVQV}	t_{ACC}		90		120		150	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		90		120		150	ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		40		50		55	ns
Chip Select High to Output High Z (1)	t_{EHQZ}	t_{DF}		20		30		35	ns
Output Enable High to Output High Z (1)	t_{GHQZ}	t_{DF}		20		30		35	ns
Output Hold from Addresses, CS# or OE# Change, whichever is First	t_{AXQX}	t_{OH}	0		0		0		ns
RST Low to Read Mode (1,2)		t_{Ready}		20		20		20	µs

NOTES:
1. Guaranteed by design, not tested.
2. RESET# internally tied to V_{CC} for the default pin configuration in the HIP package.

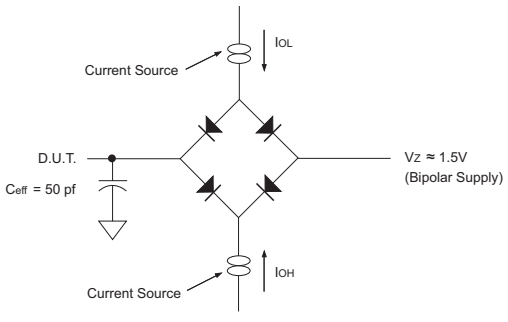
AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS,CS# CONTROLLED

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-90 Min	-90 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
Write Cycle Time	t_{AVAV}	t_{WC}	90		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase Time (2)	t_{WHWH2}			15		15		15	sec
Read Recovery Time	t_{GHEL}		0		0		0		µs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		t_{OEH}	10		10		10		ns

NOTES:
1. Typical value for tWHWH1 is 7µs.
2. Typical value for tWHWH2 is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

FIGURE 3 – AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75 ý.
VZ is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIGURE 4 – RESET TIMING DIAGRAM

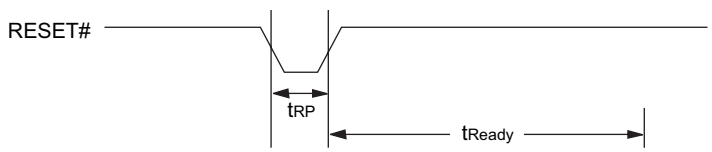


FIGURE 5 – AC WAVEFORMS FOR READ OPERATIONS

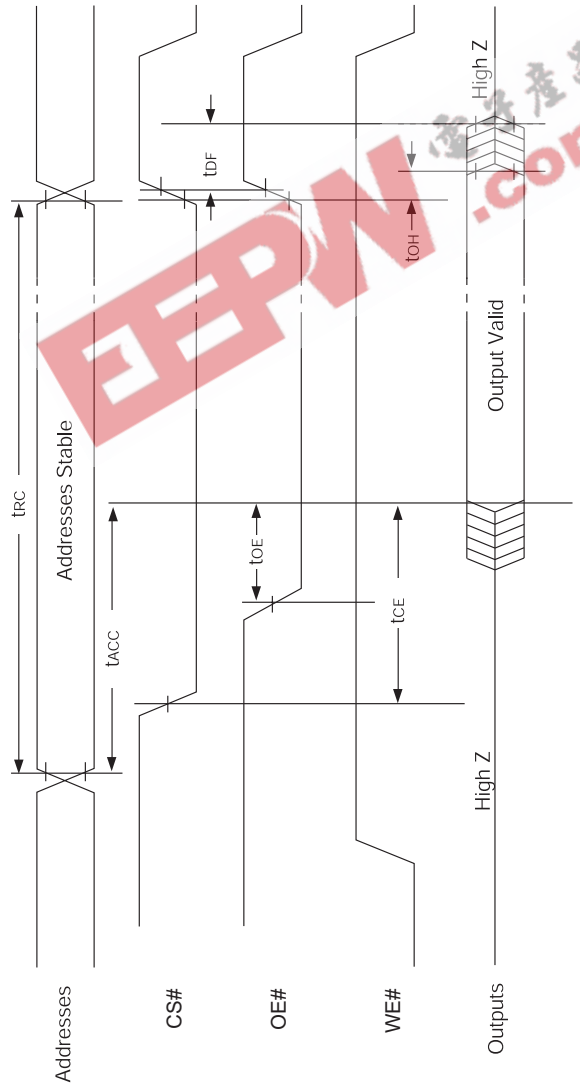
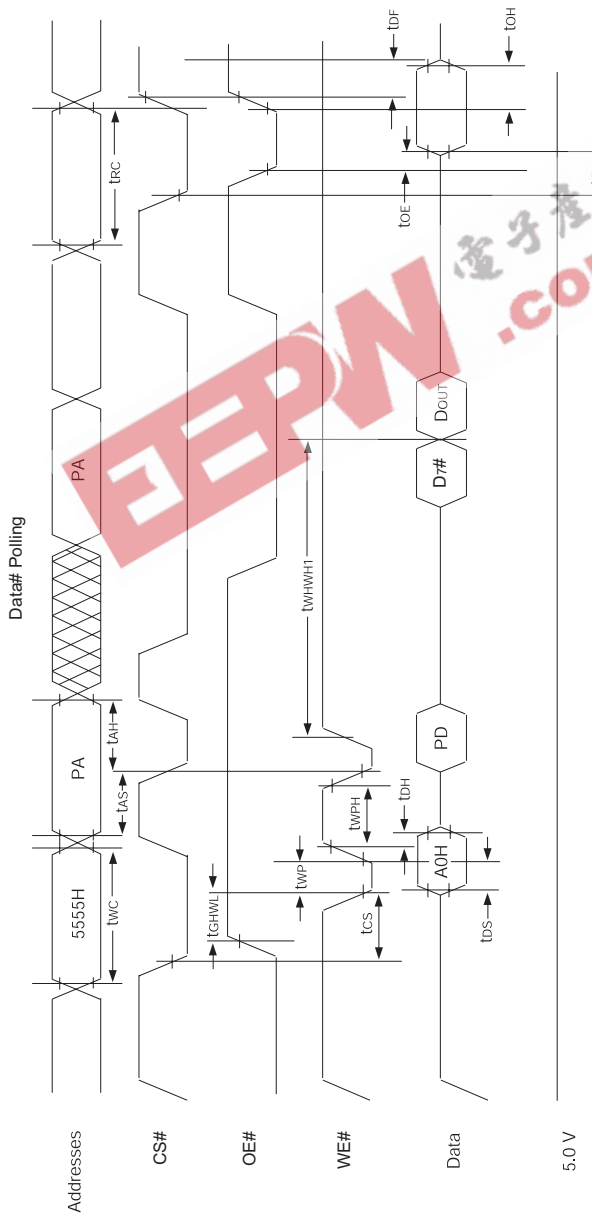


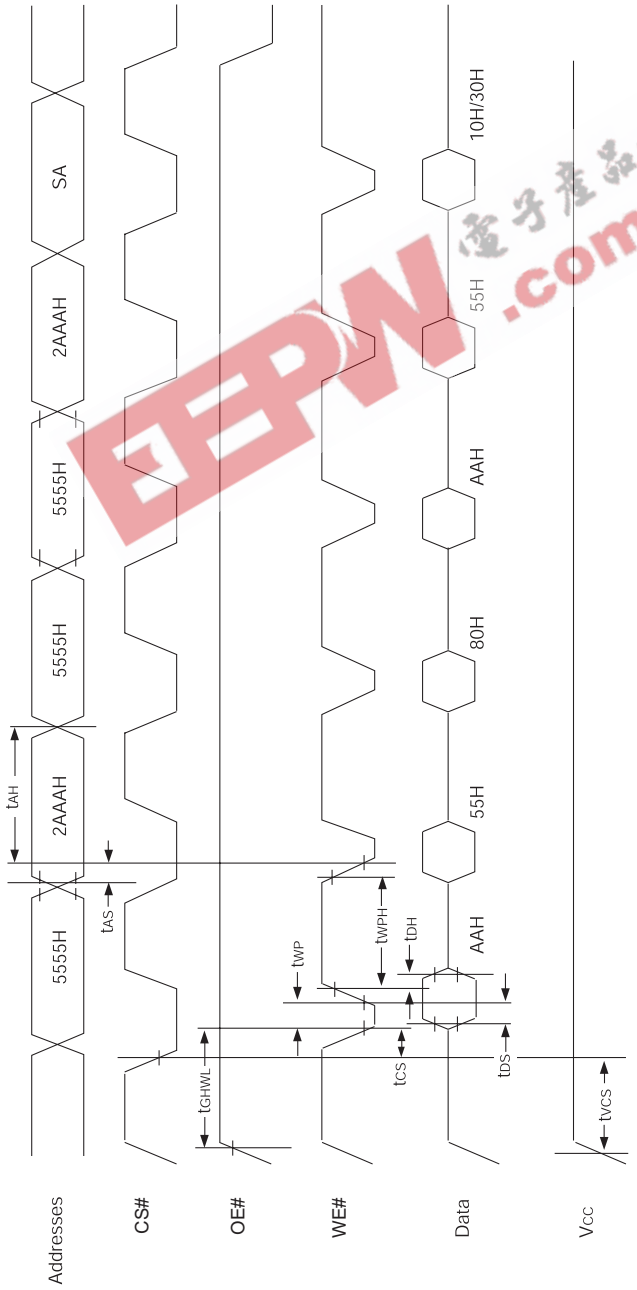
FIGURE 6 – WRITE/ERASE/PROGRAM OPERATION, WE# CONTROLLED



NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to each chip.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

FIGURE 7 – AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



NOTE:
1. SA is the sector address for Sector Erase.

FIGURE 8 – AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS

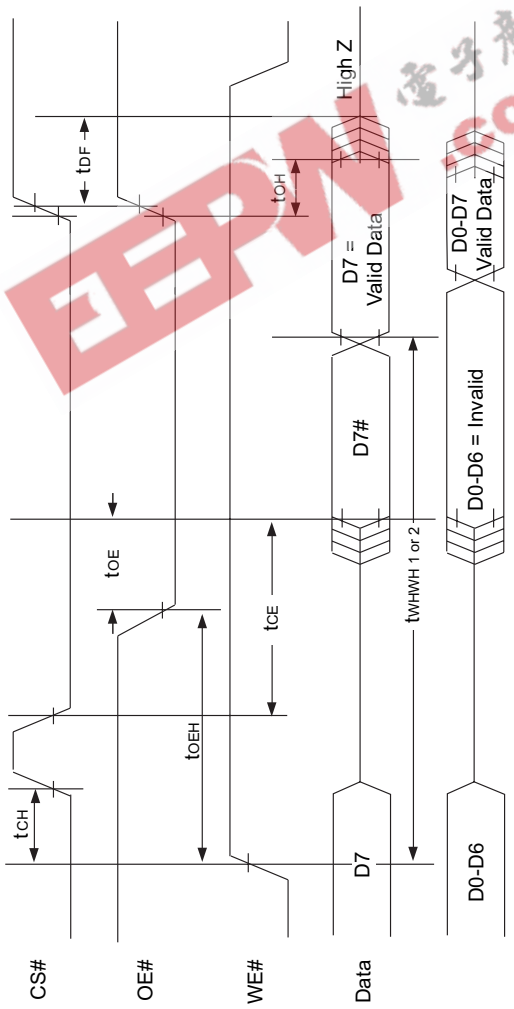
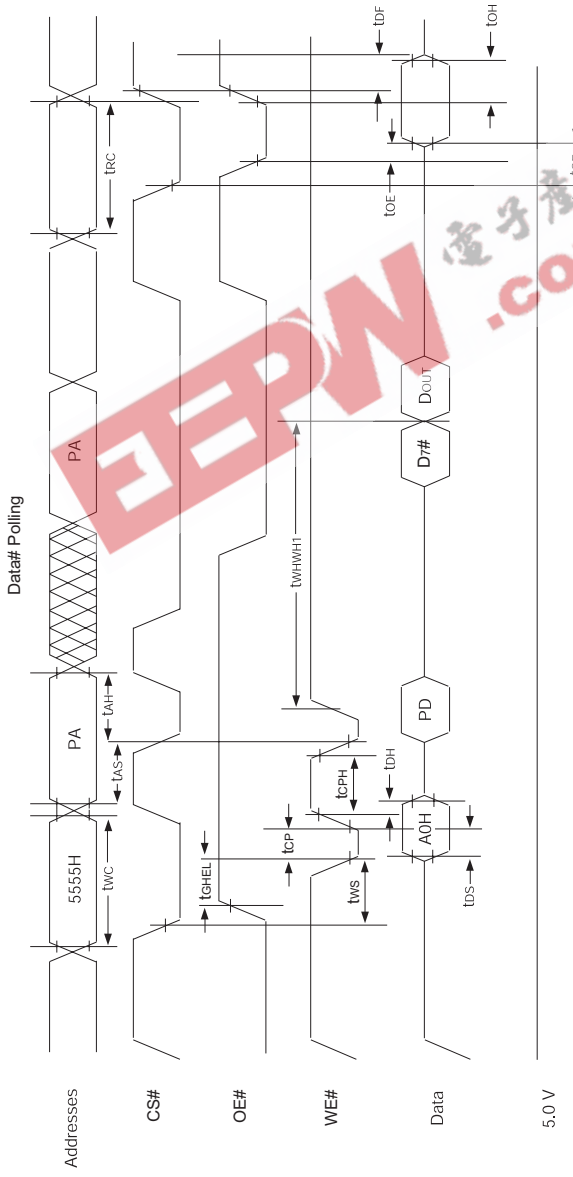


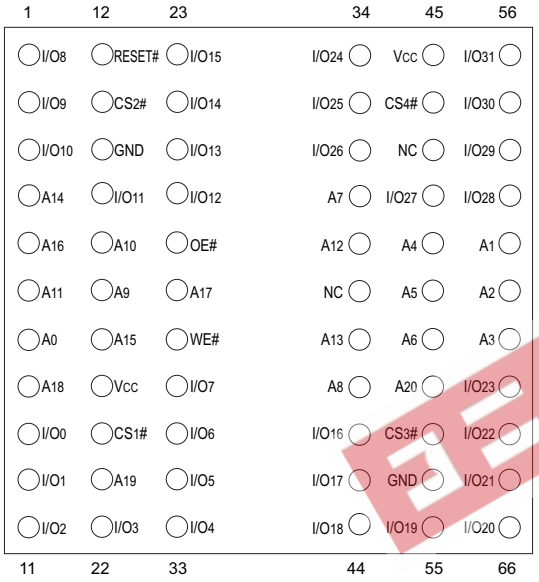
FIGURE 9 – ALTERNATE CS# CONTROLLED PROGRAMMING OPERATION TIMINGS



Notes:
1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to each chip.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

FIGURE 10 – ALTERNATE PIN CONFIGURATION FOR WF2M32I-XHX5

TOP VIEW



PIN DESCRIPTION

I/O_{0-31}	Data Inputs/Outputs
A_{0-20}	Address Inputs
WE#	Write Enable
CS_{1-4}#	Chip Selects
OE#	Output Enable
V_{CC}	Power Supply
GND	Ground
RESET#	Reset

BLOCK DIAGRAM

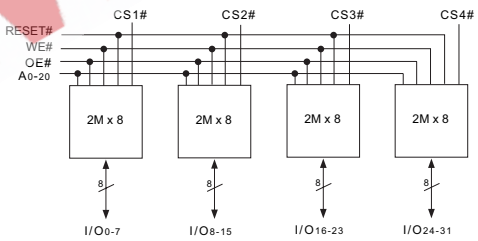
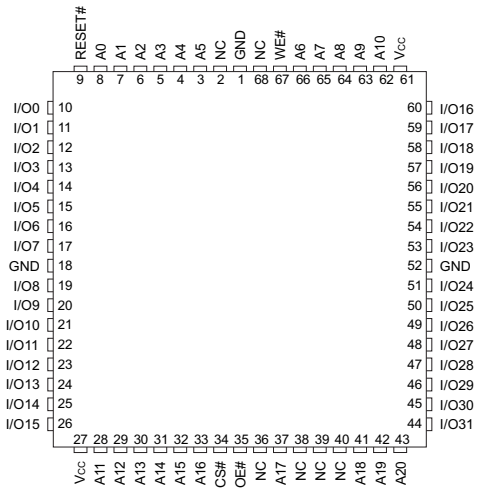
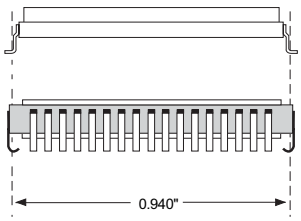


FIGURE 11 – ALTERNATE PIN CONFIGURATION FOR WF2M32U-XG2UX5

TOP VIEW





The WEDC 68 lead G2U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2U has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O_{0-31}	Data Inputs/Outputs
A_{0-20}	Address Inputs
WE#	Write Enable
CS#	Chip Select
OE#	Output Enable
V_{CC}	Power Supply
GND	Ground
RESET#	Reset

BLOCK DIAGRAM

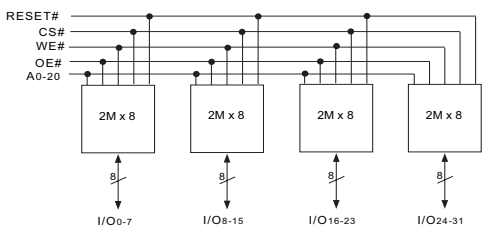
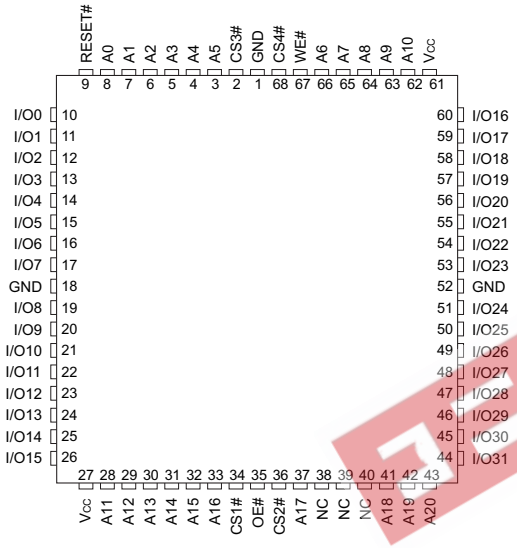


FIGURE 12 – PIN CONFIGURATION FOR WF2M32I-XG2UX5

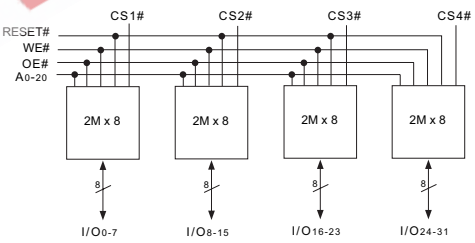
TOP VIEW

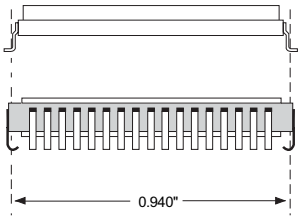


PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-20	Address Inputs
WE#	Write Enable
CS1-4#	Chip Selects
OE#	Output Enable
VCC	Power Supply
GND	Ground
RESET#	Reset

BLOCK DIAGRAM





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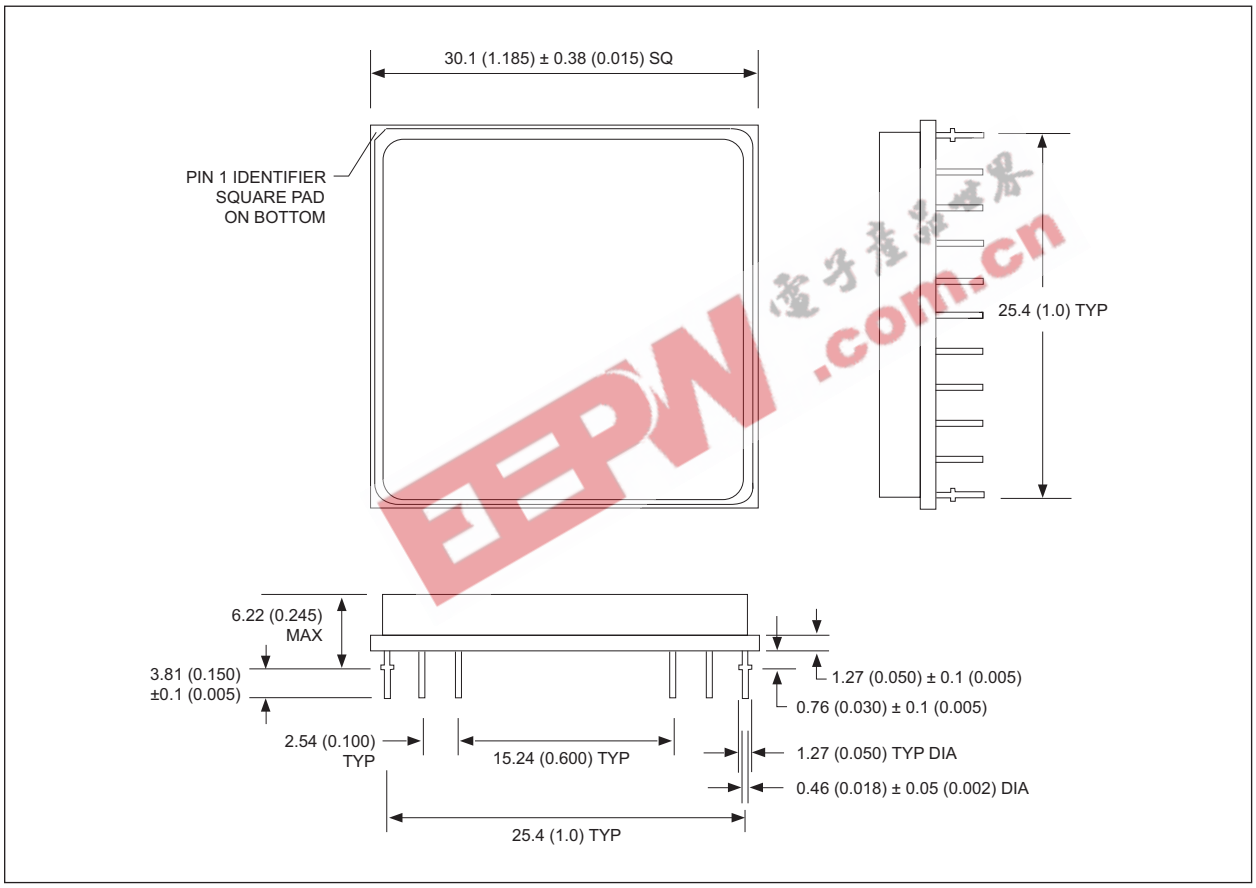
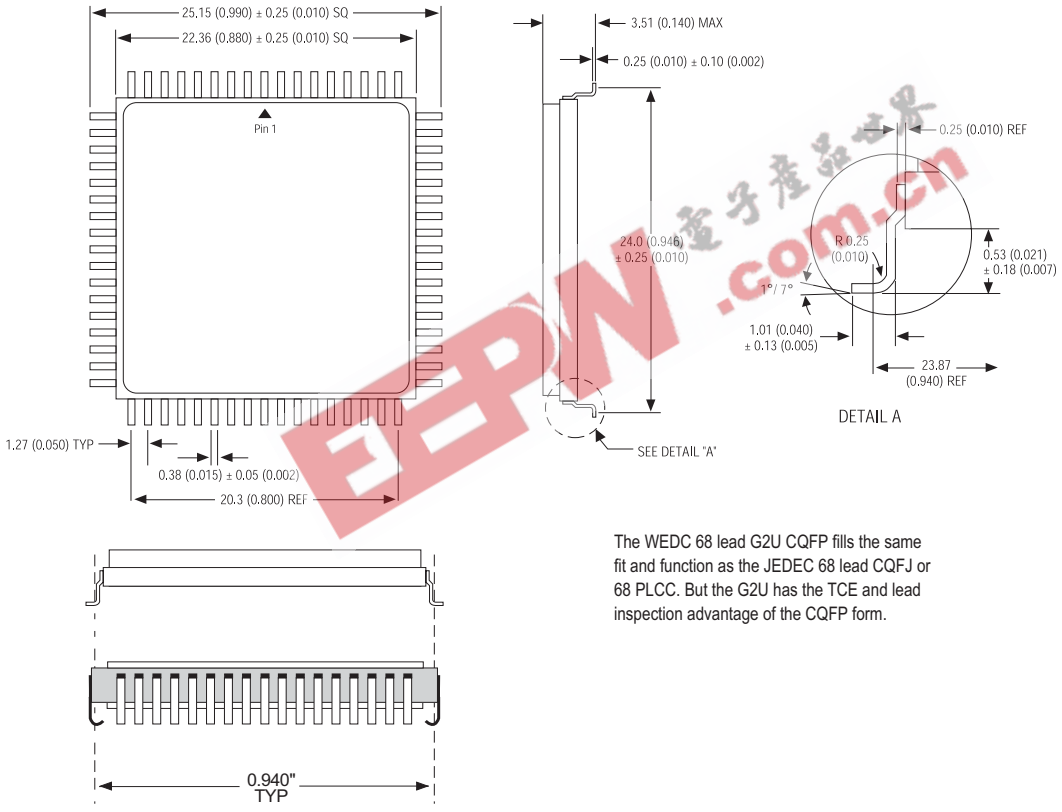
PACKAGE 401: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 510: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2U)



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ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W F 2M32 X - XXX X X 5 X

LEAD FINISH:
Blank = Gold plated leads
A = Solder dip leads

V_{PP} PROGRAMMING VOLTAGE
5 = 5 V

DEVICE GRADE:

Q	=	Compliant	-55°C to +125°C
M	=	Military	-55°C to +125°C
I	=	Industrial	-40°C to +85°C
C	=	Commercial	0°C to +70°C

PACKAGE TYPE:
H = Ceramic Hex In line Package, HIP (Package 401)
G2U = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 510)

ACCESS TIME (ns)

IMPROVEMENT MARK
• For HIP Package
Blank = 4CS# and 4WE#
I = 4CS# and 1WE#, RESET#
• For G2U Package
Blank = 4CS# and 4WE#
U = 1CS# and 1WE#
I = 4CS# and 1WE#, RESET#

ORGANIZATION, 2M x 32
User configurable as 4M x 16 or 8M x 8
(Except WF2M32U-XG2UX which is 32 bit wide only.)

Flash

WHITE ELECTRONIC DESIGNS CORP.