WHITE ELECTRONIC DESIGNS

512Kx32 Synchronous Pipeline Burst SRAM

*PRELIMINARY**

FEATURES

- Fast clock speed: 200, 166, 150 & 133MHz
- Fast access times: 2.5ns, 3.5ns, 3.8ns & 4.0ns
- Fast $\overline{OE}$ access times: 2.5ns, 3.5ns, 3.8ns 4.0ns
- Single +3.3V power supply (V_{DD})
- Separate +3.3V or +2.5V isolated output buffer supply (V_{DDQ})
- Snooze Mode for reduced-power standby
- Single-cycle deselect
- Common data inputs and data outputs
- Individual Byte Write control and Global Write
- Clock-controlled and registered addresses, data I/Os and control signals
- Burst control (interleaved or linear burst)
- Packaging:
  - 119-bump BGA package
- Low capacitive bus loading

DESCRIPTION

The WEDC SyncBurst - SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process. WEDC's 16Mb SyncBurst SRAMs integrate two 512K x 16 SRAMs into a single BGA package to provide 512K x 32 configuration. All synchronous inputs pass through registers controlled by a positive-edge-triggered single-clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable ($\overline{CE}$), burst control input ($\overline{ADSC}$) and byte write enables ($\overline{BW}_{0-3}$). Asynchronous inputs include the output enable ($\overline{OE}$), clock (CLK) and snooze enable (ZZ). There is also a burst mode input (MODE) that selects between interleaved and linear burst modes. Write cycles can be from one to four bytes wide, as controlled by the write control inputs. Burst operation can be initiated with the address status controller ($\overline{ADSC}$) input.

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

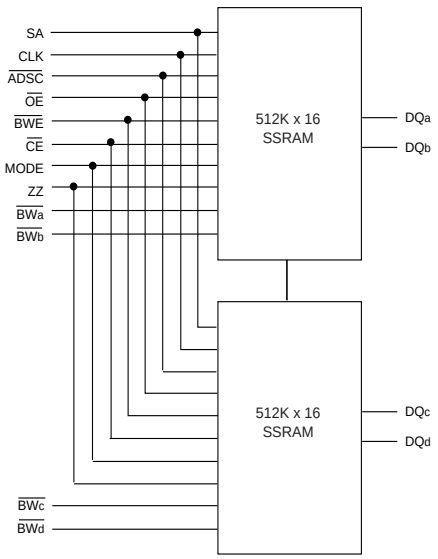
FIG. 1 PIN CONFIGURATION

(TOP VIEW)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	SA	SA	$\overline{ADSC}$	SA	SA	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	NC	V_{SS}	NC	V_{SS}	NC	DQb
E	DQc	DQc	V_{SS}	$\overline{CE}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{OE}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{BWc}$	NC	$\overline{BWb}$	DQb	DQb
H	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{BWd}$	NC	$\overline{BWa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{BWE}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA1	V_{SS}	DQa	DQa
P	DQd	NC	V_{SS}	SA0	V_{SS}	NC	DQa
R	NC	SA	MODE	V_{DD}	NC	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	DC	DC	DC	DC	NC	V_{DDQ}

NOTE: DC = Do Not Connect

BLOCK DIAGRAM



PIN DESCRIPTION

x36	Symbol	Type	Description
CLK	Input	Pulse	The system clock input. All of the SSRAM inputs are sampled on the rising edge of the clock.
4P 4N 2A, 2C, 2R, 2B 3A, 3B, 3C, 3T 4T, 5A, 5B, 5C, 5T, 6A, 6B, 6C, 6R	SA_0 SA_1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
5L 5G 3G 3L	$\overline{BWa}$ $\overline{BWb}$ $\overline{BWc}$ $\overline{BWd}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BWa}$ controls DQa's and DQPa; $\overline{BWb}$ controls DQb's and DQPb; $\overline{BWc}$ controls DQc's and DQPc; $\overline{BWd}$ controls DQd's and DQPd.
4M	$\overline{BWE}$	Input	Byte Write Enable: This active LOW input permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK.
4K	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
4E	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of $\overline{ADSP}$. $\overline{CE}$ is sampled only when a new external address is loaded.
7T	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When active, all other inputs are ignored.
4F	$\overline{OE}$	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers.
4B	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if $\overline{CE}$ is LOW. $\overline{ADSC}$ is also used to place the chip into power-down state when $\overline{CE}$ is HIGH.
3R	MODE	Input	Mode: This input selects the burst sequence. A LOW on MODE selects "linear burst." NC or HIGH on this input selects "interleaved burst." Do not alter input state while device is operating.
(a) 6K, 6L, 6M, 6N, 7K, 7L, 7N, 7P (b) 6E, 6F, 6G, 6H, 7D, 7E, 7G, 7H (c) 1D, 1E, 1G, 1H 2E, 2F, 2G, 2H (d) 1K, 1L, 1N, 1P, 2K, 2L, 2M, 2N	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: Byte "a" is DQa's; Byte "b" is DQb's; Byte "c" is DQc's; Byte "d" is DQd's. Input data must meet setup and hold times around rising edge of CLK.
2J, 4C, 4J, 4R, 5R, 6J	V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
1A, 1F, 1J, 1M 1U 7A, 7F, 7J, 7M, 7U	V_{DDQ}	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
3D, 3E, 3F, 3H, 3K, 3M, 3N, 3P, 5D, 5E, 5F, 5H, 5K, 5M, 5N, 5P	V_{SS}	Supply	Ground: GND.
2U	TMS	Input	Scan Test Mode Select
3U	TDI	Input	Scan Test Data In
4U	TDO	Output	Scan Test Data Out
5U	TCK	Input	Scan Test Clock

INTERLEAVED BURST TABLE (MODE = NC OR HIGH)

First Address External	Second Address Internal	Third Address Internal	Fourth Address Internal
X...X00	X...X01	X...X10	X...X11
X...X01	X....X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

INTERLEAVED BURST TABLE (MODE = LOW)

First Address External	Second Address Internal	Third Address Internal	Fourth Address Internal
X...X00	X...X01	X...X10	X...X11
X...X01	X....X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

TRUTH TABLE

Function	Address Used	$\overline{CE}$	ZZ	$\overline{ADSC}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-Down	None	H	L	L	X	X	L-H	High-Z
Deselected Cycle, Power-Down	None	L	L	L	X	X	L-H	High-Z
SNOOZE MODE, Power-Down	None	X	H	X	X	X	X	High-Z
WRITE Cycle, Begin Burst	External	L	L	L	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	L	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	L	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	X	L	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	L	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	L	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	L	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	L	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	L	H	L	X	L-H	D

NOTES:
1. X means "Don't Care." — means active LOW. H means logic HIGH. L means logic LOW.
2. For $\overline{WRITE}$, L means any one or more byte write enable signals ($\overline{BWa}$, $\overline{BWb}$, $\overline{BWc}$ or $\overline{BWd}$) and $\overline{BWE}$ are LOW.
3. $\overline{BWa}$ enables WRITEs to DQa's and DQPa. $\overline{BWb}$ enables WRITEs to DQb's. $\overline{BWc}$ enables WRITEs to DQc's. $\overline{BWd}$ enables WRITEs to DQd's.
4. All inputs except $\overline{OE}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, $\overline{OE}$ must be HIGH before the input data setup time and held HIGH throughout the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.

PARTIAL TRUTH TABLE - WRITE COMMANDS

Function	$\overline{BWE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$
Read	H	X	X	X	X
Read	L	H	H	H	H
Write Byte "a"	L	L	H	H	H
Write All Bytes	L	L	L	L	L

NOTE: Using $\overline{BWE}$ and $\overline{BWa}$ through $\overline{BWd}$, any one or more bytes may be written.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply relative to V_{SS}	-0.5V to +4.6V
Voltage on V_{DDQ} Supply relative to V_{SS}	-0.5V to +4.6V
V_{IN} (DQx)	-0.5V to V_{DDQ} +0.5V
V_{IN} (Inputs)	-0.5V to V_{DD} +0.5V
Storage Temperature (BGA)	-55°C to +125°C
Short Circuit Output Current	100 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS

Description	Symbol	Conditions	Min	Max	Units	Notes
Input High (Logic 1)Voltage	V_{IH}		2.0	V_{DD} +0.3	V	1
Input Low (Logic 0) Voltage	V_{IL}		-0.3	0.8	V	1
Input Leakage Current	I_{LI}	$0V \le V_{IN} \le V_{DD}$	-1.0	1.0	mA	2
Ouptut Leakage Current	I_{LO}	Output(s) disabled, $0V \le V_{IN} \le V_{DD}$	-1.0	1.0	mA	
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4	—	V	1
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA	—	0.4	V	1
Supply Voltage	V_{DD}		3.135	3.6	V	1
Isolated Output Buffer SupplyV_{DDQ}		3.134	3.6	V		

NOTES:
1. All voltages referenced to Vss (GND).
2. MODE has an internal pull-up, and input leakage = ±10µA.

DC CHARACTERISTICS

Description	Symbol	Conditions	Typ	200* MHz	166 MHz	150 MHz	133 MHz	Units	Notes
Power Supply Current: Operating	I_{DD}	Device selected; All inputs ≤ V_{IL} or 3 V_{IH}; Cycle time 3 t_{KC} MIN; V_{DD} = MAX; Outputs open		950	800	740	600	mA	1,2,3
CMOS Standby	I_{SB2}	Device deselected; V_{DD} = MAX; All inputs ≤ V_{SS} + 0.2 or V_{DD} - 0.2; All inputs static; CLK frequency = 0	10	20	20	20	20	mA	2,3
TTL Standby	I_{SB3}	Device deselected; V_{DD} = MAX; All inputs ≤ V_{IL} or V_{IH}; All inputs static; CLD frequency = 0	20	40	40	40	40	mA	2,3
Clock Running	I_{SB4}	Device deselected; V_{DD} = MAX; All inputs ≤ V_{SS} + 0.2 or V_{DD} -0.2; Cycle time 3 t_{KC} MIN	80	220	180	160	140	mA	2,3

** Advanced Information*

NOTES:
1. I_{DD} is specified with no output current and increases with faster cycle times. IDD increases with faster cycle times and greater output loading.
2. "Device deselected" means device is in power-down mode as defined in the truth table. "Device selected" means device is active (not in power-down mode).
3. Typical values are measured at 3.3V, 25°C and 133MHz.

BGA CAPACITANCE

Description	Conditions	Symbol	Typ	Max	Units	Notes
Control Input Capacitance	T_A = 25°C; f = 1MHz	C_I	3	6	pF	1
Input/Output Capacitance (DQ)	T_A = 25°C; f = 1MHz	C_O	4	5	pF	1
Address Capacitance	T_A = 25°C; f = 1MHz	C_A	3	5	pF	1
Clock Capacitance	T_A = 25°C; f = 1MHz	C_{CK}	2.5	4	pF	1

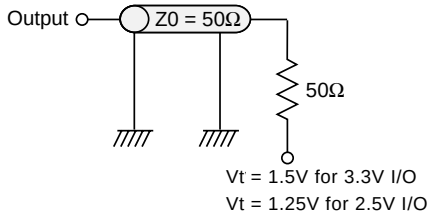
NOTES:
1. This parameter is sampled.

AC CHARACTERISTICS

Parameter	Symbol	200MHz		166MHz		150MHz		133MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock										
Clock Cycle Time	t_{KC}	5.0		6.0		6.6		7.5		ns
Clock Frequency	t_{KF}		200		166		150		133	MHz
Clock HIGH Time	t_{KH}	2.0		2.4		2.6		2.6		ns
Clock LOW Time	t_{KL}	2.0		2.4		2.6		2.6		ns
Output Times										
Clock to output valid	t_{KQ}		2.5		3.5		3.8		4.0	ns
Clock to output invalid (2)	t_{KQX}	1.5		1.25		1.25		1.5		ns
Clock to output on Low-Z (2,3,4)	t_{KQLZ}	0		0		0		0		ns
Clock to output in High-Z (2,3,4)	t_{KQHZ}		3.0		3.5		3.8		4.0	ns
$\overline{OE}$ to output valid (5)	t_{OEQ}		2.5		3.5		3.8		4.0	ns
$\overline{OE}$ to output in Low-Z (2,3,4)	t_{OELZ}	0		0		0		0		ns
$\overline{OE}$ to output in High Z (2,3,4)	t_{OEHZ}		2.5		3.5		3.8		4.0	ns
Setup Times										
Address (6,7)	t_{AS}	1.5		1.5		1.5		1.5		ns
Address status ($\overline{ADSC}$) (6,7)	t_{ADSS}	1.5		1.5		1.5		1.5		ns
Write signals ($\overline{BWa}$-$\overline{BWd}$, $\overline{BWE}$) (6,7)	t_{WS}	1.5		1.5		1.5		1.5		ns
Data-in (6,7)	t_{DS}	1.5		1.5		1.5		1.5		ns
Chip enables ($\overline{CE}$) (6,7)	t_{CES}	1.5		1.5		1.5		1.5		ns
Hold Times										
Address (6,7)	t_{AH}	0.5		0.5		0.5		0.5		ns
Address status ($\overline{ADSC}$) (6,7)	t_{ADSH}	0.5		0.5		0.5		0.5		ns
Write Signals ($\overline{BWa}$-$\overline{BWd}$, $\overline{BWE}$) (6,7)	t_{WH}	0.5		0.5		0.5		0.5		ns
Data-in (6,7)	t_{DH}	0.5		0.5		0.5		0.5		ns
Chip Enables ($\overline{CE}$) (6,7)	t_{CEH}	0.5		0.5		0.5		0.5		ns

NOTES:
1. Test conditions as specified with the output loading as shown in Figure 1 for 3.3V 1/0 and Figure 3 for 2.5V 1/0 unless otherwise noted.
2. This parameter is measured with output load as shown in Figure 2 for 3.3V 1/0 and Figure 4 for 2.5V 1/0.
3. This parameter is sampled.
4. Transition is measured ±500mV from steady state voltage.
5. $\overline{OE}$ is a "Don't Care" when a byte write enable is sampled LOW.
6. A WRITE cycle is defined by at least one byte write enable LOW for the required setup and hold times. A READ cycle is defined by all byte write enables HIGH and $\overline{ADSC}$ LOW for the required setup and hold times.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when $\overline{ADSC}$ is LOW to remain enabled.

OUTPUT LOADS



AC Output Load Equivalent

AC TEST CONDITIONS

Parameter	3.3V I/O	2.5V I/O	Unit
Input Pulse Levels	V_{SS} to 3.0	V_{SS} to 2.5	V
Input Rise and Fall Times	1	1	ns
Input Timing Reference Levels	1.5	1.25	V
Output Timing Reference Levels	1.5	1.25	V
Output Load	See figure, at left		

SNOOZE MODE

SNOOZE MODE is a low-current, "power-down" mode In which the device is deselected and current is reduced to I_{SB2Z}. The duration of SNOOZE MODE is dictated by the length of time ZZ is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored. ZZ is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When ZZ becomes a logic HIGH, I_{SB2Z} is guaranteed after the setup time t_{ZZ} is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

SNOOZE MODE

Description	Conditions	Symbol	Min	Max	Units	Notes
Current during SNOOZE MODE	ZZ ≥ VIH	I_{SB2Z}		10	mA	
ZZ active to input ignored		t_{ZZ}		2(t_{KC})	ns	1
ZZ inactive to input sampled		t_{RZZ}	2(t_{KC})		ns	1
ZZ active to snooze current		t_{ZZI}		2(t_{KC})	ns	1
ZZ inactive to exit snooze current		t_{RZZI}			ns	1

FIG. 2 SNOOZE MODE TIMING DIAGRAM

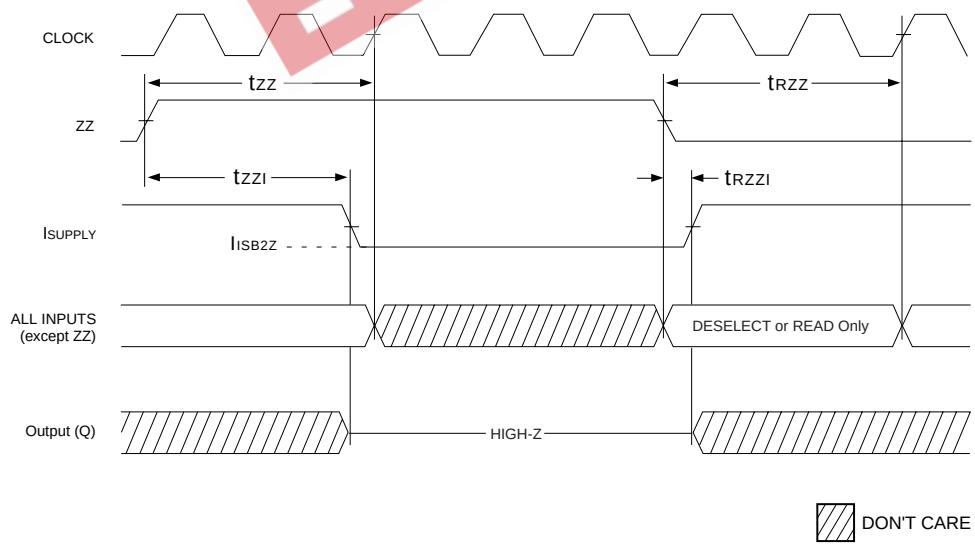
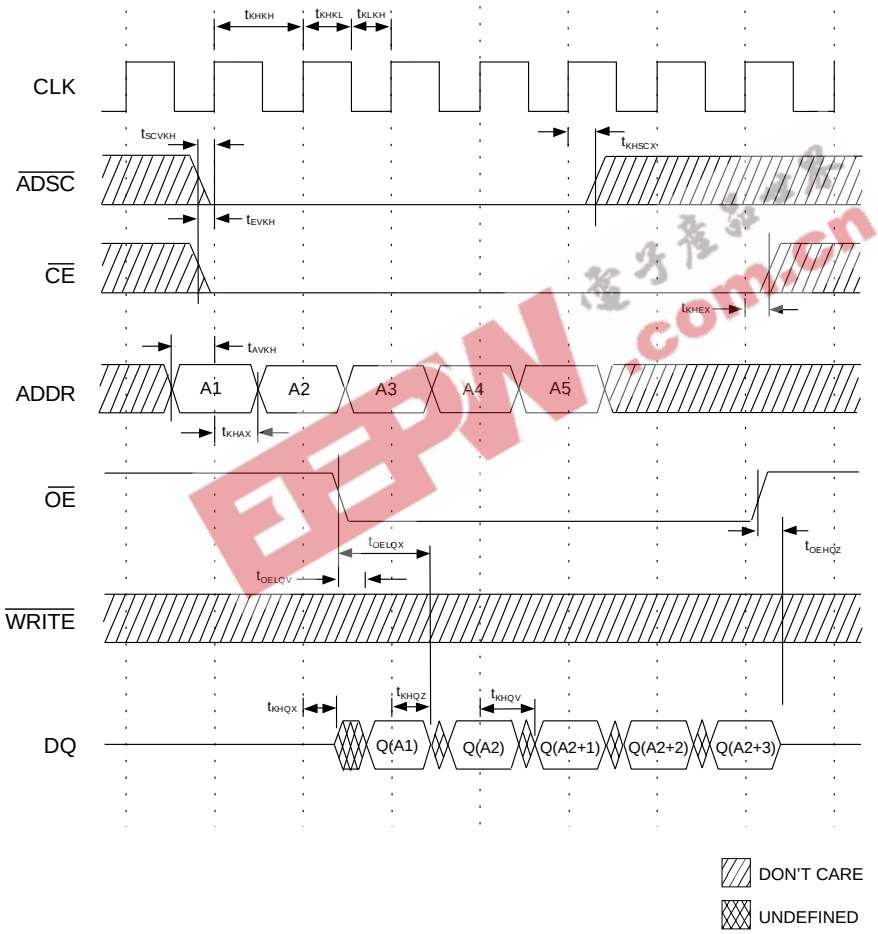
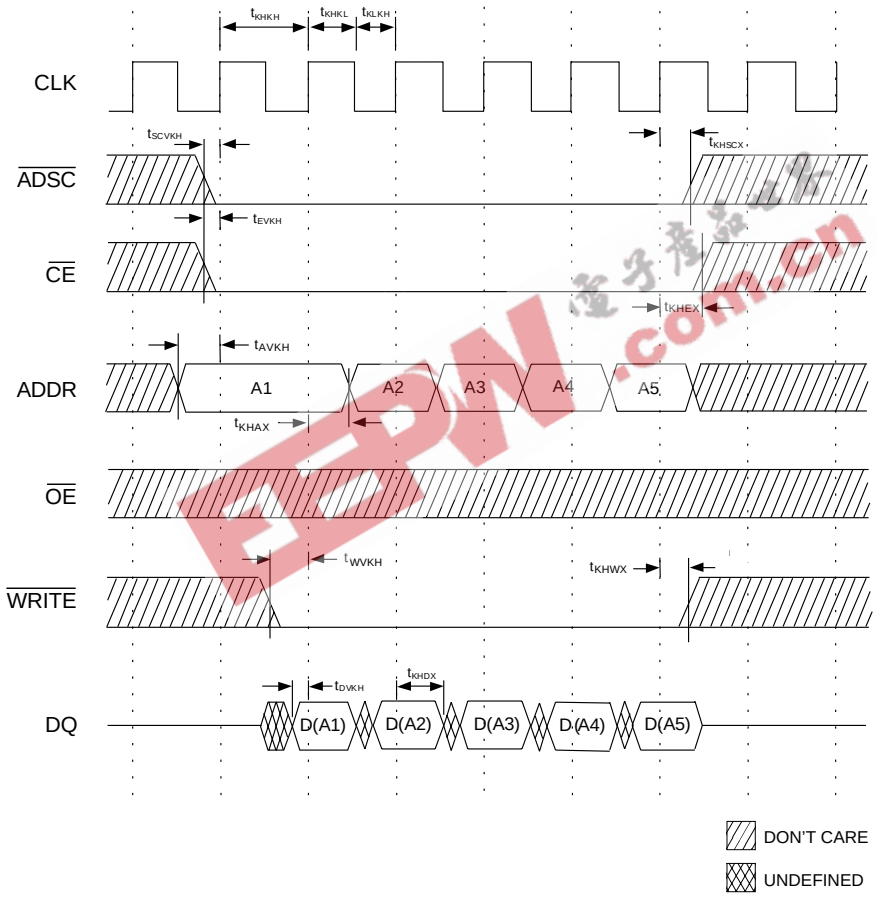


FIG. 3 READ TIMING DIAGRAM



NOTES:
1. Q (A2) refers to output from address A2. Q (A2+1) refers to output from the next internal burst address following A2.

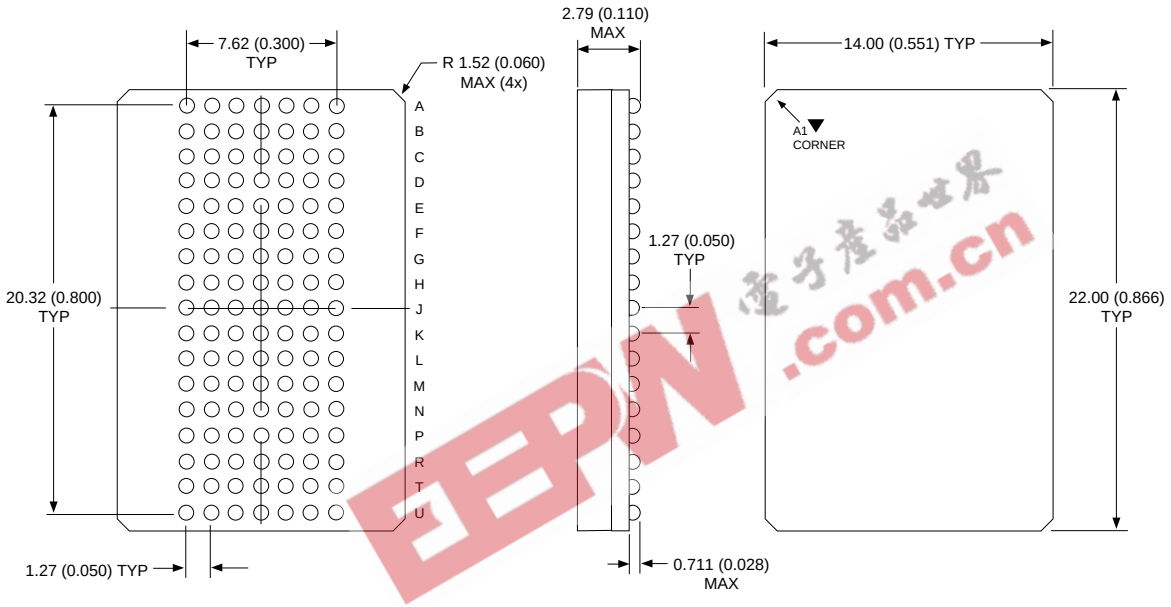
FIG. 4 WRITE TIMING DIAGRAM



NOTES:

1. D (A2) refers to output from address A2. D (A2+1) refers to output from the next internal burst address following A2.
2. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data content in for the time period prior to the byte write enable inputs being sampled.
3. Full-width WRITE can be initiated by $\overline{BWE}$, $\overline{BWa}$, - $\overline{BWd}$ LOW. Timing is shown assuming that the device was not enabled before entering into its sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.

PACKAGE DIMENSION: 119 BUMP PBGA



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

512Kx32 Part Number	Config.	t_{KQ} (ns)	Clock (MHz)	Package No.
Commercial Temp Range (0°C to 70°C)				
WED2DL32512V25BC	512Kx32	2.5	200	435
WED2DL32512V35BC	512Kx32	3.5	166	435
WED2DL32512V38BC	512Kx32	3.8	150	435
WED2DL32512V40BC	512Kx32	4.0	133	435
Industrial Temp Range (-40°C to +85°C)*				
WED2DL32512V38BI	512Kx32	3.8	150	435
WED2DL32512V40BI	512Kx32	4.0	133	435

** Advanced Information*