16MB (4x512Kx72) SYNC BURST PIPELINE, DUAL KEY DIMM

FEATURES

- 4x512Kx72 Synchronous Burst
- Pipeline Architecture; Dual Cycle Deselect
- Linear and Sequential Burst Support via MODE pin
- Clock Controlled Registered Module Enable (EM#)
- Clock Controlled Registered Bank Enables (E1#, E2#, E3#, E4#)
- Clock Controlled Byte Write Mode Enable (BWE#)
- Clock Controlled Byte Write Enables (BW1#-BW8#)
- Clock Controlled Registered Address
- Clock Controlled Registered Global Write (GW#)
- Asynchronous Output Enable (G#)
- Internally Self-Timed Write
- Individual Bank Sleep Mode Enables (ZZ1, ZZ2, ZZ3, ZZ4)
- Gold Lead Finish
- 3.3V ± 10% Operation
- Frequency(s): 200, 166, 150 and 133MHz
- Access Apeed(s): t_{KHQV} = 3.0, 3.5, 3.7 and 4.0ns
- Common Data I/O
- High Capacitance (30pF) Drive, at Rated Access Speed
- Single Total Array Clock
- Multiple V_{CC} and G_{ND} for Improved Noise Immunity

DESCRIPTION

The WED2EG472512V is a Synchronous/Synchronous Burst SRAM, 84 position Dual Key; Double High DIMM (168 contacts) Module, organized as 4x512Kx72. The Module contains sixteen (16) Synchronous Burst RAM devices, packaged in the industry standard JEDEC 14mmx20mm TQFP placed on a Multilayer FR4 Substrate. The Module Architecture is defined as a Sync/SyncBurst, Pipeline, with support for either linear or sequential burst. This Module provides high performance, 3-1-1-1 accesses when used in Burst Mode.

Synchronous Only operations are performed via strapping ADSC# Low, and ADSP#/ADV# High, which provides for Ultra Fast Accesses in Read Mode while providing for internally self-timed Early Writes.

Synchronous/Synchronous Burst operations are in relation to an externally supplied clock, Registered Address, Registered Global Write, egistered Enables as well as an Asynchronous Output Enable. This module has been defined with full flexibility, which allowes individual control of each of the eight bytes, as well as Quad Words in both Read and Write Operations.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

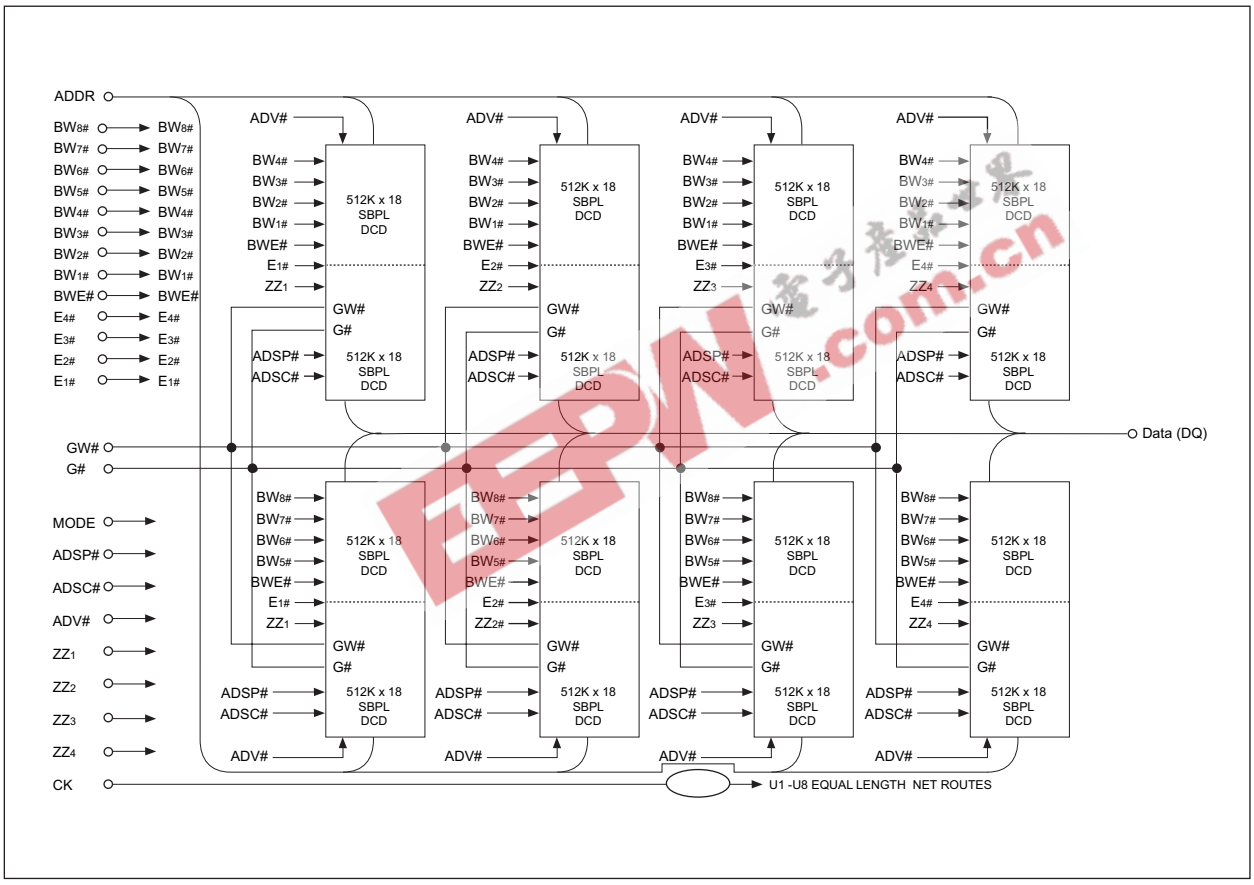
PIN CONFIGURATION

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V_{SS}	29	NC	57	NC	85	V_{SS}	113	DQP0	141	DQP4
2	A0	30	V_{CC}	58	V_{CC}	86	A17	114	V_{CC}	142	V_{CC}
3	A16	31	DQ0	59	DQ32	87	A1	115	DQ7	143	DQ39
4	A2	32	DQ1	60	DQ33	88	A15	116	DQ6	144	DQ38
5	A14	33	DQ2	61	DQ34	89	A3	117	DQ5	145	DQ37
6	V_{CC}	34	DQ3	62	DQ35	90	V_{CC}	118	DQ4	146	DQ36
7	A4	35	V_{SS}	63	V_{SS}	91	A13	119	V_{SS}	147	V_{SS}
8	A12	36	ZZ1	64	ZZ3	92	A5	120	DQP1	148	DQP5
9	A6	37	V_{CC}	65	V_{CC}	93	A11	121	V_{CC}	149	V_{CC}
10	A10	38	DQ8	66	DQ40	94	A7	122	DQ15	150	DQ47
11	V_{SS}	39	DQ9	67	DQ41	95	V_{SS}	123	DQ14	151	DQ46
12	A8	40	DQ10	68	DQ42	96	A9	124	DQ13	152	DQ45
13	RFU	41	DQ11	69	DQ43	97	A18	125	DQ12	153	DQ44
14	E4#	42	V_{SS}	70	V_{CC}	98	E1#	126	V_{SS}	154	V_{SS}
15	E2#	43	NC	71	NC	99	E3#	127	DQP2	155	DQP6
16	V_{SS}	44	V_{CC}	72	V_{CC}	100	V_{SS}	128	V_{CC}	156	V_{CC}
17	MODE	45	DQ16	73	DQ48	101	CK	129	DQ23	157	DQ55
18	EM#	46	DQ17	74	DQ49	102	V_{SS}	130	DQ22	158	DQ54
19	GW#	47	DQ18	75	DQ50	103	G#	131	DQ21	159	DQ53
20	RFU	48	DQ19	76	DQ51	104	BWE#	132	DQ20	160	DQ52
21	V_{CC}	49	V_{SS}	77	V_{SS}	105	V_{CC}	133	V_{SS}	161	V_{SS}
22	BW4#	50	ZZ2	78	ZZ4	106	BW2#	134	DQP3	162	DQP7
23	BW3#	51	V_{CC}	79	V_{CC}	107	BW1#	135	V_{CC}	163	V_{CC}
24	BW8#	52	DQ24	80	DQ56	108	BW6#	136	DQ31	164	DQ63
25	BW7#	53	DQ25	81	DQ57	109	BW5#	137	DQ30	165	DQ62
26	ADSC#	54	DQ26	82	DQ58	110	V_{SS}	138	DQ29	166	DQ61
27	ADSP#	55	DQ27	83	DQ59	111	ADV#	139	DQ28	167	DQ60
28	V_{SS}	56	V_{SS}	84	V_{SS}	112	V_{SS}	140	V_{SS}	168	V_{SS}

PIN DESCRIPTION

DQ0 - DQ63	Input / Output Bus
DQP0 - DQP7	Parity Bits
A0 - A18	Address Bus
EM#	Module Enable
E1#, E2#, E3#, E4#	Synchronous Bank Enables
BWE#	Byte Write Mode Enable
BW1# - BW8#	Byte Write Enables
CK	Array Clock
GW#	Synchronous Global Write Enable
G#	Asynchronous Output Enable
ZZ1, ZZ2, ZZ3, ZZ4	Bank Sleep Mode Enables
V_{CC}	3.3V Power Supply
V_{SS}	Ground

FUNCTIONAL BLOCK DIAGRAM



SYNC BURST - TRUTH TABLE

Operation	E1#	E2#	E3#	E4#	ADSP#	ADSC#	ADV#	GW#	G#	CK	DQ	Addr. Used
Deselected Cycle, Power Down; Bank 1	H	X			X	L	X	X	X	L-H	High-Z	None
Deselected Cycle, Power Down; Bank 2	X	H			X	L	X	X	X	L-H	High-Z	None
Read Cycle, Begin Burst; Bank 1	L	H			L	X	X	X	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	H			L	X	X	X	H	L-H	High-Z	External
Read Cycle, Begin Burst; Bank 2	H	L			L	X	X	X	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	H	L			L	X	X	X	H	L-H	High-Z	External
Write Cycle, Begin Burst; Bank 1	L	H			H	L	X	L	X	L-H	D	External
Write Cycle, Begin Burst; Bank 2	H	L			H	L	X	L	X	L-H	D	External
Read Cycle, Begin Burst; Bank 1	L	H			H	L	X	H	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	H			H	L	X	H	H	L-H	High-Z	External
Read Cycle, Begin Burst; Bank 2	H	L			H	L	X	H	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	H	L			H	L	X	H	H	L-H	High-Z	External
Read Cycle, Continue Burst; Bank 1	X	H			X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	X	H			X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	H	X			X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	H	X			X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 1	H	H			X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	H	H			X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	H	H			X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	H	H			X	H	L	H	H	L-H	High-Z	Next
Write Cycle, Continue Burst; Bank 1	X	H			H	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 1	H	H			X	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	H	X			H	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	H	H			X	H	L	L	X	L-H	D	Next
Read Cycle, Suspend Burst; Bank 1	X	H			H	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	X	H			H	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	H	X			H	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	H	X			H	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 1	H	H			X	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	H	H			X	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	H	H			X	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	H	H			X	H	H	H	H	L-H	High-Z	Current
Write Cycle, Suspend Burst; Bank 1	X	H			H	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 1	H	H			X	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	H	X			H	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	H	H			X	H	H	L	X	L-H	D	Current

Note A : All truth Table Functions Repeat for Bank 3 (E3#)and Bank 4 (E4#).

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Relative to V_{SS}	-0.3V to +4.6V
V_{IN}	-0.3V to V_{CC} +0.5V
Storage Temperature	-55°C to +125°C
Operating Temperature (Commercial)	0°C to +70°C
Operating Temperature (Industrial)	-40°C to +85°C
Short Circuit Output Current	100mA

* Stress greater than those listed under "Absolute Maxamin Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect reliability

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	3.3	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V
Input High	V_{IH}	2.0	3.0	V_{CC} + 0.3	V
Input Low	V_{IL}	-0.3	0	0.3	V
Input Leakage	I_{LI}	-2	1	3	µA
Output Leakage	I_{LO}	-2	1	2	µA

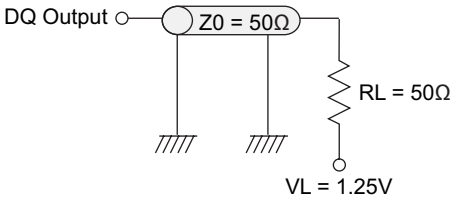
SYNCHRONOUS ONLY - TRUTH TABLE

Operation	E1#	E2#	E3#	E4#	GW#	G#	ZZ	CK	DQ
Synchronous Write - Bank 1	L	H	H	H	L	H	L	↑	High-Z
Synchronous Read - Bank 1	L	H	H	H	H	L	L	↑	
Synchronous Write - Bank 2	H	L	H	H	L	H	L	↑	High-Z
Synchronous Read - Bank 2	H	L	H	H	H	L	L	↑	
Synchronous Write - Bank 3	H	H	L	H	L	H	L	↑	High-Z
Synchronous Read - Bank 3	H	H	L	H	H	L	L	↑	
Synchronous Write - Bank 4	H	H	H	L	L	H	L	↑	High-Z
Synchronous Read - Bank 4	H	H	H	L	H	L	L	↑	
Snooze Mode	X	X	X	X	X	X	H	X	High-Z

DC ELECTRICAL CHARACTERISTICS READ CYCLE

Description	Sym	Typ	Max				Units
			5.0	6.0	6.5	7.0	
Power Supply Current	I_{CC1}	1.8	2.6	2.4	2.3	2.2	A
Power Supply Current Device Selected, No Operation	I_{CC}	875	1.8	1.8	1.3	1.3	A
Snooze Mode	I_{CCZZ}	270	350	350	350	350	mA
CMOS Standby	I_{CC3}	500	700	700	700	700	mA
Clock Running-Deselect	I_{CCK}	900	1.1	1.1	1.0	1.0	A

AC TEST LOAD



Output Test Equivalencies

AC TEST CONDITIONS

Input Pulse Levels	V_{SS} to 3.0V
Input and Output Timing Ref.	1.25V
Output test Equivalencies	see figure at left

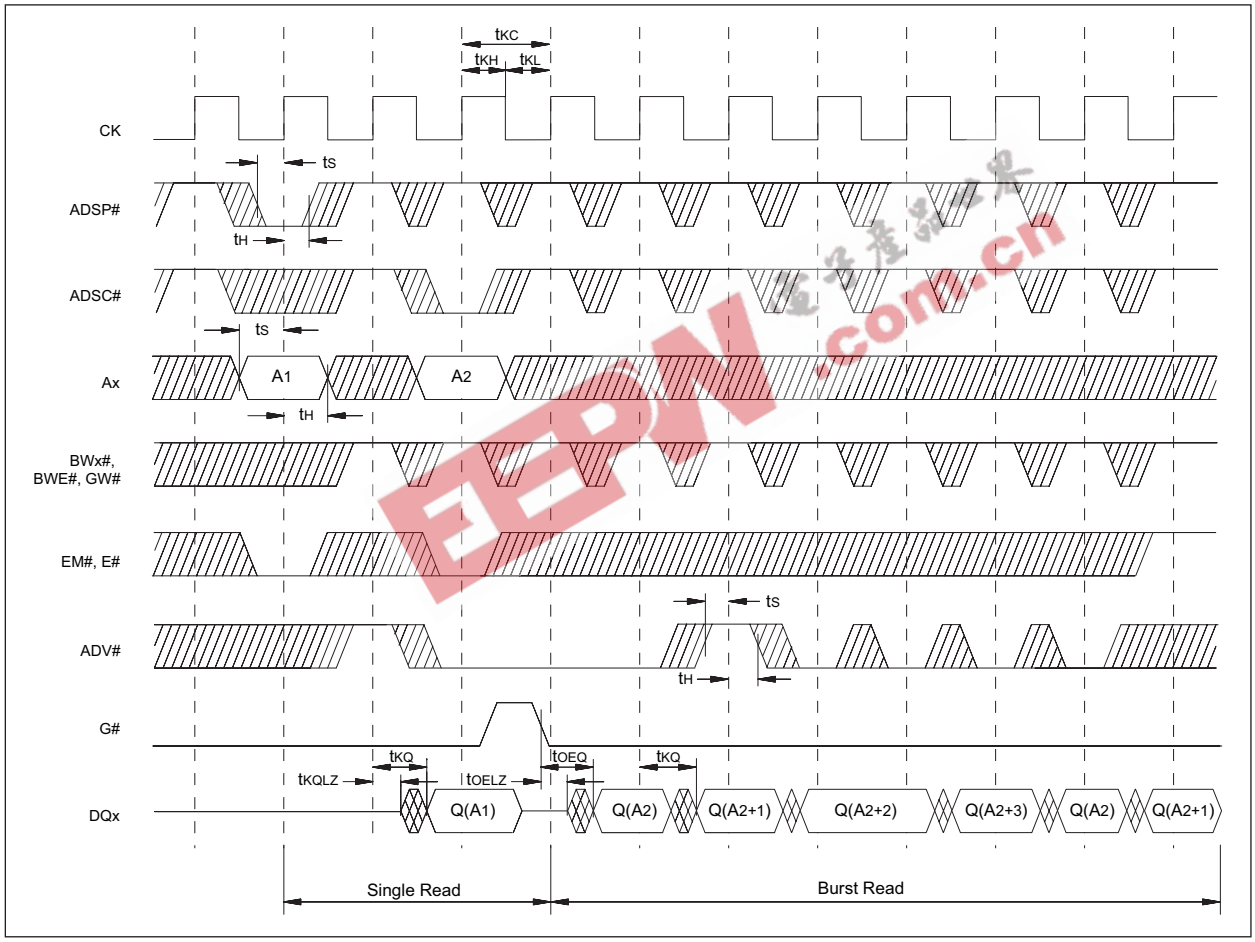
SYNC-BURST READ CYCLE PARAMETERS

Description	Sym	3.0ns		3.5ns		3.7ns		4.0ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Frequency	f_{MAX}		200		160		150		133	MHz
Clock Cycle Time	t_{KC}	5.0		6.0		6.5		7.0		ns
Clock High Time	t_{KH}	2		2.4		2.5		3		ns
Clock Low Time	t_{KL}	2		2.4		2.5		3		ns
Clock to Output Valid	t_{KQ}		3		3.5		3.7		4	ns
Clock to Output Invalid	t_{KQX}	1.25		1.25		1.25		1.25		ns
Clock to Output Low-Z	t_{KQLZ}	0		0		0		0		ns
Clock Enable to Output Valid	t_{OEQ}	1.25	3	1.25	4	1.25	4	1.25	5	ns
Clock Enable to Output Low-Z	t_{OELZ}	0		0		0		0		ns
Clock Enable to Output High-Z	t_{OEHZ}		2.5		3.5		3.5		4	ns
Address Setup	t_S	1.5		1.5		1.8		2.0		ns
Bank Enable Setup	t_S	1.5		1.5		1.8		2.0		ns
Address Hold	t_H	0.5		0.5		0.5		0.5		ns
Bank Enable Hold	t_H	0.5		0.5		0.5		0.5		ns

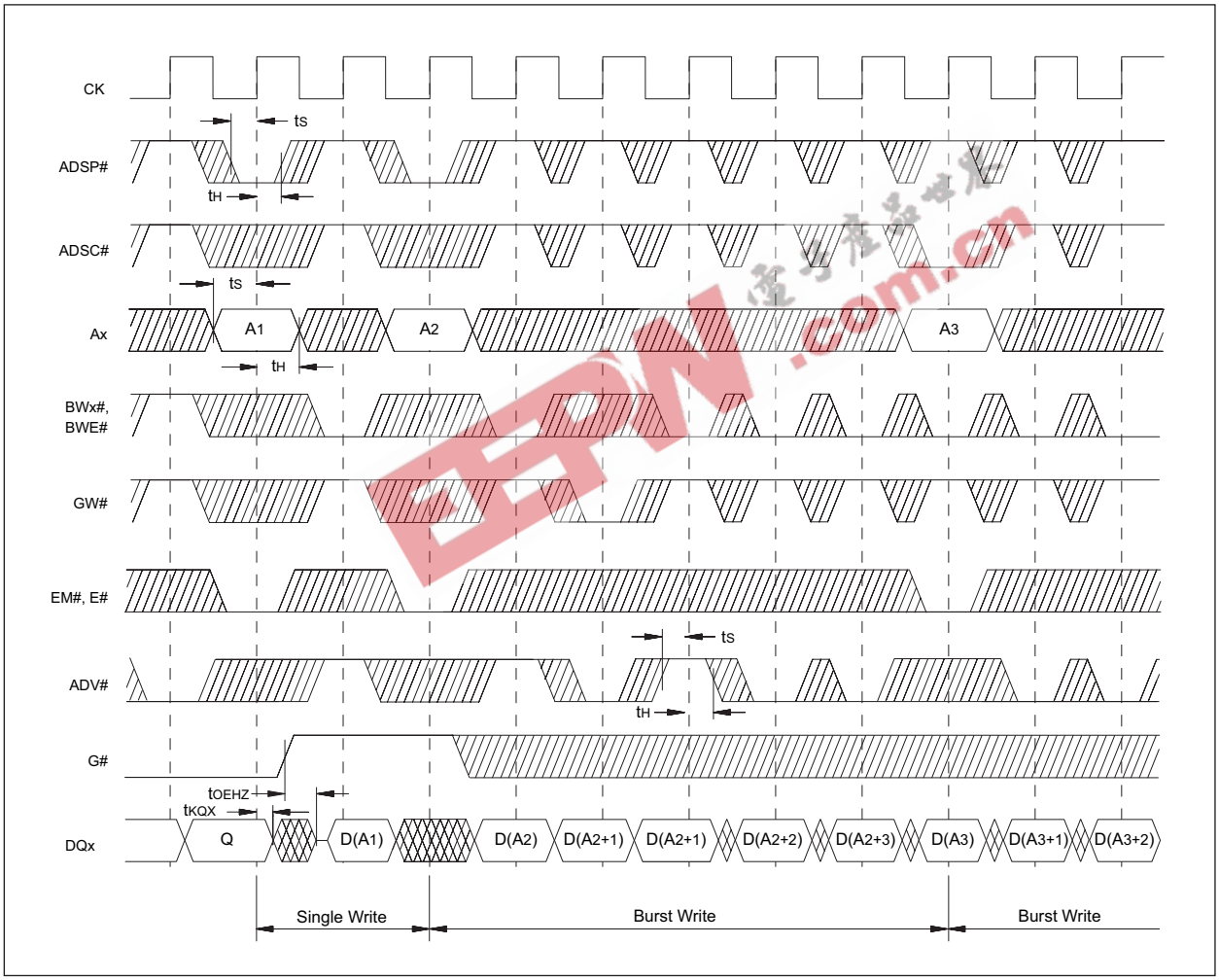
SYNC-BURST WRITE CYCLE PARAMETERS

Description	Sym	3.0ns		3.5ns		3.7ns		4.0ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Frequency	f_{MAX}		200		166		150		133	MHz
Clock Cycle Time	t_{KC}	5.0		6.0		6.5		7.0		ns
Clock High Time	t_{KH}	2		2.4		2.7		3		ns
Clock Low Time	t_{KL}	2		2.4		2.7		3		ns
Address Setup	tS	1.5		1.5		1.8		2.0		ns
Address Hold	tH	0.5		0.5		0.5		0.5		ns
Bank Enable Setup	tS	1.5		1.5		1.8		1.8		ns
bank Enable Hold	tH	0.5		0.5		0.5		0.5		ns
Global Write Enable Setup	tS	1.5		1.5		1.8		1.8		ns
Global Write Enable Hold	tH	0.5		0.5		0.5		0.5		ns
Data Setup	tS	1.5		1.5		1.8		1.8		ns
Data Hold	tH	0.5		0.5		0.5		0.5		ns

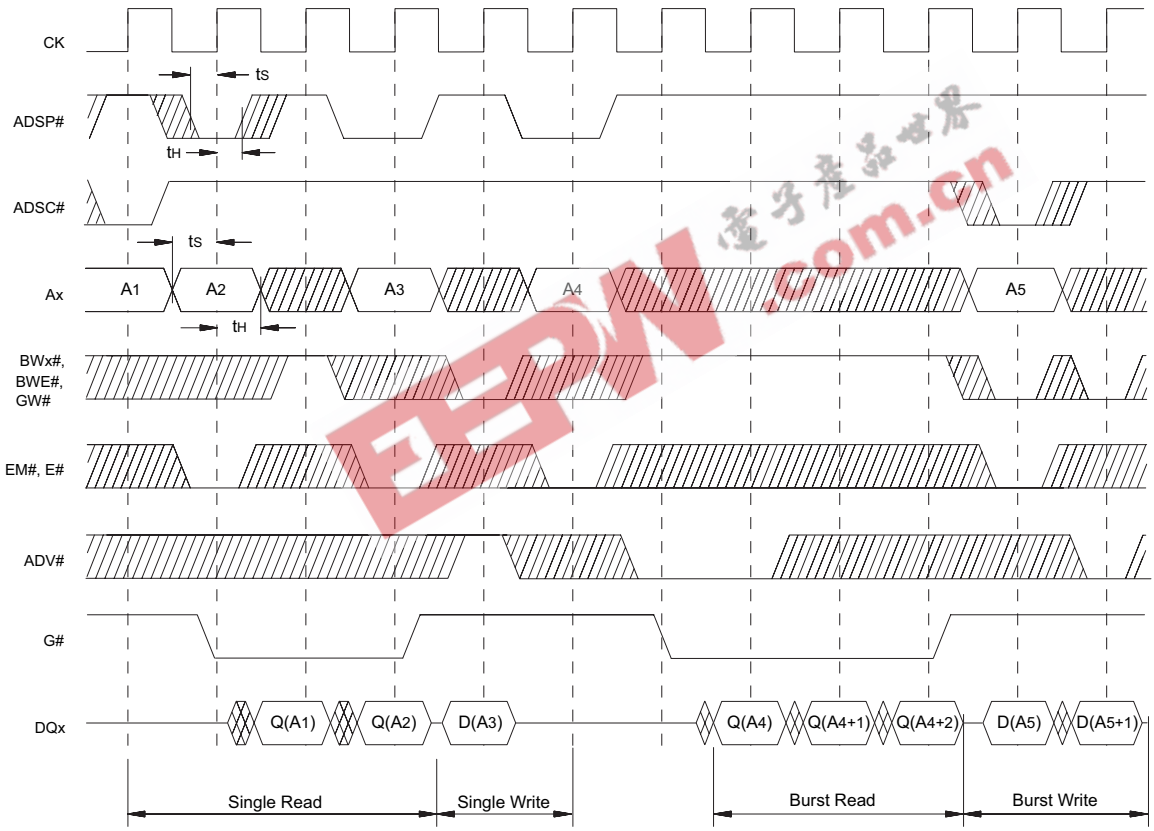
SYNC-BURST READ CYCLE



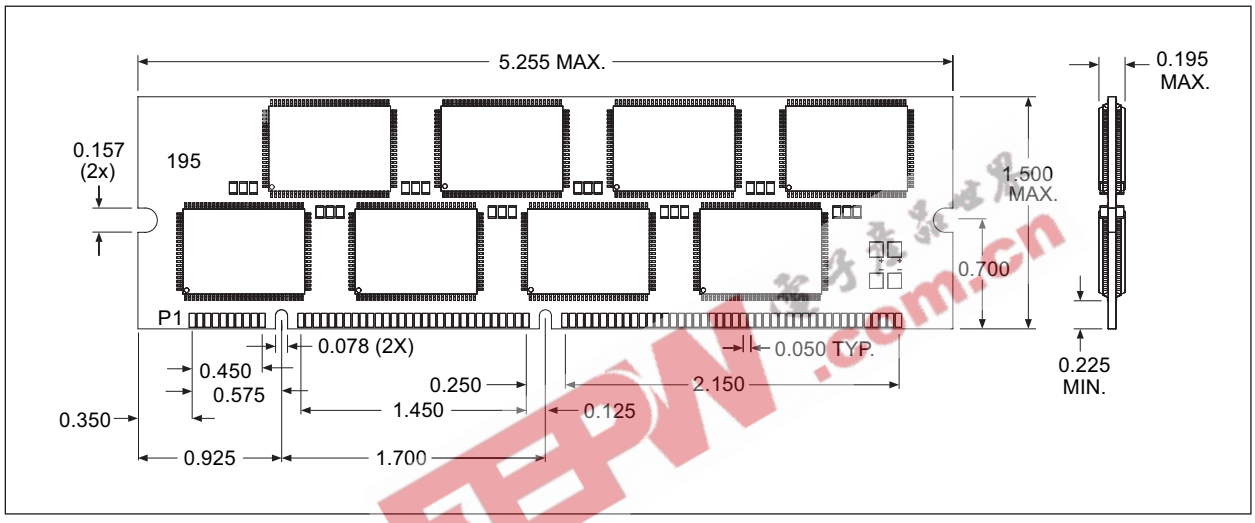
SYNC-BURST WRITE CYCLE



SYNC-BURST READ/WRITE CYCLE



PACKAGE DIMENSIONS: 168 DUAL KEY DIMM



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

Part Number	Configuration	Description	Voltage (V)	Frequency	Package
WED2EG472512V5D2	16MB (4 x 512K x 72)	Sync-Burst Pipeline	3.3	200MHz	168 Dual Key DIMM
WED2EG472512V6D2	16MB (4 x 512K x 72)	Sync-Burst Pipeline	3.3	166MHz	168 Dual Key DIMM
WED2EG472512V65D2	16MB (4 x 512K x 72)	Sync-Burst Pipeline	3.3	150MHz	168 Dual Key DIMM
WED2EG472512V7D2	16MB (4 x 512K x 72)	Sync-Burst Pipeline	3.3	133MHz	168 Dual Key DIMM