512Kx32 SRAM MULTI-CHIP PACKAGE

FEATURES

- Access Times of 12, 15, 17, 20, ns
- Packaging
  - 16mm x 18mm, 143 PBGA
- Organized as 512Kx32, User Configurable as 1Mx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 5V Power Supply
- Low Power CMOS

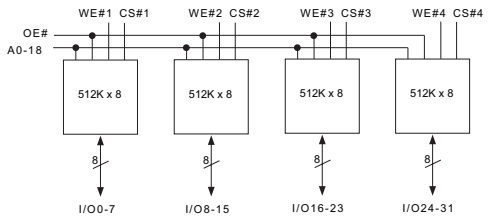
This product is subject to change without notice.

PIN CONFIGURATION FOR WEDPS512K32-XBX

TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12
A	-	A2	A1	A0	GND	GND	Vcc	Vcc	A18	A17	A16	GND
B	CS#2	A3	A4	D14	D15	NC	CS#4	D24	D25	OE#	A15	NC
C	D9	D8	NC	D12	D13	GND	Vcc	D26	D27	WE#4	D31	D30
D	D10	D11	GND	GND	GND	GND	Vcc	Vcc	Vcc	Vcc	D28	D29
E	WE#2	GND	GND	GND	GND	GND	Vcc	Vcc	Vcc	Vcc	Vcc	NC
F	GND	GND	GND	GND	GND	GND	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc
G	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc	GND	GND	GND	GND	GND	GND
H	CS#1	Vcc	Vcc	Vcc	Vcc	Vcc	GND	GND	GND	GND	GND	NC
J	D1	D0	Vcc	Vcc	Vcc	Vcc	GND	GND	GND	GND	D23	D22
K	D2	D3	NC	D7	D5	Vcc	GND	D17	D16	CS#3	D20	D21
L	WE#1	A6	A5	D6	D4	NC	WE#3	D19	D18	A14	A13	NC
M	GND	A7	A8	A9	Vcc	Vcc	GND	GND	A10	A11	A12	Vcc

BLOCK DIAGRAM



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
WE#1-4	Write Enables
CS#1-4	Chip Selects
OE#	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	V_{CC}+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

TRUTH TABLE

CS	OE	WE	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp (Mil)	T_A	-55	+125	°C

BGA THERMAL RESISTANCE

Description	Symbol	Max	Unit	Notes
Junction to Ambient (No Airflow)	Theta JA	16.5	°C/W	1
Junction to Ball	Theta JB	11.3	°C/W	1
Junction to Case (Top)	Theta JC	9.8	°C/W	1

NOTE: Refer to Application Note "PBGA Thermal Resistance Correlation" at www.whiteedc.com in the application notes section for modeling conditions.

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	30	pF
WE#1-4 capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	10	pF
CS#1-4 capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	10	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	10	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	30	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	CS# = V_{IH}, OE# = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current x 32 Mode	I_{CC} x 32	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz, Vcc = 5.5		660	mA
Standby Current	I_{SB}	CS# = V_{IH}, OE# = V_{IH}, f = 5MHz, Vcc = 5.5		80	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-12		-15		-17		-20		Units
Read Cycle		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Read Cycle Time	t_{RC}	12		15		17		20		ns
Address Access Time	t_{AA}		12		15		17		20	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		ns
Chip Select Access Time	t_{ACS}		12		15		17		20	ns
Output Enable to Output Valid	t_{OE}		7		8		9		10	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	1		2		2		2		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		7		12		12		12	ns
Output Disable to Output in High Z	t_{OHZ}[1]		7		12		12		12	ns

1. This parameter is guaranteed by design but not tested.

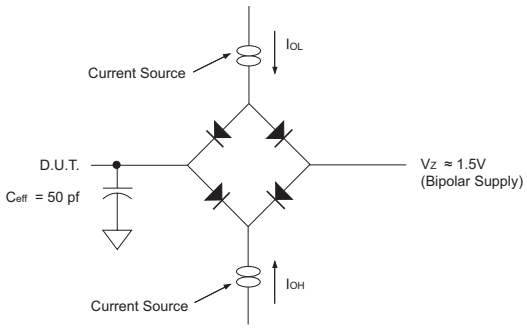
AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-12		-15		-17		-20		Units
Read Cycle		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Write Cycle Time	t_{WC}	12		15		17		20		ns
Chip Select to End of Write	t_{CW}	10		13		15		15		ns
Address Valid to End of Write	t_{AW}	10		13		15		15		ns
Data Valid to End of Write	t_{DW}	8		10		11		12		ns
Write Pulse Width	t_{WP}	10		13		15		15		ns
Address Setup Time	t_{AS}	0		2		2		2		ns
Address Hold Time	t_{AH}	0		0		0		0		ns
Output Active from End of Write	t_{OW1}	2		2		2		3		ns
Write Enable to Output in High Z	t_{WHZ1}		7		8		9		11	ns
Data Hold Time	t_{DH}	0		0		0		0		

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

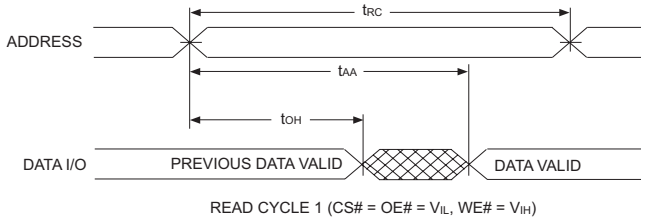


AC TEST CONDITIONS

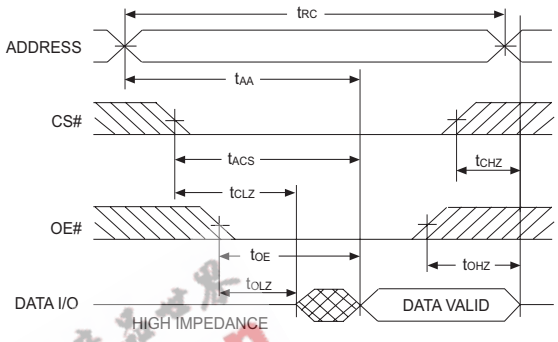
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

TIMING WAVEFORM - READ CYCLE

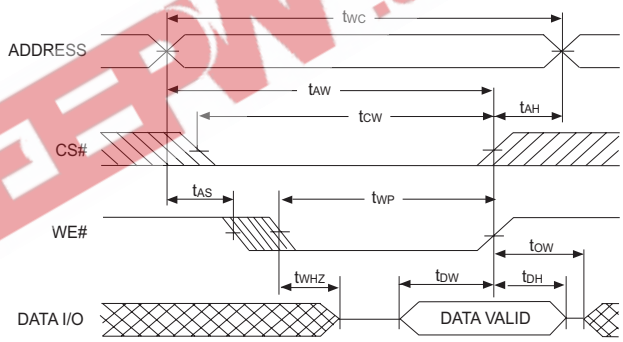


READ CYCLE 1 (CS# = OE# = V_{IL}, WE# = V_{IH})



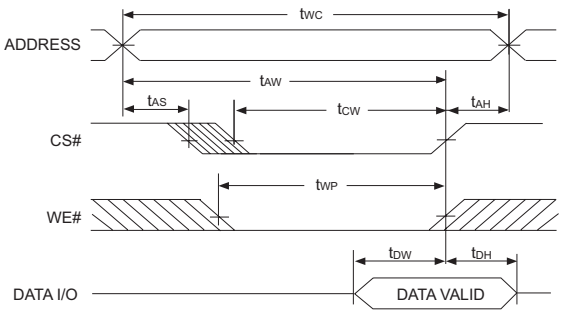
READ CYCLE 2 (WE# = V_{IH})

WRITE CYCLE - WE# CONTROLLED



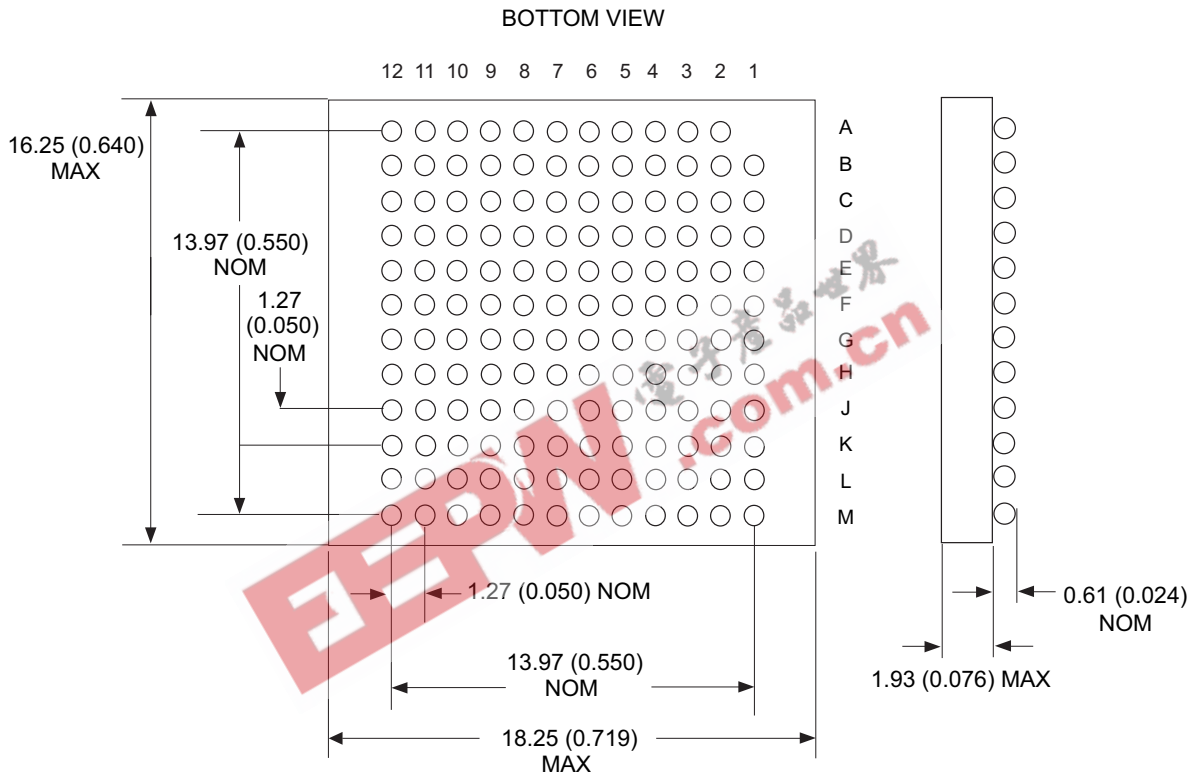
WRITE CYCLE 1, WE# CONTROLLED

WRITE CYCLE - CS# CONTROLLED



WRITE CYCLE 2, CS# CONTROLLED

PACKAGE 7043: 143 BALL GRID ARRAY



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

WED P S 512K 32 - XX X X

WHITE ELECTRONIC DESIGNS CORP.

PLASTIC

SRAM

ORGANIZATION, 512Kx32
User configurable as 1Mx16 or 2Mx8

ACCESS TIME (ns)

PACKAGE TYPE:
B = 143 PBGA, 16mm x 18mm, 288mm^2

DEVICE GRADE:

M	=	Military Screened	-55°C to +125°C
I	=	Industrial	-40°C to 85°C
C	=	Commercial	0°C to +70°C

Document Title			
512K x 32 SRAM Multi-Chip Package			
Revision History			
Rev #	**History**	**ReleaseDate**	**Status**
Rev 0	Initial Release	March 2002	Advanced
Rev 1	Switch Rows and Columns header position (Pg. 1)	March 2002	Advanced
Rev 2	Switch Rows and Columns header position (Pg. 1)	May 2002	Advanced
Rev 3	Change mechanical outline to more accurate design (Pg. 1, 5)	May 2002	Advanced
Rev 4	Remove references to 25-55ns speed grades (Pg. 1, 2, 3)	August 2002	Advanced
Rev 5	Changes (Pg. 1, 2) 1.1 Add Thermal Resistance Table 1.2 Change product status to Final	January 2003	Final
Rev 6	Changes (Pg. 1, 5, 7) 1.1 Change package body height to 1.93mm Max 1.2 Add ball pitch (1.27mm) to package dimension	November 2003	Final