W81281

USB Keyboard/ Device Controller

W81281 Data Sheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1		09/01/1997	0.50		First published.
2	All	12/16/1997 7/12/1999	0.51 0.6		Update Features Update registers description
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LIFE SUPPORT APPLICATIONS

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Preliminary

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Winbond Electronics Corp.

USB Keyboard/ Device Controller

1. GENERAL DESCRIPTION

W81281 is a low cost, high integration single-chip microcontroller with Universal Serial Bus (USB) interface for keyboard application, it includes the core of Winbond 8-bit microprocessor W78C52 which works on 6MHz. It implements a standard PC keyboard and enables connection to host system through low-speed (1.5Mhz) USB connection . It complies with USB Specification Revision 1.0 and HID Class Definition Revision 1.0.

For Keyboard application, W81281 supports an 18 X 8 keyboard scan matrix, which allows suspend wake up, and also provides a port for PS/2 mouse. It consists of an 8051 compatible CPU core, a 6K-byte ROM, a 256-byte SRAM, and three 16-bit programmable timers.

W81281 supports one device address and five endpoints, one bi-directional endpoint for Control transfer and four unidirectional endpoints for Interrupt IN transfer. Through modification of firmware of W78C52, it can be used for multifunction device design, such as USB-IR receiver and any Slow-Speed (1.5Mhz) USB peripheral device controller.

2. FEATURES

- Fully compliant with USB spec. Rev.1.0 and HID Class Rev. 1.0
- Supporting one device address and five endpoints (one Control transfer, four Interrupt transfer)
- Implementing USB keyboard with PS/2 mouse connection
- Microsoft Intellimouse(3D mouse) Supported
- Supporting 8-bit sense (row) input with wake up interrupt on falling edge, internal pull-ups
- Supporting 18-bit drive (column) output, open drain with pull-ups
- 8-bit 8051 compatible CPU core
- 6K-byte ROM
- 256-byte SRAM
- 3 direct drive LED outputs with internal series resisters
- Supporting warm reset
- Built-in low voltage reset and EFT/ESD protection circuit
- Built-in Watch-Dog Timer for device recovery
- Support Win98 system control function
- Support suspend/wake-up function, suspend current under 500μA
- Internal 3.3V regulator supported
- 40-pin DIP, 28-pin SOP and 48-pin LQFP packages
- 5V CMOS Device

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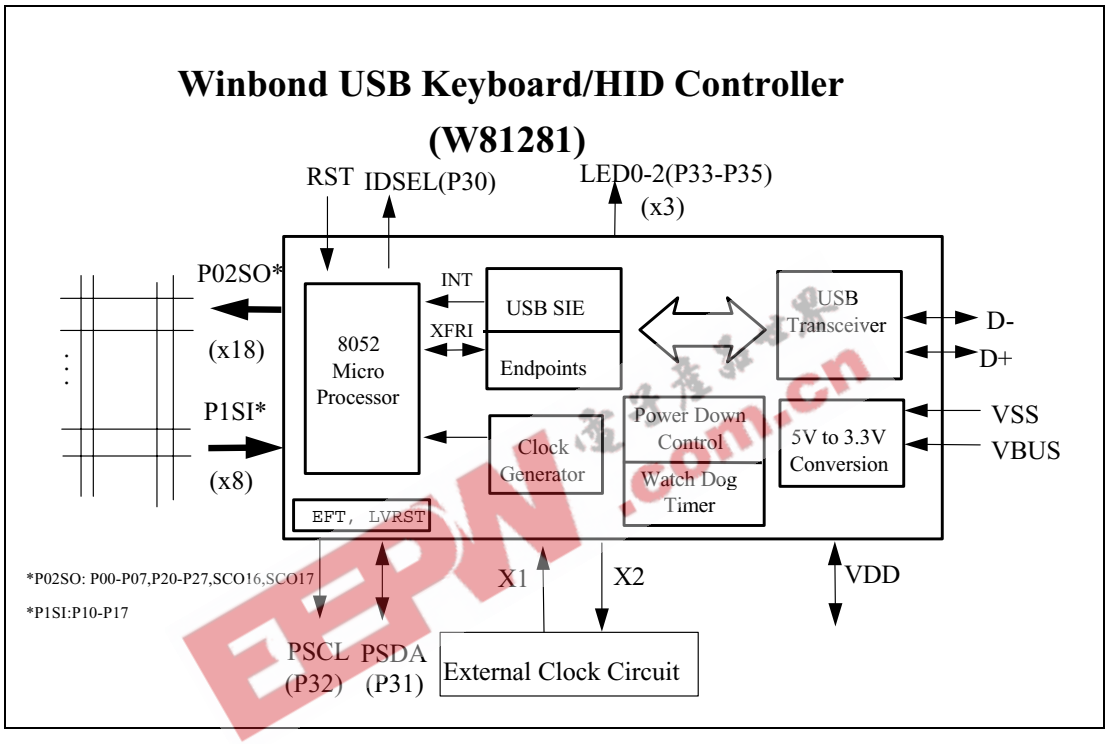
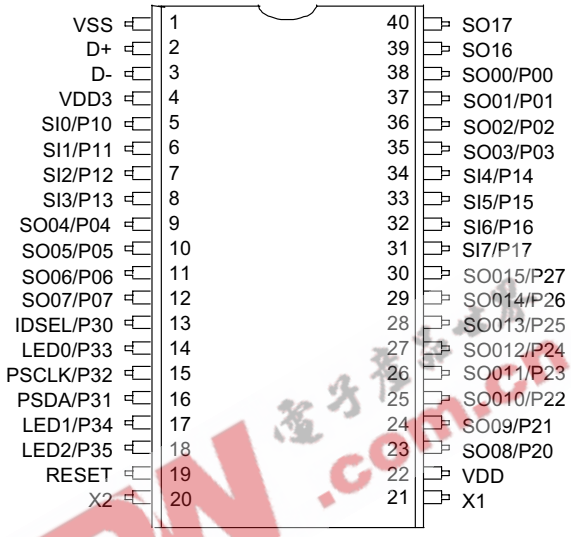
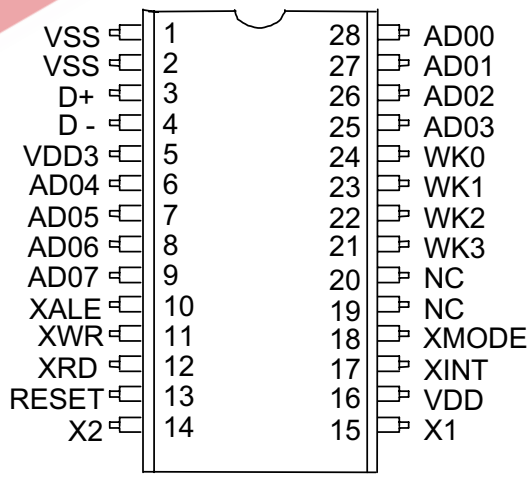
Winbond USB Keyboard/HID Controller



4. PIN CONFIGURATION



40-PIN DIP



28-PIN SOP

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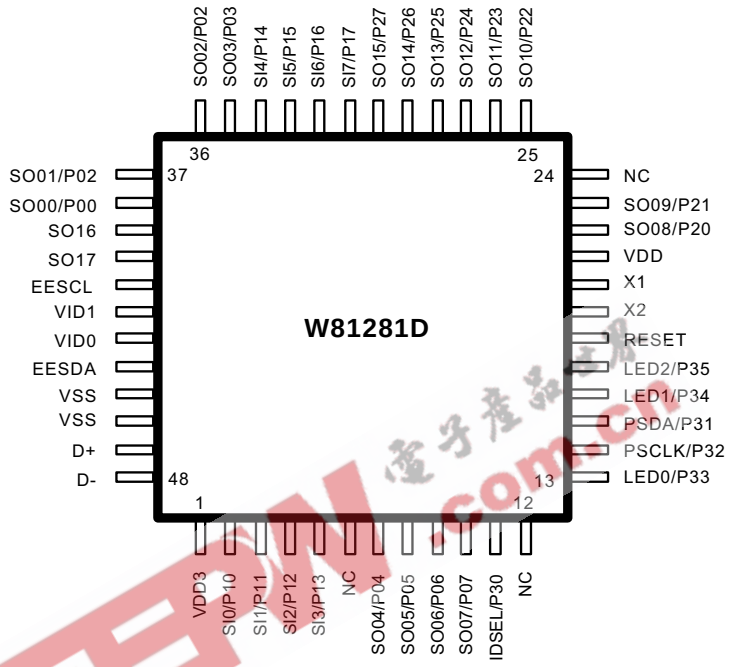

48-pin LQFP

Publication Release Date: July 1999
Revision 0.60

5. PIN DESCRIPTION

5.1 40 PIN DIP

PIN NO.	NAME	TYPE	DESCRIPTION
1	VSS	POWER	Ground
2	D+	I/O	USB signal (+)
3	D-	I/O	USB signal (-)
4	VDD3	POWER	DC power 3.3V output
5	SI0/P10	I/O	Keyboard scan Input 0 / Internal µC IO port 1.0
6	SI1/P11	I/O	Keyboard scan Input 1 / Internal µC IO port 1.1
7	SI2/P12	I/O	Keyboard scan Input 2 / Internal µC IO port 1.2
8	SI3/P13	I/O	Keyboard scan Input 3 / Internal µC IO port 1.3
9	SO04/P04	I/O	Keyboard scan Output 04 / Internal µC IO port 0.4
10	SO05/P05	I/O	Keyboard scan Output 05 / Internal µC IO port 0.5
11	SO06/P06	I/O	Keyboard scan Output 06 / Internal µC IO port 0.6
12	SO07/P07	I/O	Keyboard scan Output 07 / Internal µC IO port 0.7
13	IDSEL/P30	I/O	Vendor ID selection / Internal µC IO port 3.0
14	LED0/P33	I/O	Num. Lock LED / Internal µC IO port 3.3
15	PSCLK/P32	I/O	PS/2 mouse clock pin / Internal µC IO port 3.2
16	PSDA/P31	I/O	PS/2 mouse data pin / Internal µC IO port 3.1
17	LED1/P34	I/O	Caps Lock LED / Internal µC IO port 3.4
18	LED2/P35	I/O	Scroll Lock LED / Internal µC IO port 3.5
19	RESET	INPUT	Chip reset pin
20	X2	OUTPUT	Clock output
21	X1	INPUT	Clock input
22	VDD	POWER	VDD power
23	SO08/P20	I/O	Keyboard scan Output 08 / Internal µC IO port 2.0
24	SO09/P21	I/O	Keyboard scan Output 09 / Internal µC IO port 2.1
25	SO10/P22	I/O	Keyboard scan Output 10 / Internal µC IO port 2.2
26	SO11/P23	I/O	Keyboard scan Output 11 / Internal µC IO port 2.3
27	SO12/P24	I/O	Keyboard scan Output 12 / Internal µC IO port 2.4
28	SO13/P25	I/O	Keyboard scan Output 13 / Internal µC IO port 2.5

5.1 40-PIN DIP, continued

PIN NO.	NAME	TYPE	DESCRIPTION
29	SO14/P26	I/O	Keyboard scan Output 14 / Internal µC IO port 2.6
30	SO15/P27	I/O	Keyboard scan Output 15 / Internal µC IO port 2.7
31	SI7/P17	I/O	Keyboard scan Input 7 / Internal µC IO port 1.7
32	SI6/P16	I/O	Keyboard scan Input 6 / Internal µC IO port 1.6
33	SI5/P15	I/O	Keyboard scan Input 5 / Internal µC IO port 1.5
34	SI4/P14	I/O	Keyboard scan Input 4 / Internal µC IO port 1.4
35	SO03/P03	I/O	Keyboard scan Output 03 / Internal µC IO port 0.3
36	SO02/P02	I/O	Keyboard scan Output 02 / Internal µC IO port 0.2
37	SO01/P01	I/O	Keyboard scan Output 01 / Internal µC IO port 0.1
38	SO00/P00	I/O	Keyboard scan Output 00 / Internal µC IO port 0.0
39	SO16	OUTPUT	Keyboard scan Output 16
40	SO17	OUTPUT	Keyboard scan Output 17

5.2 28-PIN SOP

PIN NO.	NAME	TYPE	DESCRIPTION
1	VSS	POWER	Ground
2	VSS	POWER	Ground
3	D+	I/O	USB signal (+)
4	D-	I/O	USB signal (-)
5	VDD3	POWER	DC power 3.3V output
6	AD04	I/O	µC Interface AD04 (Address/Data 04)
7	AD05	I/O	µC Interface AD05 (Address/Data 05)
8	AD06	I/O	µC Interface AD06 (Address/Data 06)
9	AD07	I/O	µC Interface AD07 (Address/Data 07)
10	XALE	I/O	µC Interface ALE (Address Latch Enable)
11	XWR	I/O	µC Interface WR (Data Write)
12	XRD	I/O	µC Interface RD (Data Read)
13	RESET	INPUT	Chip reset pin
14	X2	OUTPUT	Clock output
15	X1	INPUT	Clock input
16	VDD	POWER	VDD power
17	XINT	I/O	µC Interface INT (Interrupt)
18	XMODE	I/O	Controller mode setting, it should be kept high
19	NC	I/O	Not Used
20	NC	I/O	Not Used
21	WK3	INPUT	Wakeup pin, Active low and keep more than 100ns
22	WK2	INPUT	Wakeup pin, Active low and keep more than 100ns
23	WK1	INPUT	Wakeup pin, Active low and keep more than 100ns
24	WK0	INPUT	Wakeup pin, Active low and keep more than 100ns
25	AD03	I/O	µC Interface AD03 (Address/Data 03)
26	AD02	I/O	µC Interface AD02 (Address/Data 02)
27	AD01	I/O	µC Interface AD01 (Address/Data 01)
28	AD00	I/O	µC Interface AD00 (Address/Data 00)

5.3 48-PIN LQFP

PIN NO.	NAME	TYPE	DESCRIPTION
1	VDD3	POWER	DC power 3.3V output
2	SI0/P10	I/O	Keyboard scan Input 0 / Internal µC IO port 1.0
3	SI1/P11	I/O	Keyboard scan Input 1 / Internal µC IO port 1.1
4	SI2/P12	I/O	Keyboard scan Input 2 / Internal µC IO port 1.2
5	SI3/P13	I/O	Keyboard scan Input 3 / Internal µC IO port 1.3
6	NC	none	Not Used
7	SO04/P04	I/O	Keyboard scan Output 04 / Internal µC IO port 0.4
8	SO05/P05	I/O	Keyboard scan Output 05 / Internal µC IO port 0.5
9	SO06/P06	I/O	Keyboard scan Output 06 / Internal µC IO port 0.6
10	SO07/P07	I/O	Keyboard scan Output 07 / Internal µC IO port 0.7
11	IDSEL/P30	I/O	Vendor ID selection / Internal µC IO port 3.0
12	NC	none	Not Used
13	LED0/P33	I/O	Num. Lock LED / Internal µC IO port 3.3
14	PSCLK/P32	I/O	PS/2 mouse clock pin / Internal µC IO port 3.2
15	PSDA/P31	I/O	PS/2 mouse data pin / Internal µC IO port 3.1
16	LED1/P34	I/O	Caps Lock LED / Internal µC IO port 3.4
17	LED2/P35	I/O	Scroll Lock LED / Internal µC IO port 3.5
18	RESET	INPUT	Chip reset pin
19	X2	OUTPUT	Clock output
20	X1	INPUT	Clock input
21	VDD	POWER	VDD power
22	SO08/P20	I/O	Keyboard scan Output 08 / Internal µC IO port 2.0
23	SO09/P21	I/O	Keyboard scan Output 09 / Internal µC IO port 2.1
24	NC	none	Not Used
25	SO10/P22	I/O	Keyboard scan Output 10 / Internal µC IO port 2.2
26	SO11/P23	I/O	Keyboard scan Output 11 / Internal µC IO port 2.3
27	SO12/P24	I/O	Keyboard scan Output 12 / Internal µC IO port 2.4
28	SO13/P25	I/O	Keyboard scan Output 13 / Internal µC IO port 2.5
29	SO14/P26	I/O	Keyboard scan Output 14 / Internal µC IO port 2.6
30	SO15/P27	I/O	Keyboard scan Output 15 / Internal µC IO port 2.7

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5.3 48-PIN LQFP, continued

PIN NO.	NAME	TYPE	DESCRIPTION
31	SI7/P17	I/O	Keyboard scan Input 7 / Internal µC IO port 1.7
32	SI6/P16	I/O	Keyboard scan Input 6 / Internal µC IO port 1.6
33	SI5/P15	I/O	Keyboard scan Input 5 / Internal µC IO port 1.5
34	SI4/P14	I/O	Keyboard scan Input 4 / Internal µC IO port 1.4
35	SO03/P03	I/O	Keyboard scan Output 03 / Internal µC IO port 0.3
36	SO02/P02	I/O	Keyboard scan Output 02 / Internal µC IO port 0.2
37	SO01/P01	I/O	Keyboard scan Output 01 / Internal µC IO port 0.1
38	SO00/P00	I/O	Keyboard scan Output 00 / Internal µC IO port 0.0
39	SO16	OUTPUT	Keyboard scan Output 16
40	SO17	OUTPUT	Keyboard scan Output 17
41	EESCL	OUTPUT	Clock pin of External serial EEPROM
42	VID1	INPUT	Vendor ID selection 1
43	VID0	INPUT	Vendor ID selection 0
44	EESDA	I/O	Data pin of External serial EEPROM
45	VSS	POWER	Ground
46	VSS	POWER	Ground
47	D+	I/O	USB signal (+)
48	D-	I/O	USB signal (-)

6 FUNCTIONAL DESCRIPTION

6.1 First In First Out Storage (FIFO'S) Organization

The W81281 has six FIFO's, one for receiving and five for transmitting.

FIFO or SRAM	SIZE (Byte)	NOTES
Endpt 0 Receiving	8	Data received on upstream port which contains the correct address and pids will be stored here for the CPU core to read.
Endpt 0 Transmitting	8	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.
Endpt 1 Transmitting	8	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.
Endpt 2 Transmitting	8	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.
Endpt 3 Transmitting	8	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.
Endpt 4 Transmitting	8	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.

6.1.1 INTERFACE TO THE MICROCONTROLLER:

The FIFOs communicate with the CPU core by address 06H 0f External DATA Memory Access of CPU during IP.6 = "1".The FIFO access steps are firstly set IP.6 = "1" in CPU core. Secondly, CPU core selects FIFO to access by setting the followed bits in control register 2 :

EP0_RD_EN : read "IN" FIFO of Endpoint 0 (EP0).
EP0_WR_EN : write "OUT" FIFO of Endpoint 0 (EP0).
EP1_WR_EN : write "OUT" FIFO of Endpoint 1 (EP1).
EP2_WR_EN : write "OUT" FIFO of Endpoint 2 (EP2).
EP3_WR_EN : write "OUT" FIFO of Endpoint 3 (EP3).
EP4_WR_EN : write "OUT" FIFO of Endpoint 4 (EP4).

Then access FIFO by address 06H of External DATA Memory Access of CPU. For detailed programming steps, refer to section 7.3 Programming Note.

6.2 Register Descritpion

The CPU core accesses registers by External DATA Memory Access during IP.6 = "1"'1'

6.2.1 Status Registers

CPU core can set "High" at USB_EventINT_EN bit of control register 4 to enable interrupt of USB events to INT0. When interrupt comes, CPU reads status register 0 and 1 to check which event occurs. (refer to section 7.2 for accessing Status Registers)

Status Register 0: Address = 00H (Interrupt Event Flags)

BIT	SYMBOL	DESCRIPTION
7	NAK_EP0_IN	NAK occurs from EP0 for IN Transaction. (only valid during NakEP0In_INT_EN = 1 in Control Register 3)
6	ACK_EP0_SETUP	ACK occurs from EP0 for SETUP Transaction
5	ACK_EP0_OUT	ACK occurs from EP0 for OUT Transaction
4	ACK_EP0_IN	ACK occurs from EP0 for IN Transaction
3	ACK_EP1_IN	ACK occurs from EP1 for IN Transaction
2	ACK_EP2_IN	ACK occurs from EP2 for IN Transaction
1	ACK_EP3_IN	ACK occurs from EP3 for IN Transaction
0	ACK_EP4_IN	ACK occurs from EP4 for IN Transaction

Status Register 1: Address = 01H (Interrupt Event Flags)

BIT	SYMBOL	DESCRIPTION
7-6	VID[1:0]	Keyboard Scan Matrix Selection.
5	Reserved	must ignore this value.
4	EP0OutNullData	receiving Null Data at EP0 during OUT Transaction
3	Suspend_In	Suspend Mode active (no traffic on USB Bus > 3 mS)
2	USB_Reset	receiving Reset command from USB Bus
1	Resume_In	receiving Resume command from USB Bus
0	Reserved	must ignore this value

Status Register 2: Address = 07H (Data Byte Count of EP0 IN FIFO)

BIT	SYMBOL	DESCRIPTION
7-4	Reserved	must ignore those values
3-0	DataLength_CNT[3:0]	Number of Data byte for EP0 FIFO (receiving Data from USB Bus)

6.2.2 Control Registers

(All registers are set to 00h at power up.)(refer to section 7.1 for accessing Control Registers)

Control Register 0: Address = 02H (Endpoint Enable Control)

BIT	SYMBOL	DESCRIPTION
7-5	Reserved	must keep bits = "0"
4	USB_Speed	set "High" for Full Speed; set "Low" for Low Speed
3	EP1_EN	set "High" to enable Endpoint 1
2	EP2_EN	set "High" to enable Endpoint 2
1	EP3_EN	set "High" to enable Endpoint 3
0	EP4_EN	set "High" to enable Endpoint 4

Control Register 1: Address = 03H (Device Address Setting)

BIT	SYMBOL	DESCRIPTION
7	Bus_Connection	connect up stream port on USB Bus after chip initialization done
6-0	Device_Address[6:0]	Setup Device Address

Control Register 2: Address = 04H (FIFO Access Control)

BIT	SYMBOL	DESCRIPTION
7	Reserved	must keep bit = "0".
6	Set_Stall	Set Stall for EP 0 -4 (refer to section 7.4 for programming)

5	EP0_RD_EN	Set "High" before reading IN FIFO of EP0 (receiving Data from USB Bus)
4	EP0_WR_EN	Set "High" before writting OUT FIFO of EP0 (transmitting Data to USB Bus)
3	EP1_WR_EN	Set "High" before writting OUT FIFO of EP1 (transmitting Data to USB Bus)
2	EP2_WR_EN	Set "High" before writting OUT FIFO of EP2 (transmitting Data to USB Bus)
1	EP3_WR_EN	Set "High" before writting OUT FIFO of EP3 (transmitting Data to USB Bus)
0	EP4_WR_EN	Set "High" before writting OUT FIFO of EP4 (transmitting Data to USB Bus)

Control Register 3: Address = 05H (USB Event Control)

BIT	SYMBOL	DESCRIPTION
7	Reserved	must keep bit = "0"
6	NakEP0In_INT_EN	Enable interrupt event when NAK comes from EP0 for IN Transaction
5	Set_EP0NullData	set Null Data for IN Transaction of EP 0 (refer to section 7.5 for programming)
4	Warm_Reset	Active Warm Reset
3	Resume_Out	Send Resume command (K-state) to USB Bus (Set_Suspend should be “1”)
2	Set_Suspend	Set suspend mode active
1	Read_Event	Set "High" during reading Status Registers (refer to section 7.2 for programming)
0	Set_EP0_Nak	Set "High" for responsing Nak when IN/OUT Transaction of EP0 come

Control Register 4: Address = 08H (Interrupt Enable Control)

BIT	SYMBOL	DESCRIPTION
7-4	Reserved	must keep bits = "0"
3	Remote_Wakeup_EN	for Remote Wakeup Enable from Keystroke or Mouse moving
2	USB_EventINT_EN	for USB event interrupt enable
1	SCANOUT[17]	output port value of port SO17
0	SCANOUT[16]	output port value of port SO16

Control Register 5: Address = 09H (CPU Reset Control)

BIT	SYMBOL	DESCRIPTION
7-2	Reserved	must keep bit = "0"
1	UC_WarmReset_EN	set "High" for reseting CPU when Warm_Reset = "1"
0	DisconUSB_Bus_Disable	set "High" keeping device conecting with USB Bus during software or hardware reset set "Low" disconnecting with USB Bus during software or hardware reset

Control Register 6: Address = 0EH (Watch Dog Timer Reset)

BIT	SYMBOL	DESCRIPTION
7-0	Reset_WDT	Clear WDT = 00H when set Reset_WDT = AAH

6.3 Reset

The W81281 supports three types of reset. During a reset, all registers of the CPU core and USB return to their default status, and USB device address is set to zero.

6.3.1 External Reset (Hardware Reset)

As in 8051 series controller, the external RESET signal is sampled at S5P2. To take effect, it must be held high at least two machine cycles while the oscillator is running.

An internal trigger circuit in the reset line is used to deglitch the reset line. The reset logic also has a special glitch remocal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON(with exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

6.3.2 Warm Reset (Software Reset)

W81281 provides a warm reset by setting "High" at Warm_Reset bit of control register 3.

The W81281 handles the USB reset function independently from the CPU core. If a Single Ended Zero (SE0) is detected on the upstream port for greater then 2.5us, then the interrupt is enabled. The CPU core read flag from USB_Reset bit of status register 1 then CPU

- to reset the device address to 0, and enter the default state. No any reset timing occurs.

or

- to set "High" at Warm_Reset bit of control register

6.3.3 WDT Reset (Hardware Reset)

There is a Watch Dog Timer installed in W81C281. CPU should periodically clear WDT to 00H by setting Reset_WDT=AAH before WDT time out. If CPU hangs WDT will time-out and cause hardware reset.

6.4 USB SUSPEND

If there is no upstream activity for 3 msec then the Suspend_In flag is set and the interrupt enabled. When Suspend_In flag is read, CPU core actives power down mode for W81281 go into suspend

6.5 USB RESUME:

The suspend state can be exit by a 'resume'. The resume can occur by three methods.

- The host can send a resume to all ports by placing a 0 (K state) on the bus. The W81281 sees the resume, , and enables the interrupt. In this case, the CPU core does not have to perform any functions.
- The host can reset the bus.
- When any falling edge is detected on CPU port1(keystrokes). The CPU core will exit from power down mode and initiate a resume by setting Resume_Out in the Control Register 3 which will cause a K state to be sent. To un-resume, the CPU core must clear the Resume_Out bit in the Control Register 3.

7. PROGRAMMING NOTES:

The W81281 uses reserved bit of the Interrupt Priority Register IP.6 as a pre-decoding bit to implement a alternative register and FIFO by External Data Memory Access of CPU core. Programming functions described as below:

7.1 Control Registers Access:

Step 1: set IP.6 = 1

Step 2: access Control Register (by MOVX Instruction)

Step 3: set IP.6 = 0

7.2 Status Registers Access:

Step 1: set IP.6 = 1

Step 2 : set Read_Event = 1 in Control Register 3 (by MOVX Instruction)

step 3 : access Status Registers (by MOVX Instruction)

step 4 : set IP.6 = 0

7.3 FIFOs Access :

step 1 : set IP.6 = 1

step 2 : set EP0_RD_EN/EPX_WR_EN = 1 (X : 0 - 4) (by MOVX Instruction)

step 3 : access FIFO by address 06H of MOVX Instruction

step 4 : set EP0_RD_EN/EPX_WR_EN = 0 (X : 0 - 4) (by MOVX Instruction)

step 5 : set IP.6 = 0

7.4 Set Stall for Endpoint 0 - 4 :

step 1 : set IP.6 = 1

step 2 : set Set_Stall = 1 (by MOVX Instruction)

step 3 : set EP0_RD_EN/EPX_WR_EN = 1 (X : 0 - 4) (by MOVX Instruction)

step 4 : set EP0_RD_EN/EPX_WR_EN = 0 (X : 0 - 4) (by MOVX Instruction)

step 5 : set Set_Stall = 0 (by MOVX Instruction)

step 6 : set IP.6 = 0

Note : 1. EP0_RD_EN = 1 for OUT Transaction of EP0.

2. EP0_WR_EN = 1 for IN Transaction of EP0.

7.5 Set Null Data for IN Transaction of EP 0 :

step 1 : set IP.6 = 1

step 2 : set Set_EP0NullData = 1 (by MOVX Instruction)

step 3 : set EP0_WR_EN = 1 (by MOVX Instruction)

step 4 : set EP0_WR_EN = 0 (by MOVX Instruction)

step 5 : set Set_EP0NullData = 0 (by MOVX Instruction)

step 6 : set IP.6 = 0

8. ELECTRICAL CHARACTERISTICS & CAPACITANCE

(Ta = 0¢ to + 70¢ ,VDD = +5V ± 5%)

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT	NOTE
VDD	Power Support	4.0	5.0	5.5	V	
VIL	Input Low Voltage (except RESET)			0.8	V	
VIL1	Input Low Voltage (RESET)			0.6	V	
VIH1	Input High Voltage (except RESET)	2.0			V	
VIH2	Input High Voltage (RESET)	3.5			V	
VOH	Output High Voltage (except D+/D-)			2.4	V	IOH=-4mA
VOL	Output Low Voltage (except D+/D-)	0.4			V	IOL= 4mA
IOFL	Output Leakage Current (High-Z state)	-10		10	uA	
IIH	Input Leakage Current	-10		10	uA	VDD=5.5V VIN=VDD
IIL	Input Leakage Current	-10		10	uA	VDD=5.5V VIN=VSS

	Symbol	Conditions	Min	Max	Unit
D+/D- Leakage Current:					
Hi-Z State Data Line Leakage	ILO	0 V < VIN < 3.3V	-10	+10	µA
D+/D- Input Levels:					
Differential Input Sensitivity	VDI	|(D+)-(D-)|	0.2		V
Differential Common Mode Range	VCM	Includes VDI range	0.8	2.5	V
Single Endge Receiver Threshold	VSE		0.8	2.0	V
D+/D- Output Levels:					
Static Output Low	VOL	RL of 1.5kΩ to 3.6V		0.3	V
Static Output High	VOH	RL of 1.5kΩ to GND	2.8	3.6	V
D+/D- Capacitance:					
Transceiver Capacitance	CIN	Pin to GND		20	pF
D+/D- Driver Characteristics:					
Transition Time:					
Rise Time	TR	CL=50pF/350pF	75	300	ns
Fall Time	TF	CL=50pF/350pF	75	300	ns
Rise / Fall Time Matching	TRFM	(TR / TF)	80	125	%
Output Signal Crossover Voltage	VCRS		1.3	2.0	V
D+/D- Data Source Timings:					
Low Speed Data Rate	TDRATE	Ave.Bit Rate (1.5Mb/s ±1.5%)	1.4775	1.5225	Mbs
Source Differential Driver Jitter					
To Next Transition	TDJ1		-95	95	ns
For Paired Transitions	TDJ2		-150	150	ns
Source EOP Width	TEOPT		1.25	1.50	µs
Differential to EOP Transition Skew	TDEOP		-40	100	ns
D+/D- Data Receiver Timings:					
Receiver Data Jitter Tolerance					
To Next Transition	TDJR1		-75	75	ns
For Paired Transitions	TDJR2		-45	45	ns
Receiver SE0 Tolerance during Differential Transition	TLST			210	ns

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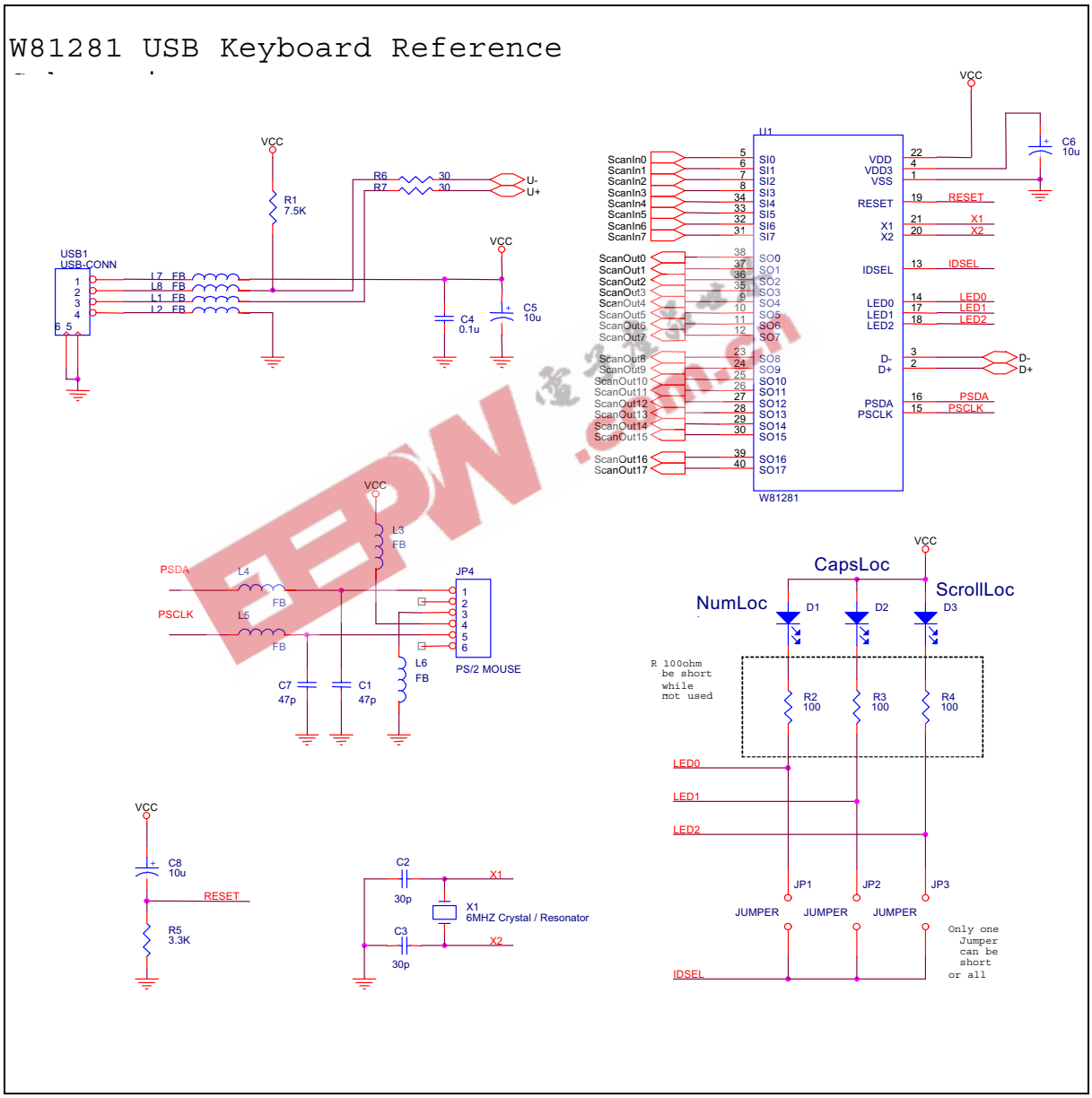
Revision 0.60

EOP Width at receiver					
Must reject as EOP	TEORP1		330		ns
Must accept as EOP	TEOPR2		675		ns

9. USB KEYBOARD SAMPLE APPLICATION

1. For 40 pin DIP package



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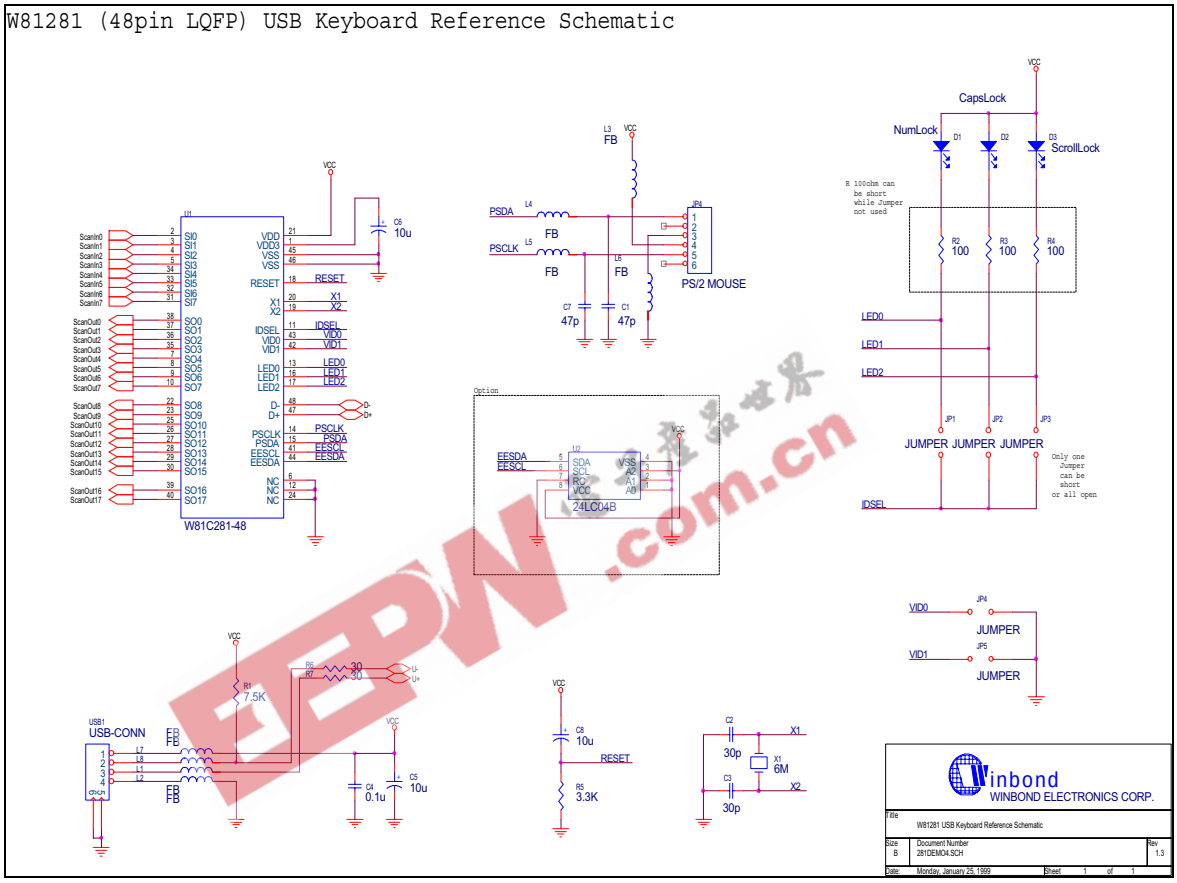
For 48 pin LQFP package reference circuit



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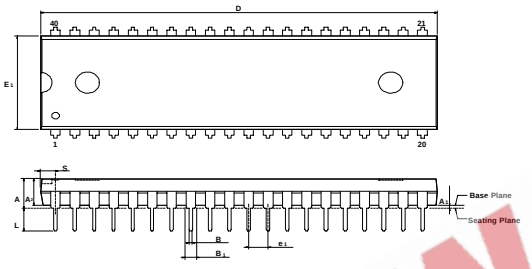
Revision 0.60

10. PACKAGE DIMENSIONS

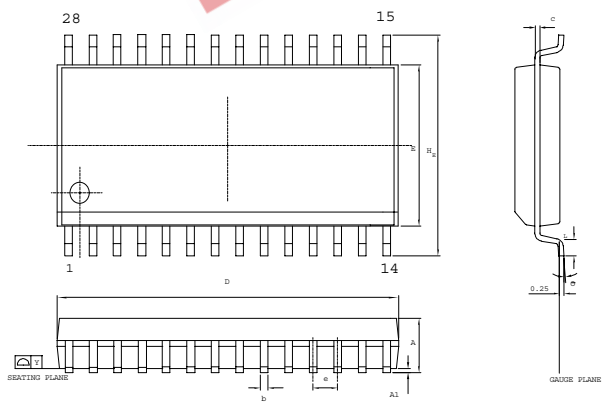
40-pin DIP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.090	—	—	2.29

Notes:
1. Dimensions D Max & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

28-pin SOP



Control demensions are in milme

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
E	7.40	7.60	0.291	0.299
D	17.70	18.10	0.697	0.713
e	1.27 BSC		0.050 BSC	
H_E	10.00	10.65	0.394	0.419
Y	—	0.10	—	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

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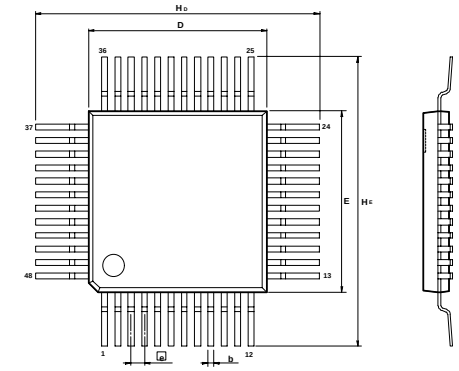
48-pin LQFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A				---	---	1.60
A_1				0.05	---	0.15
A_2				1.35	1.40	1.45
b				0.17	0.20	0.27
c				0.09	---	0.20
D					7.00	
E					7.00	
e					0.50	
H_D					9.00	
H_E					9.00	
L				0.45	0.60	0.75
L_1					1.00	
y				---	0.08	---
θ				0	3.5°	7

Notes:
1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

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Report No. : 500-8801-018
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ELECTROMAGNETIC SUSCEPTIBILITY TEST REPORT

Company : Winbond Electronics Corp.
Address : No.4, Creation Rd. Ⅲ, Science-Based Industrial Park
Hsinchu, Taiwan, R.O.C.
Sample Name : USB Keyboard
Model : W81281
Date Received : JAN. 11, 1999
Date Tested : JAN. 11, 1999

WE HEREBY CERTIFY THAT: The object of these measurements were made to establish a common and reproduciple basis for evaluating the performance of electrical and electronic equipment when were subjected to the immunity test. We assume full responsibility for the accuracy and completeness of these measurements and vouch for the qualifications of all persons taking them.

	Name	Signature	Date
Testing Engineer	J. S. Song	J. S. Song	
Approving Manager	Paul Y. Liau	Paul Y. Liau	Jan. 14, 1999

Notes :
1. This report will be invalid if duplicated or photocopied in part.
2. This report refers only to the specimen(s) submitted to test, and is invalid as seperately used.
3. This report is invalid without examination stamp and signature of this institute.
4. The tested specimen(s) will be preserved for thirty days from the date issued.

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2.4 Performance criteria

A. The equipment shall continue to operate as intended. No degradation of performance or loss of function is allowed below a performance level specified by the manufacturer.

B. After the test the equipment shall continue to operate as intended. No degradation of performance or loss of function is allowed after the application of the phenomena below a performance level specified by the manufacturer.

During the test, degradation of performance is allowed however. No change of actual operating state or stored data is allowed.

C. Loss of function is allowed, provided the function is self recoverable or can be restored by the operation of the controls by the user in accordance with the manufacturers instructions.

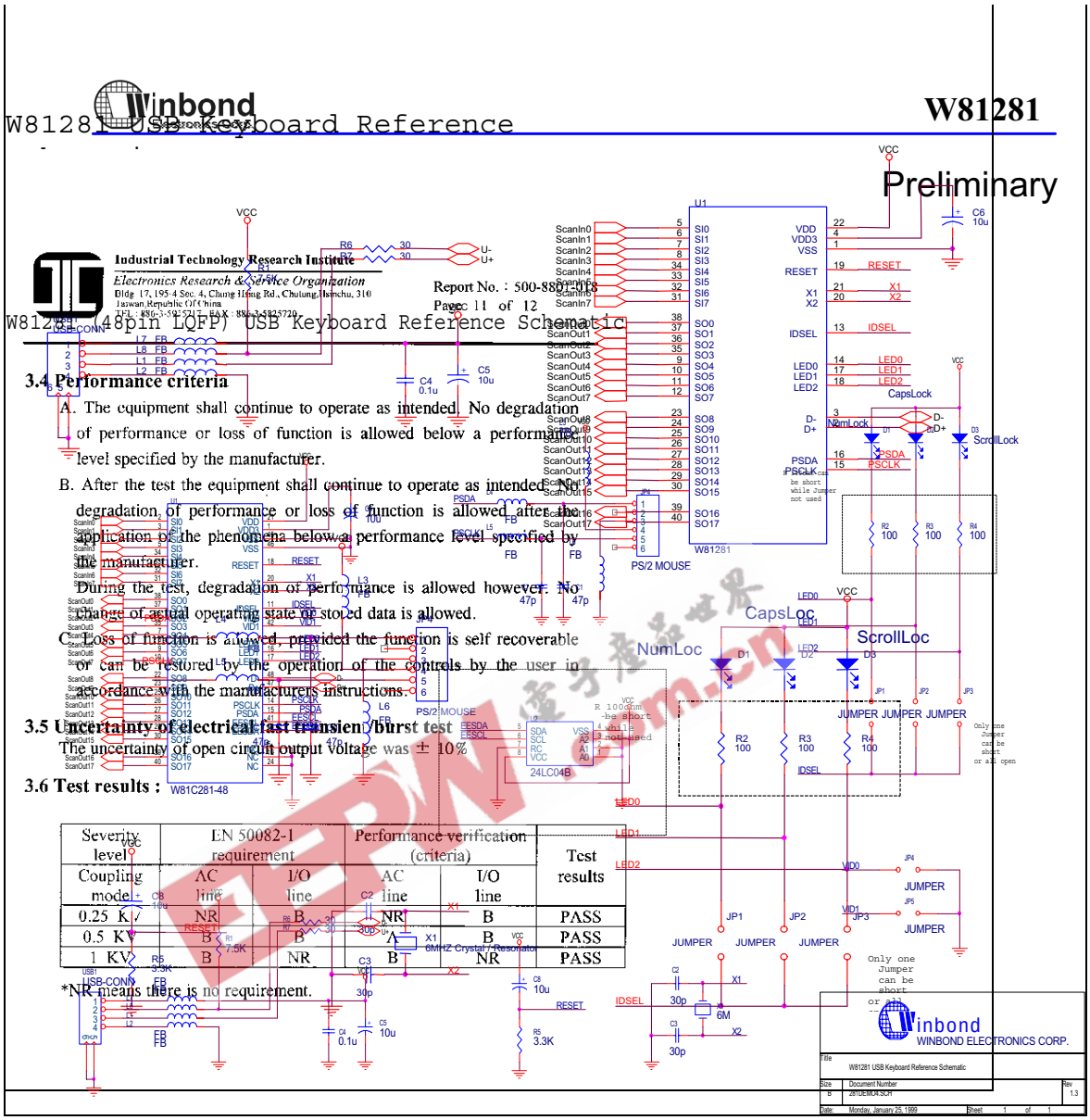
2.5 Uncertainty of electrostatic discharge test

The uncertainty of output voltage indication was ± 5%

2.6 Test results :

Severity level	EN 50082-1 requirement				Performance verification (criteria)				Test results
	Air discharge	Contact discharge	HCP discharge	VCP discharge	Air discharge	Contact discharge	HCP discharge	VCP discharge	
2 KV	B	B	B	B	A	A	A	A	Pass
4 KV	B	B	B	B	A	A	B	A	Pass
8 KV	B	NR	NR	NR	A	NR	NR	NR	Pass

*NR means there is no requirement



APPENDIX A: WINBOND(W81281-004) DEFAULT MATRIX CODE

VID: **0000** PID: **0801**(with PS/2 mouse) PID: **0802**(without PS/2 mouse)

101(AT)/102(Europe+Macro)(+Fn)/103(Korean)(Brazillian)/106(Japan.)+Windows 95 keys compatible

	SO0	SO1	SO2	SO3	SO4	SO5	SO6	SO7	SO8	SO9	SO10	SO11	SO12	SO13	SO14	SO15	SO16	SO17
SI0	***64*** ***K45*** *Macro*	24 7	14 Q	12 O	07 D	34 “	05 B	39 Caps	3F F6	60 P_8	5A P_2	***31*** ***K29*** \	EC	***8B*** ***K131*** *J-NCHG*	E1 Shift-L	F5	FA	EB
SI1	29 ESC	25 8	1A W	13 P	09 F	35 ~	11 N	2C SPC	40 F7	61 P_9	5B P_3	4A Home	Wake -up	E3 Win-L	***87*** ***K56*** *J-56*	***89*** ***K14*** *J-14*	F9	EE
SI2	1E 1	26 9	08 E	2F [	0A G	4D End	10 M	4E PgDn	41 F8	56 P_-	62 P_0	52 Up	E0 Ctrl-L	F1	01	01	***91*** ***K150*** *Kor0-L*	EA
SI3	1F 2	27 0	15 R	30]	0B H	***32*** ***K42*** \	36 <	3A F1	42 F9	5C P_4	63 P_.	4B PgUp	E4 Ctrl-R	F0	01	01	F8	***90*** ***K151*** *Kor1-R*
SI4	20 3	2D -	17 T	28 Enter	0D J	1D Z	37 >	3B F2	43 F10	5D P_5	58 P_Entr	48 Pause	Power	EF	E5 Shift-R	F4	***87*** ***K56*** *BZ0*	E5 Shift-R
SI5	21 4	2E +	1C Y	51 Down	0E K	1B X	38 ?	3C F3	53 Num	5E P_6	44 F11	50 Left	E9	Sleep	F3	E2 Alt-L	F7	***94*** ***K107*** *BZ1*
SI6	22 5	2A BKS	18 U	04 A	0F L	06 C	4C Del	3D F4	47 Scroll	57 P_+	45 F12	4F Right	E8	ED	F2	E6 Alt-R	E7 Win-R	FF
SI7	23 6	2B TAB	0C I	16 S	33 ;	19 V	55 *	3E F5	5F P_7	59 P_1	46 PrtScr	49 Ins	54 /	***8A*** ***K132*** *J-CHG*	65 APP	***88*** ***K133*** *J-ROMA*	F6	FB

NOTE 1: The contents in the table are hexadecimal HID codes and function descriptor.

2: Six are scan-in lines, Sox are scan-out lines.

3: The three ACPI power management keys for Windows 98 are Power (SI4-SO12), Sleep (SI5-SO13) and Wakeup (SI1-SO12).

Multimedia Buttons & Reserved Buttons (W81281-004)

HID Code	Functions (ref. Qtronix)
E8	Play/Pause
E9	Stop/Eject
EA	Rewind
EB	Forward
EC	Record
ED	Volume+
EE	Volume-
EF	Mute
F0	WWW
F1	Previous
F2	Next
F3	Stop
F4	Search
F5	Scroll-Up
F6	Scroll-Down
F7	Menu
F8	Suspend
F9	Coffee
FA	Xfer
FB	Calculator
FC	Reserved (On-Power)
FD	Reserved (On-Sleep)
FE	Reserved (On-Wakeup)
FF	Reserved

HID Codes vs. Legacy Scan-Codes (W81281-004)

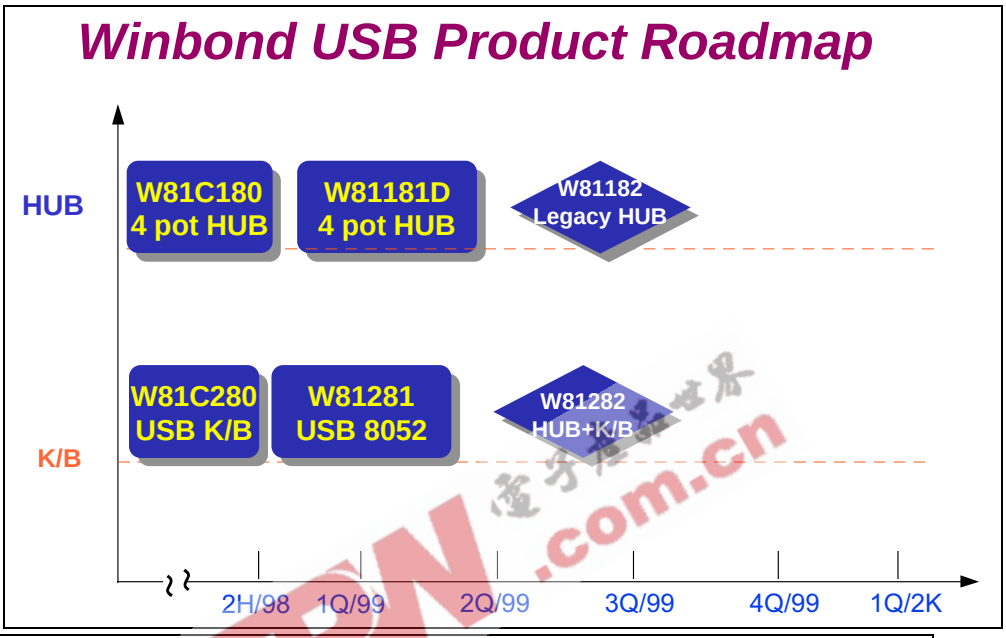
	SO0	SO1	SO2	SO3	SO4	SO5	SO6	SO7	SO8	SO9	SO10	SO11	SO12	SO13	SO14	SO15	SO16	SO17
SI0	***64*** ***K45*** ***56 61 13***	24 K8 08 3D 3D	14 K17 10 15 15	12 K25 18 44 44	07 K33 20 23 23	34 K41 28 52 52	05 K50 30 32 32	39 K30 3A 58 14	3F K117 40 0B 2F	60 K96 48 75 75	5A K98 50 72 72	***31*** ***K29*** ***2B 5D 5C***	EC	***8B*** ***K131*** ***7B 67 85***	E1 K44 2A 12 12	F5	FA	EB
SI1	29 K110 01 76 08	25 K9 09 3E 3E	1A K18 11 1D 1D	13 K26 19 4D 4D	09 K34 21 2B 2B	35 K1 29 0E 0E	11 K51 31 31 31	2C K61 39 29 29	40 K118 41 83 37	61 K101 49 7D 7D	5B K103 51 7A 7A	4A K80 47 6C 6E	63 5E	E3 K127 5B 1F 8B	***87*** ***K56*** ***73 51 51***	***89*** ***K14*** ***7D 6A 5D***	F9	EE
SI2	1E K2 02 16 16	26 K10 0A 46 46	08 K19 12 24 24	2F K27 1A 54 54	0A K35 22 34 34	4D K81 4F 69 65	10 K52 32 3A 3A	4E K86 51 7A 6D	41 K119 42 0A 3F	56 K105 4A 7B 84	62 K99 52 70 70	52 K83 48 75 63	E0 K58 1D 14 11	F1	01	01	***91*** ***K150*** ***F1 F1 F1***	EA
SI3	1F K3 03 1E 1E	27 K11 0B 45 45	15 K20 13 2D 2D	30 K28 1B 5B 5B	0B K36 23 33 33	***32*** ***K42*** ***2B 5D 53***	36 K53 33 41 41	3A K112 3B 05 07	42 K120 43 01 47	5C K92 4B 6B 6B	63 K104 53 71 71	4B K85 49 7D 6F	E4 K64 1D 14 58	F0	01	01	F8	***90*** ***K151*** ***F0 F2 F2***
SI4	20 K4 04 26 26	2D K12 0C 4E 4E	17 K21 14 2C 2C	28 K43 1C 5A 5A	0D K37 24 3B 3B	1D K46 2C 1A 1A	37 K54 34 49 49	3B K113 3C 06 0F	43 K121 44 09 4F	5D K97 4C 73 73	58 K108 1C 5A 79	48 K126 FF FF 62	5E 37	EF	E5 K57 36 59 59	F4	***87*** ***K56*** ***73 51 51***	E5 K57 36 59 59
SI5	21 K5 05 25 25	2E K13 0D 55 55	1C K22 15 35 35	51 K84 50 72 60	0E K38 25 42 42	1B K47 2D 22 22	38 K55 35 4A 4A	3C K114 3D 04 17	53 K90 45 77 76	5E K102 4D 74 74	44 K122 57 78 56	50 K79 4B 6B 61	E9	5F 3F	F3	E2 K60 38 11 19	F7	***94*** ***K107*** ***7E 6D 7B***
SI6	22 K6 06 2E 2E	2A K15 0E 66 66	18 K23 16 3C 3C	04 K31 1E 1C 1C	0F K39 26 4B 4B	06 K48 2E 21 21	4C K76 53 71 64	3D K115 3E 0C 1F	47 K125 46 7E 5F	57 K106 4E 79 7C	45 K123 58 07 5E	4F K89 4D 74 6A	E8	ED	F2	E6 K62 38 11 39	E7 K128 5C 27 8C	FF
SI7	23 K7 07 36 36	2B K16 0F 0D 0D	0C K24 17 43 43	16 K32 1F 1B 1B	33 K40 27 4C 4C	19 K49 2F 2A 2A	55 K100 37 7C 7E	3E K116 3F 03 27	5F K91 47 6C 6C	59 K93 4F 69 69	46 K124 37 7C 57	49 K75 52 70 67	54 K95 35 4A 77	***8A*** ***K132*** ***79 64 86***	65 K129 5D 2F 8D	***88*** ***K133*** ***70 13 87***	F6	FB

NOTE: The contents in the table are hexadecimal HID Code + Order Number of Legacy Keys + Legacy Scan-Code (set1 set2 set3).

Winbond Electronics Corp.

Preliminary

Winbond USB Product Roadmap



Winbond USB Product Brief

- W81C180: USB 4 Port Hub Controller
- W81181D: High Integrated USB 4 Port Hub Controller
- W81182:USB Legacy Hub, Translate EPP, Serial, PS/2 to USB Connection, Including 4 port USB Hub
- W81C280: USB K/B Controller
- W81281: High Integrated USB+8052 Controller or USB K/B Controller
- W81282:USB 4 Port Hub + K/B Controller

Preliminary

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