



# 256K x 16 Static RAM

## Features

- High speed
  - $t_{AA} = 12ns$
- 2.0V Data Retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with CE and OE features

## Functional Description

The WCFS4016V1C is high-performance CMOS Static RAMs organized as 262K words by 16 bits.

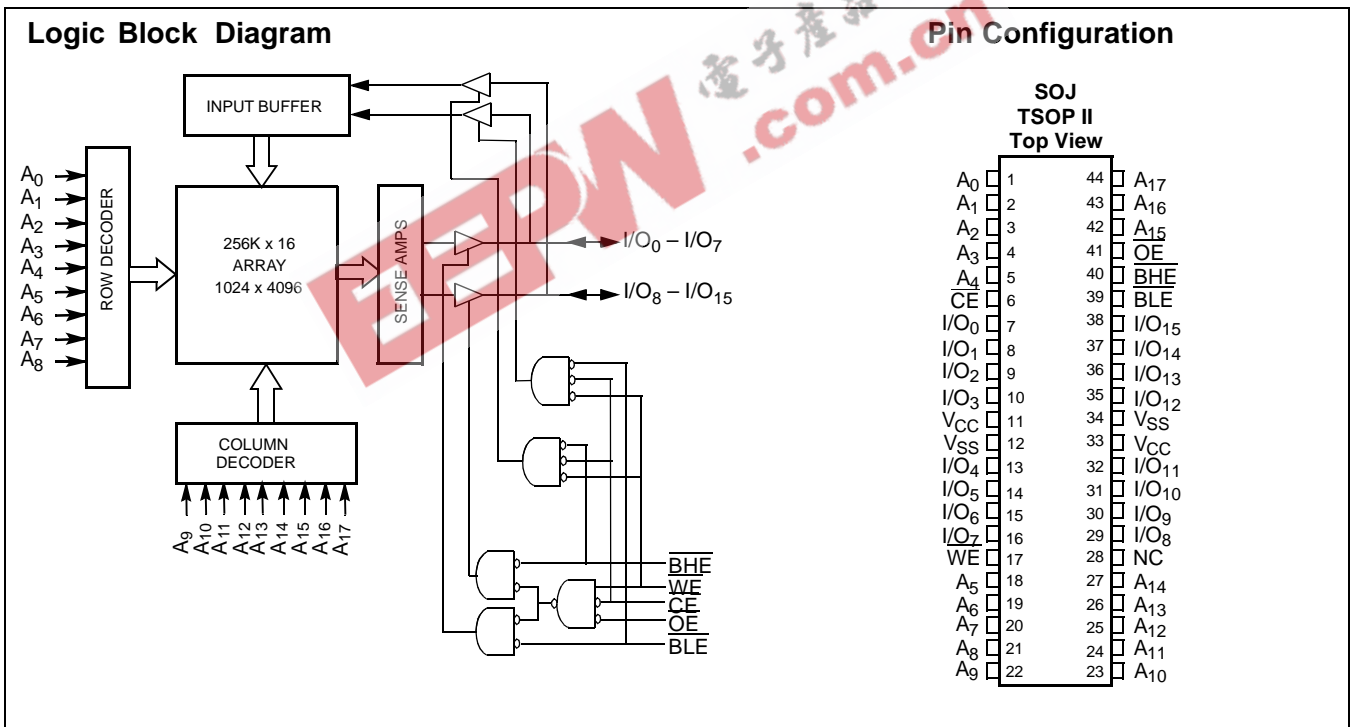
Writing to the devices is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>). If Byte High Enable (BHE) is LOW, then data

from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>).

Reading from the devices is accomplished by taking Chip Enable (CE) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation (CE LOW, and WE LOW).

The WCFS4016V1C is available in a standard 44-pin 400-mil-wide body width SOJ and 44-pin TSOP II package with center power and ground pinout.



## Selection Guide

		WCFS4016V1C 12ns
Maximum Access Time (ns)		12
Maximum Operating Current (mA)	Comm'l	85
Maximum CMOS Standby Current (mA)	Comm'l	10



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied ..... -55°C to +125°C  
 Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[1]</sup> .... -0.5V to +4.6V  
 DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

DC Input Voltage<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V  
 Current into Outputs (LOW) ..... 20 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	3.3V ± 0.3V

**DC Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	12ns		Unit
			Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.3	0.8	V
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		85	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		40	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0		10	mA

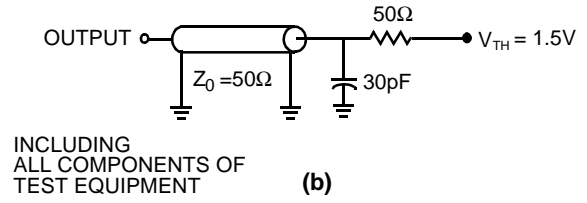
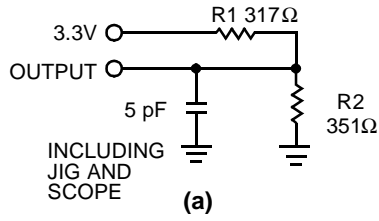
**Capacitance<sup>[2]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.3V	8	pF
C <sub>OUT</sub>	I/O Capacitance		8	pF

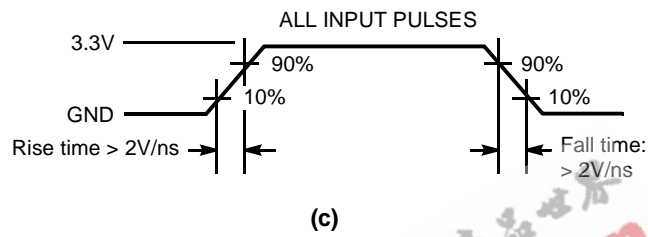
**Note:**

- V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



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**AC Switching Characteristics<sup>[3]</sup> Over the Operating Range**

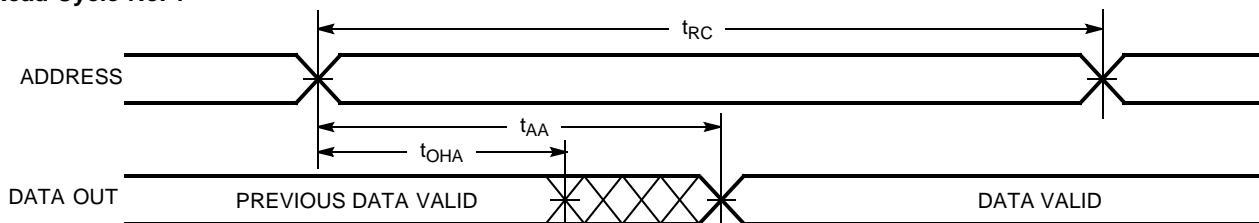
Parameter	Description	WCFS4016V1C 12ns		Unit
		Min.	Max.	
<b>READ CYCLE</b>				
$t_{power}^{[4]}$	$V_{CC}$ (typical) to the first access	1		$\mu s$
$t_{RC}$	Read Cycle Time	12		ns
$t_{AA}$	Address to Data Valid		12	ns
$t_{OHA}$	Data Hold from Address Change	3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		12	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		6	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[5, 6]</sup>		6	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[5, 6]</sup>		6	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		12	ns
$t_{DBE}$	Byte Enable to Data Valid		6	ns
$t_{LZBE}$	Byte Enable to Low Z	0		ns
$t_{HZBE}$	Byte Disable to High Z		6	ns
<b>WRITE CYCLE<sup>[7, 8]</sup></b>				
$t_{WC}$	Write Cycle Time	12		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	8		ns
$t_{AW}$	Address Set-Up to Write End	8		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Set-Up to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	8		ns
$t_{SD}$	Data Set-Up to Write End	6		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>		6	ns
$t_{BW}$	Byte Enable to End of Write	8		ns

**Notes:**

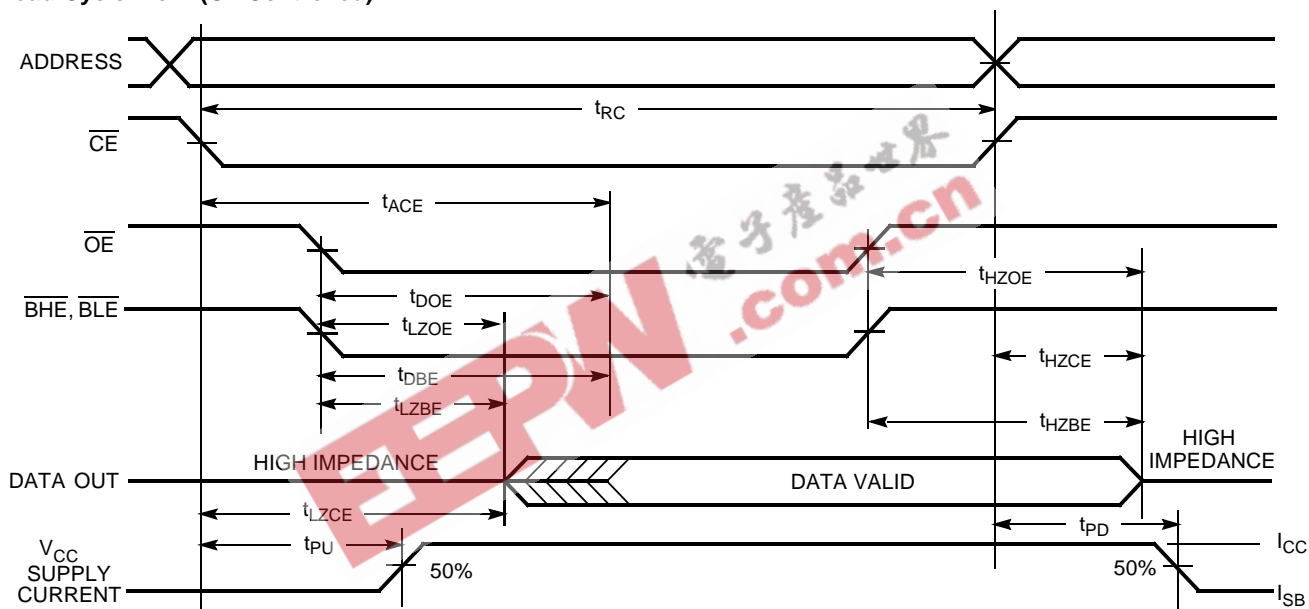
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
- $t_{POWER}$  gives the minimum amount of time that the power supply should be at typical  $V_{CC}$  values until the first memory access can be performed.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5pF as in part (a) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

### Switching Waveforms

Read Cycle No. 1<sup>[9, 10]</sup>



Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[10, 11]</sup>

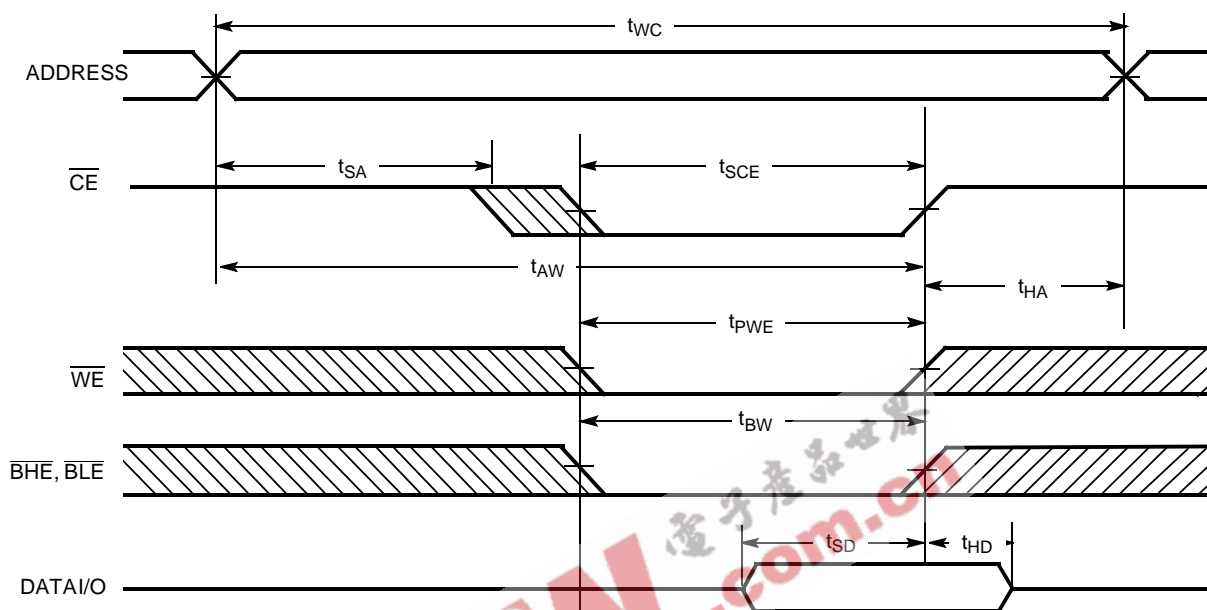


**Notes:**

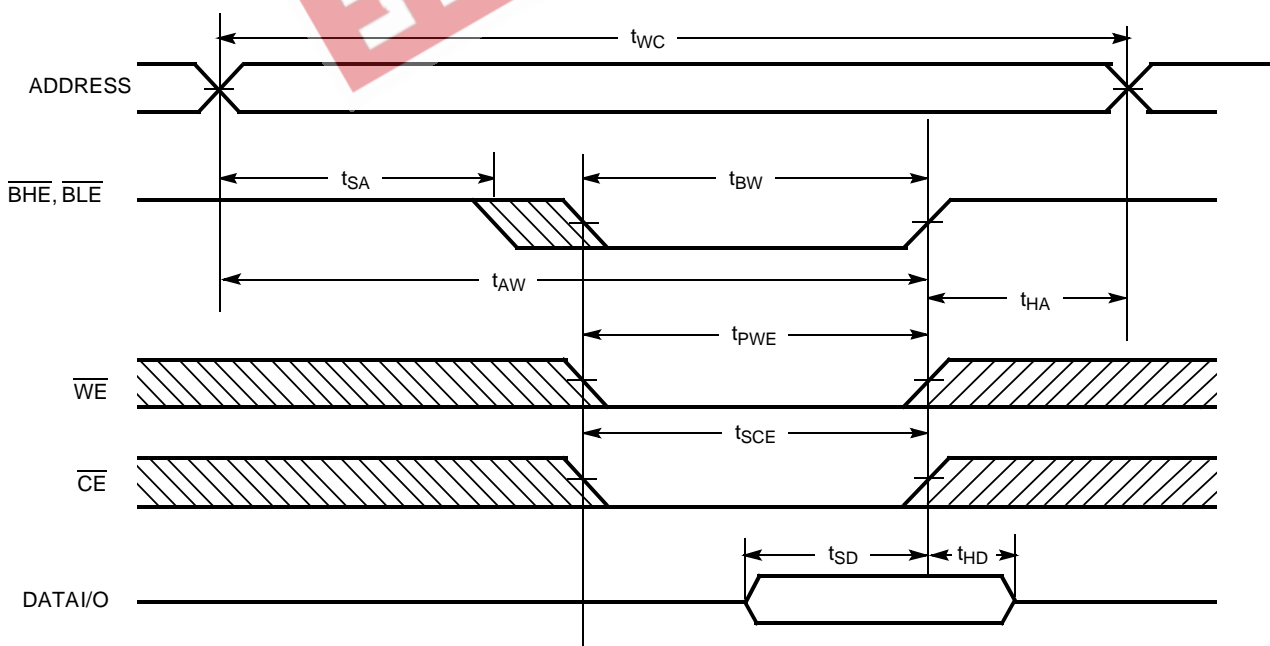
- 9. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ .
- 10.  $\overline{WE}$  is HIGH for read cycle.
- 11. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[12, 13]</sup>



Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)



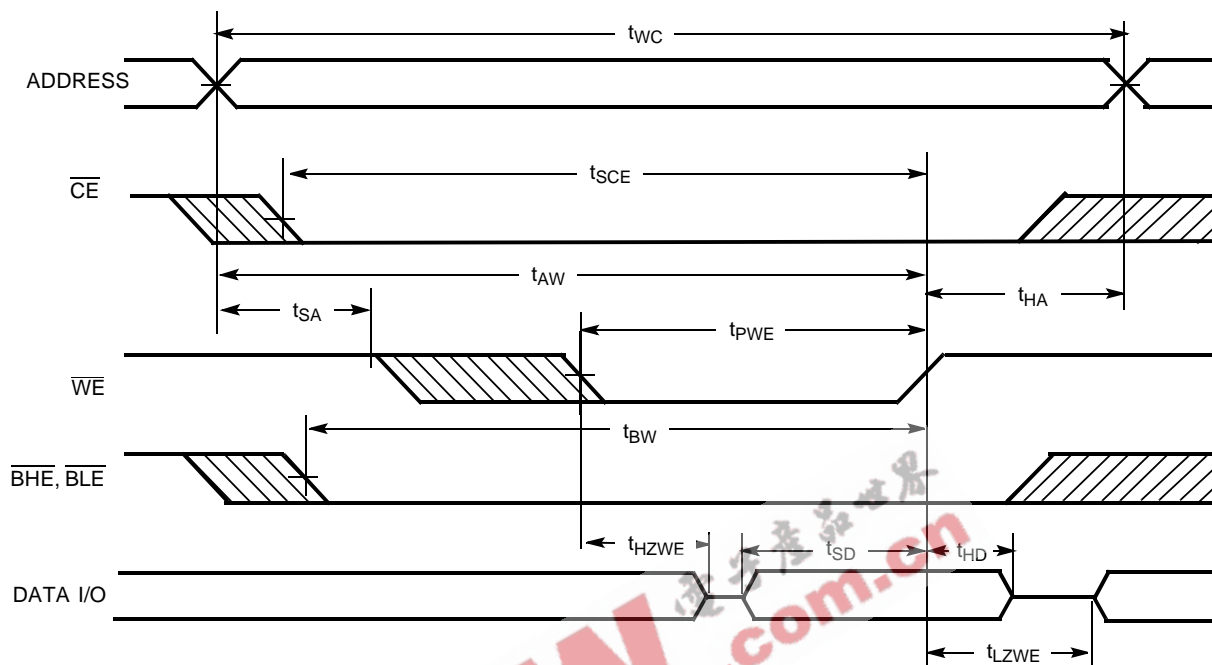
Notes:

12. Data I/O is high-impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IH}$ .
13. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.



Switching Waveforms (continued)

Write Cycle No.3 (WE Controlled, OE LOW)



Truth Table

CE	OE	WE	BLE	BHE	I/O <sub>0</sub> -I/O <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby (I <sub>SB</sub> )
L	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I <sub>CC</sub> )
L	L	H	L	H	Data Out	High Z	Read Lower Bits Only	Active (I <sub>CC</sub> )
L	L	H	H	L	High Z	Data Out	Read Upper Bits Only	Active (I <sub>CC</sub> )
L	X	L	L	L	Data In	Data In	Write All Bits	Active (I <sub>CC</sub> )
L	X	L	L	H	Data In	High Z	Write Lower Bits Only	Active (I <sub>CC</sub> )
L	X	L	H	L	High Z	Data In	Write Upper Bits Only	Active (I <sub>CC</sub> )
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

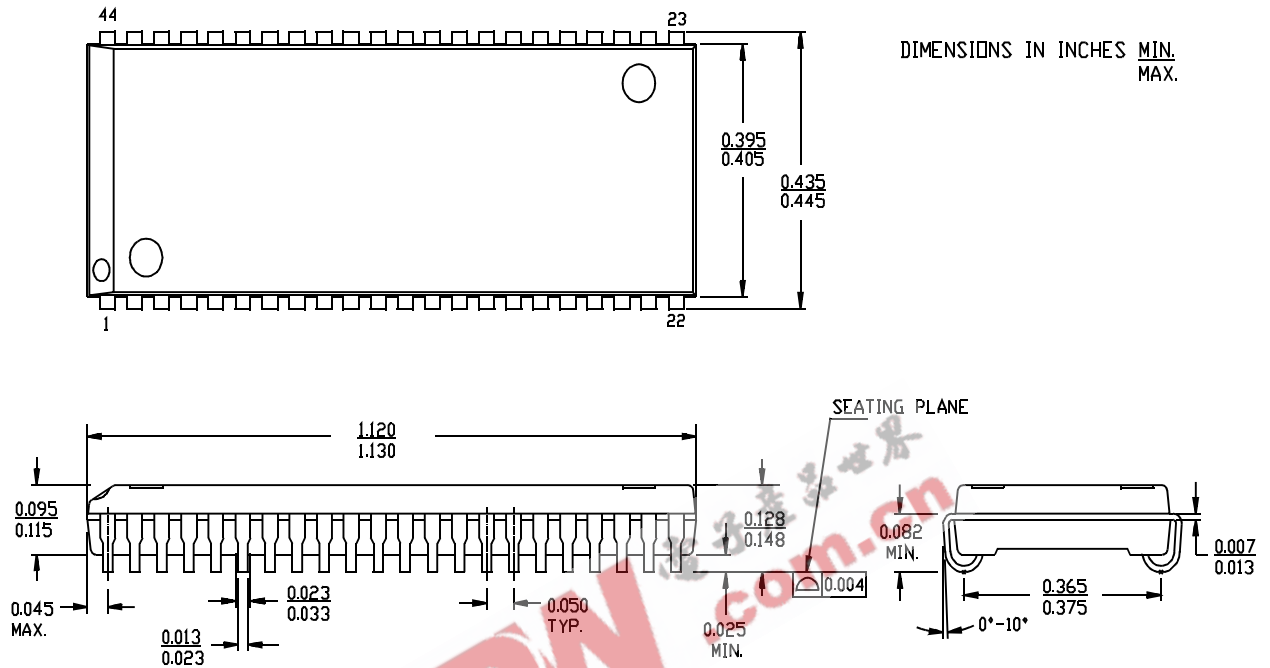
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	WCFS4016V1C-JC12	J	44-Lead (400-Mil) Molded SOJ	Commercial
	WCFS4016V1C-TC12	T	44-Pin TSOP II	



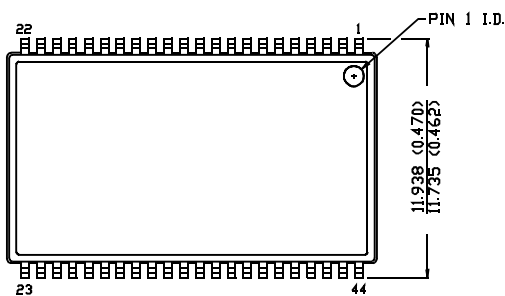
Package Diagrams

44-Lead (400-Mil) Molded SOJ J

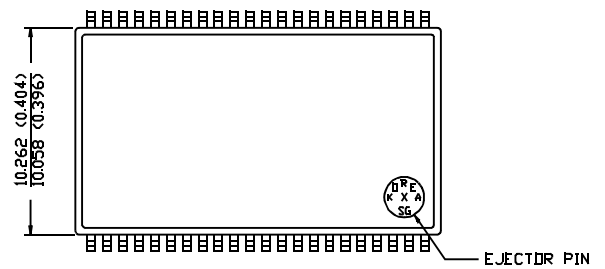


44-Pin TSOP II T

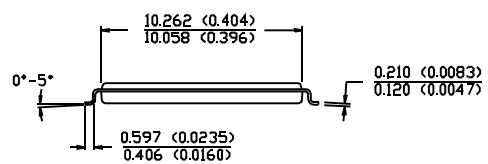
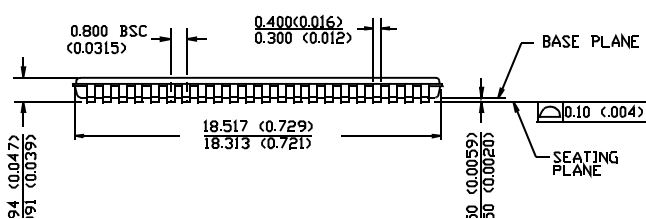
DIMENSION IN MM (INCH)  
MAX MIN.



TOP VIEW



BOTTOM VIEW







**Revision History**

Document Title: WCFS4016V1C 32K x 8 3.3V Static RAM			
REV.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE
**	4/12/2002	XFL	New Datasheet

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