

W83304D/W83304G



Winbond
ACPI Controller
W83304D
W83304G

For AMD Claw Hammer™ CPU

W83304D/W83304G



W83304D Data Sheet Revision History

	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1		June/04	0.50	N/A	Preliminary Version
2		April/06	0.51	N/A	Add Pb-free part no of W83304G
3					
4					
5					
6					
7					
8					

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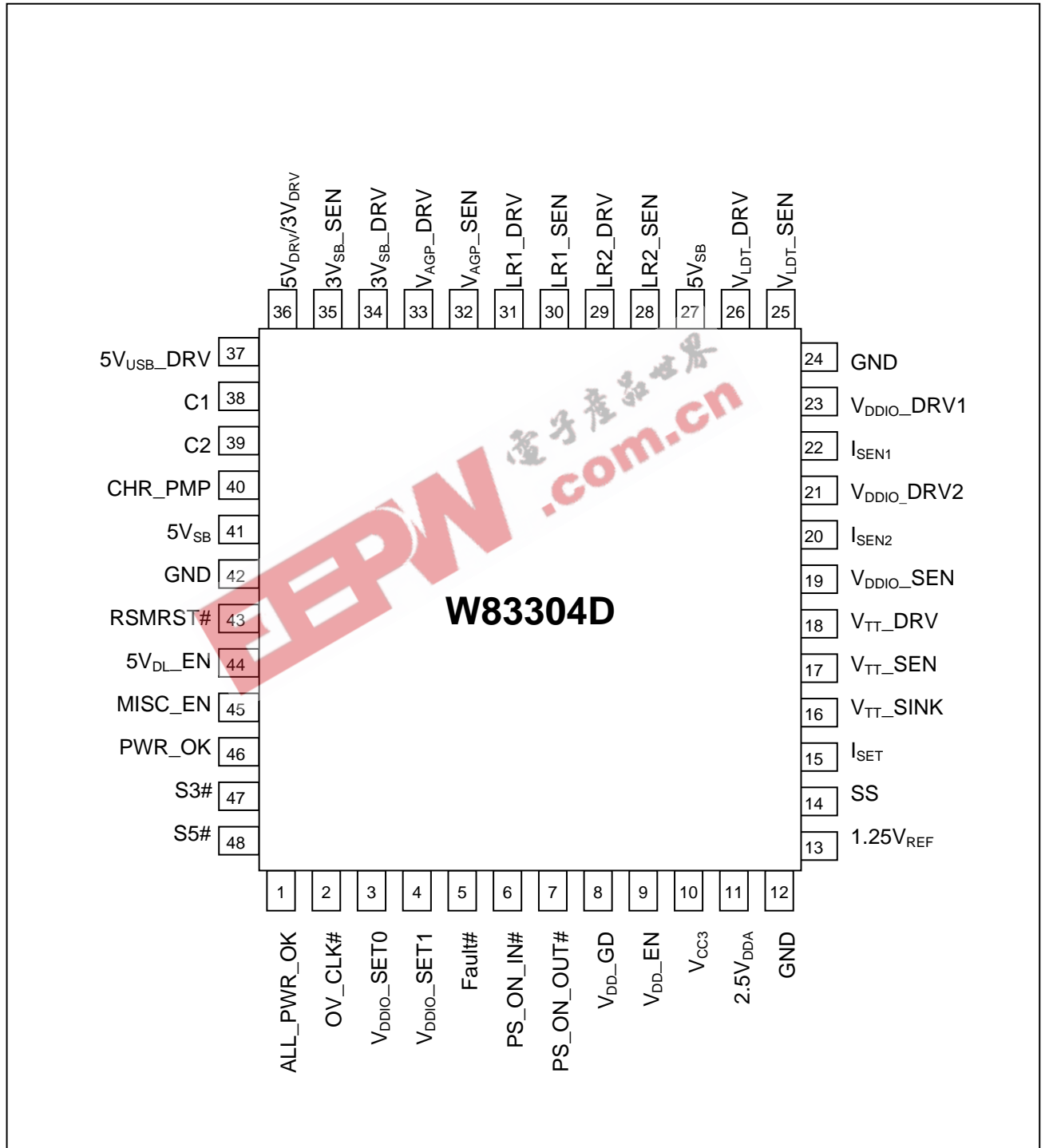
1. GENERAL FUNCTION DESCRIPTION

- Provides Powers
 - 5V Active/Sleep ($5V_{DL}$)
 - Provide a switch $5V_{DLEN}$ pin to enable/disable $5V_{DL}$ output in S5 state for USB application.
 - 3.3V Active/Sleep (3.3VDUAL)
 - Dual-Channel 2.5V Active/Sleep (2.5VSTR) for DDR
 - 1.5V for AGP 4X/8X Voltage
 - Two 1.25V~5V Linear Voltage Regulators Support VCC/VSTR/VDL/VS_B Voltages
 - 1.25V DDR Bus Termination Regulated Voltage
 - 1.2V VLDT for AMD_K8 CPU Hyper transport.
 - 2.5VDDA for AMD_K8 PLL.
 - 1.25VREF for AMD_K8 reference.
 - Up to 0.3V/0.1V incremental voltage on DDR RAM for over-clocking application.
- Provides Signals for ATX Power Supply PS_ON# Control
- Support AMD K8 Claw Hammer Specific Power Up/Down Sequence
- Provides fault signal control.
- Internal Charge Pump Support Up to 9.5V_{SB}
- Drive All N-Channel MOSFET
- Soft Start
- Under-Voltage Monitoring for VAGP, VRAM, VLDT, 3.3VDUAL Channels

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2. PIN-OUT





3. PIN DESCRIPTIONS

- I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability, open drain output
- I/O_{12ts} - TTL level and schmitt trigger
- O₁₂ - Output pin with 12 mA source-sink capability
- AO₁₂ - Output pin (Analog) with 12mA capability
- OD₁₂ - Open-drain output pin with 12 mA sink capability
- IN_t - TTL level input pin
- IN_{ts} - TTL level input pin and schmitt trigger
- AIN - Input pin (Analog)

NO	NAME	I/O	POWER SOURCE	FUNCTION DESCRIPTION															
1	ALL_PWR_OK	OD ₂₄	5VSB	Power OK Signal. The signal is drove high to indicate all power ready.															
2	OV_CLK#	I	5VSB	H/W Trapping Pin for Over-Clocking Application. 1: Normal 0: +50mV is added on All regulated powers (V _{DDIO} , V _{DDA} , V _{AGP} , V _{LDT} , 1.25V _{REF}).															
3	V _{DDIO_SET0}	I _{ts}	5VSB	VDDIO Output Voltage Setting Pin. V _{DDIO} output with OV_CLK# = High <table border="1" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>V_{DDIO_SET1}</th> <th>V_{DDIO_SET0}</th> </tr> </thead> <tbody> <tr> <td>2.5V</td> <td>0</td> <td>0</td> </tr> <tr> <td>2.6V</td> <td>0</td> <td>1</td> </tr> <tr> <td>2.7V</td> <td>1</td> <td>0</td> </tr> <tr> <td>2.8V</td> <td>1</td> <td>1</td> </tr> </tbody> </table>		V _{DDIO_SET1}	V _{DDIO_SET0}	2.5V	0	0	2.6V	0	1	2.7V	1	0	2.8V	1	1
	V _{DDIO_SET1}	V _{DDIO_SET0}																	
2.5V	0	0																	
2.6V	0	1																	
2.7V	1	0																	
2.8V	1	1																	
4	V _{DDIO_SET1}	I _{ts}	5VSB	V _{DDIO} output with OV_CLK# = Low <table border="1" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>VRAMSET1</th> <th>VRAMSET0</th> </tr> </thead> <tbody> <tr> <td>2.55V</td> <td>0</td> <td>0</td> </tr> <tr> <td>2.65V</td> <td>0</td> <td>1</td> </tr> <tr> <td>2.75V</td> <td>1</td> <td>0</td> </tr> <tr> <td>2.85V</td> <td>1</td> <td>1</td> </tr> </tbody> </table>		VRAMSET1	VRAMSET0	2.55V	0	0	2.65V	0	1	2.75V	1	0	2.85V	1	1
	VRAMSET1	VRAMSET0																	
2.55V	0	0																	
2.65V	0	1																	
2.75V	1	0																	
2.85V	1	1																	
5	Fault#	I _{ts}		System Fault Input Signal. Pull the pin low when any critical event alerted; the chip will shut the system down when the signal pulled low.															
6	PS_ON_IN#	I _{ts}		ATX PS_ON# Signal Input.															
7	PS_ON_OUT#	OD ₁₂		The PS_ON# signal of ATX power supply is routed through the chip for power fault control.															

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Pin Descriptions, continued

NO	NAME	I/O	POWER SOURCE	FUNCTION DESCRIPTION
8	V _{DD_GD}	I	5VSB	CPU Power Good Signal. The signal is inputted for power sequence control.
9	V _{DD_EN}	OD ₂₄	5VSB	Signal Output to Enable CPU Power. The signal output to enable CPU power for sequence control.
10	V _{CC3}	P		Power V_{CC}.
11	2.5V _{DDA}	AO _{200mA}	VCC3	2.5V Power for CPU PLL Core.
12	GND	P		Power Ground.
13	1.25V _{REF}	AO _{5mA}	3VSB	1.25V Reference Voltage.
14	SS	AI/AO	5VSB	Soft-Start Pin. A capacitor (0.1u) is attached in this pin for soft-start slope rate adjustment.
15	I _{SET}	AI/AO	5VSB	Reference Current Input. An input current for internal circuit reference.
16	V _{TT_SINK}	AO	5VSB	Power V_{TT}.
17	V _{TT_SEN}	AI	5VSB	A bi-direction linear regulator is provided to regulate voltage for DDR bus terminator.
18	V _{TT_DRV}	AO	9VSB	
19	V _{DDIO_SEN}	AI	9VSB	Power V_{DDIO}. A dual-channels linear regulator with current balancing architecture is provided for higher current DDR SDRAM application.
20	I _{SEN2}	AI		
21	V _{DDIO_DRV2}	AO		
22	I _{SEN1}	AI		
23	V _{DDIO_DRV1}	AO		
24	GND	P		Power Ground.
25	V _{LDT_SEN}	AI	5VSB	Power V_{LDT}.
26	V _{LDT_DRV}	AO	9VSB	1.2V power for LDT bus.
27	5V _{SB}	P		Standby Power Pin.
28	LR2_SEN	AI	5VSB	Linear Regulator 1.
29	LR2_DRV	AO	9VSB	A general purpose linear regulator is provided to generate 1.2V~5.0V power for specific device.
30	LR1_SEN	AI	5VSB	Linear Regulator 2.
31	LR1_DRV	AO	9VSB	A general purpose linear regulator is provided to generate 1.2V~5.0V power for specific device.

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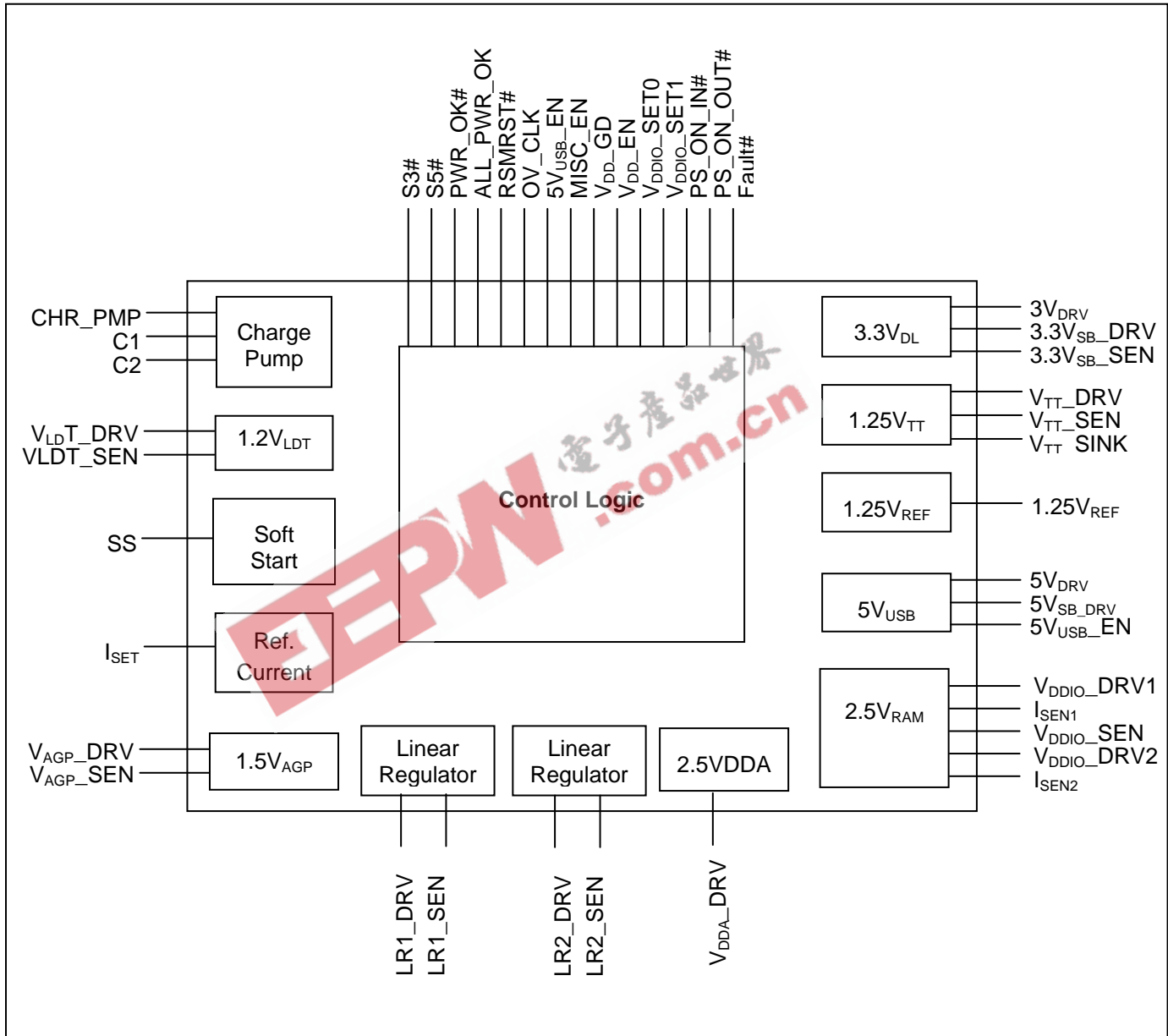
Pin Descriptions, continued

NO	NAME	I/O	POWER SOURCE	FUNCTION DESCRIPTION
32	V _{AGP_SEN}	AI	5VSB	Power for AGP Core. 1.5V power is regulated for AGP core.
33	V _{AGP_DRV}	AO	9VSB	
34	3V _{SB_DRV}	AO	9VSB	Power 3.3V_{DL}. A linear regulator and switch is combined to generate 3V dual power.
35	3V _{SB_SEN}	AI	5VSB	
36	5V _{DRV/3V_{DRV}}	AO	9VSB	
36	5V _{DRV/3V_{DRV}}	AO	9VSB	Power for USB Device. A 5V switch power is provided for USB device and can be programmed for various USB application with configuration of pin 44.
37	5V _{USB_DRV}	AO	9VSB	
38	C1	I	5VSB	Charge Pump Pins. It supports achieve 10mA driving current and insures output voltage 9.5V or above.
39	C2	I	5VSB	
40	CHR_PMP	P	5VSB	
41	5V _{SB}	P		Standby Power Pin.
42	GND			Power Ground.
43	RSMRST#	OD ₁₂		Signal to Indicate Status of Standby Power. The signal will be pulled high to indicate the standby power stable.
44	5V _{DL_EN}	I	5VSB	5VUSB Power Type Setting Pin. 5V _{USB_EN} =Low, support power for USB device in S0, S3 state. 5V _{USB_EN} =High, support power for USB device in S0, S3, S5 state.
45	MISC_EN	OD ₂₄	5VSB	Signal to Enable Miscellaneous Power.
46	PWR_OK	I _{ts}	5VSB	Power OK Signal form ATX Power Supply.
47	S3#	I		ACPI Control Signals.
48	S5#	I		

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4. BLOCK DIAGRAM





5. ELECTRICAL SPECIFICATION

5.1 AC CHARACTERISTICS

$V_{CC}=5V \pm 5\%$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VAGP Linear Regulator						
Nominal Output Voltage			1.5		V	OVA#=1
Nominal Output Voltage			1.55		V	OVA#=0
Regulation				5	%	
Under-Voltage Falling Threshold			86.67		%	
1.25VREF						
Nominal Output Voltage			1.25			$I_{load} < 5mA$; OVA#=1
Nominal Output Voltage			1.3			$I_{load} < 5mA$; OVA#=0
1.2VLDT Linear Regulator						
Nominal Output Voltage			1.2		V	OVA#=1
Nominal Output Voltage			1.25		V	OVA#=0
Regulation				5	%	
Under-Voltage Falling Threshold			87.5		%	
VDDIO Regulator						
VRAMSET0	VDDIO VOLTAGE SETTING OVA#=1					
VRAMSET1			VRAMSET1			VRAMSET0
	2.5V		0			0
	2.6V		0			1
	2.7V		1			0
	2.8V		1			1
	VDDIO VOLTAGE SETTING OVA#=0					
			VRAMSET1			VRAMSET0
	2.55V		0			0
2.65V		0			1	
2.75V		1			0	
2.85V		1			1	
Under-Voltage Falling Threshold			84		%	
Regulation				5	%	

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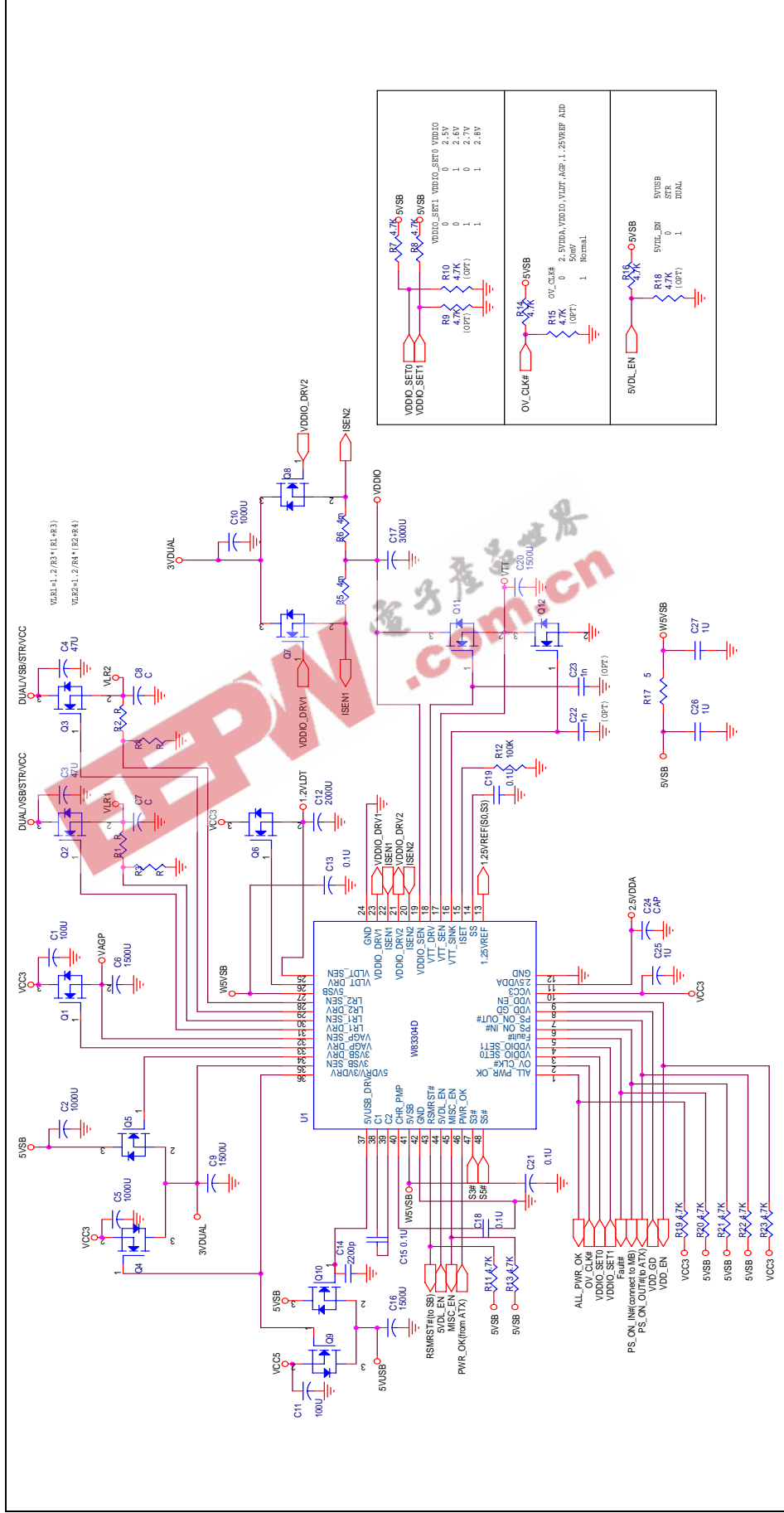


AC CHARACTERISTICS, continued

V_{CC}=5V ± 5 %, T_A = 0°C to +70°C						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
2.5VDDA						
Nominal Output Voltage			2.5			I _{load} < 200mA; OVA#=1
Nominal Output Voltage			2.55			I _{load} < 200mA; OVA#=0
Bus Terminator						
Nominal Output Voltage / V(VRAM2.5_SEN)			50		%	Regulate a 1.25V for DDR bus termination Half of VDDIO voltage
Nominal Output Voltage			1.25		V	
5VDUAL Switch Controller						
5VDRV Output High Voltage		9				Cap Loading
5VSBDRV Output High Voltage		9				Cap Loading
5VUSB SS Sourcing Current			2.5		uA	@ Soft-start
3.3VDual						
Under-Voltage Falling Threshold			78.79		%	
5VDRV Output High Voltage		9			V	
3VSBDRV		3.3				Regulation
Charge Pump						
Charge Pump Frequency			180		KHz	
Charge Pump Voltage		9.5				
Two linear regulator						
Nominal Output Voltage	Linear regulator from 1.2V~5V					

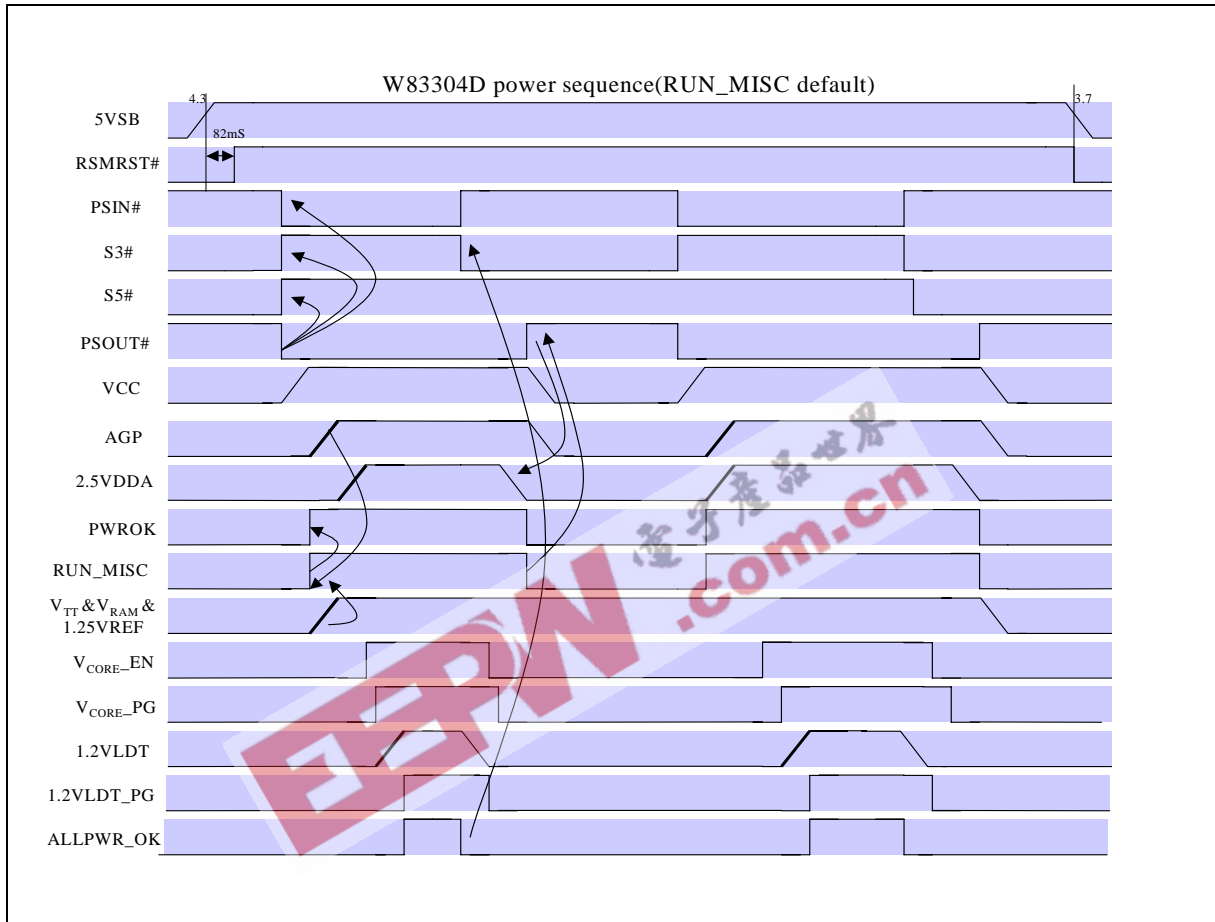


6. APPLICATION CIRCUIT





7. POWER SEQUENCE



Note:

1. When at power up sequence, the delay time between adjacent power planes is 5ms after the previous power plane is power-good.
2. When at power down sequence, the delay time between adjacent power planes is 20ms after the previous power plane is power-down.
3. After 1.2VLDT_PG=H and delay 20ms, the ALLPWR_OK will be High(ALLPWR_OK=H).
4. All "LUV" detect is enabled after the power plane have power-good.

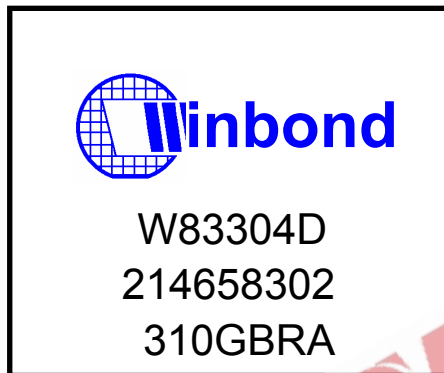
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8. ORDERING INSTRUCTION

PART NO.	PACKAGE	REMARKS
W83304D	48-pin LQFP	
W83304G	48-pin LQFP	Pb-free package

9. HOW TO READ THE TOP MARKING



1st Line: Winbond Logo

2nd Line: Part_No W83304D, W83304G (Pb-free package)

3rd Line: lot no

4th Line: tracking code 310GBRA

310 : date code, 310 means package was made in '03 week 10

G : Assembly ID, G means GR, A means ASE...etc.

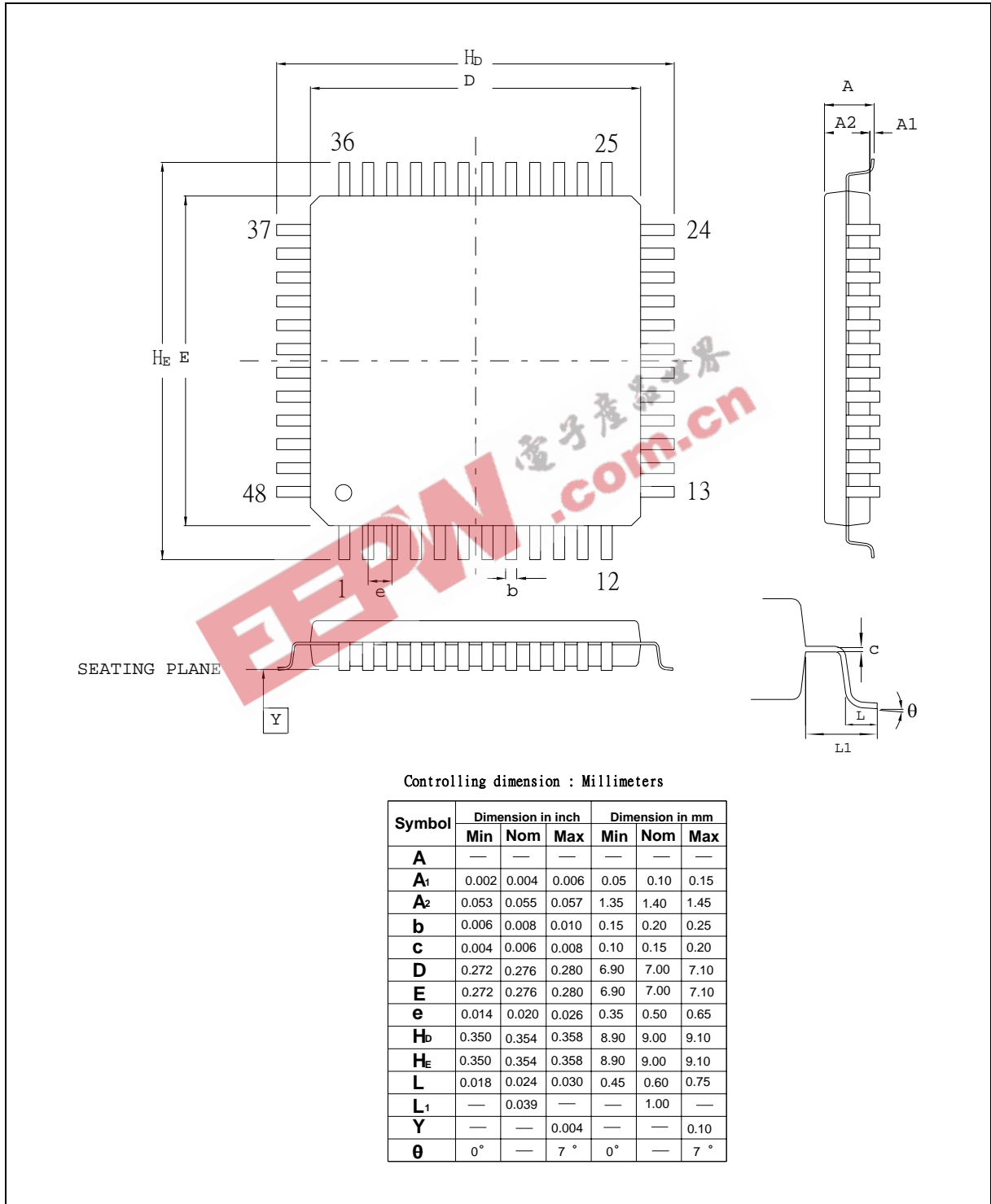
B : Chip Version, A means version A, B means version B

RA : Winbond internal use

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10. PACKAGE DIMENSION



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