CompactFlash™ Card

FEATURES

- Fully compatible with PC Card Standard & CFA(Compact Flash Association) Standard.
- Support 3 variations of mode access
  - I/O Card Mode
  - Memory Card Mode
  - True- IDE Mode
- +5.5V / +3.0V single power supply.
- Internal Error Correction Logic
  - Data Interleave to 2 for each 256 Bytes.
  - Error Correction of 1 Byte random error per 128 Bytes of data.
  - Automatic on-the-fly, in-buffer error correction.
- Compatible with all PC Card Service and Socket Service.
- Integrated PC Card attribute memory of 256 Bytes(CIS).
- 4 PC Card function register support.
- Support Host-side Write Protect.
- Automatic wake up from power-down on host reset or command write.
- Sector data transfers without microprocessor intervention.
- Operation Environment
  - Temperature — 0°C ~ 65°C
  - Humidity — 8% ~ 95%

DESCRIPTION

The WEDC CompactFlash™ Card consists of a CompactFlash™ Controller, which supports Toshiba/ Samsung NAND type flash. The CompactFlash™ Card meets CFA specification V1.4, and provides error correcting code (ECC) reliability to detect and correct errors automatically.

* This product is subject to change without notice.

Notes: CompactFlash™ is a trademark of SanDisk Corporation and is licensed royalty-free to the CFA, which in turn will license it royalty-free to CFA members.
CFA: CompactFlash™ Association.

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PRODUCT TYPES

Card Density	Model No.
32MB	7P032CFA80xxC25
64MB	7P064CFA80xxC25
128MB	7P128CFA80xxC25
256MB	7P256CFA80xxC25
512MB	7P512CFA80xxC25
1024MB	7P1024CFA80xxC25
2048MB	7P2048CFA80xxC25
4096MB	7P4G0CFA80xxC25

xx = Housing
00 = WEDC logo
01 = No logo

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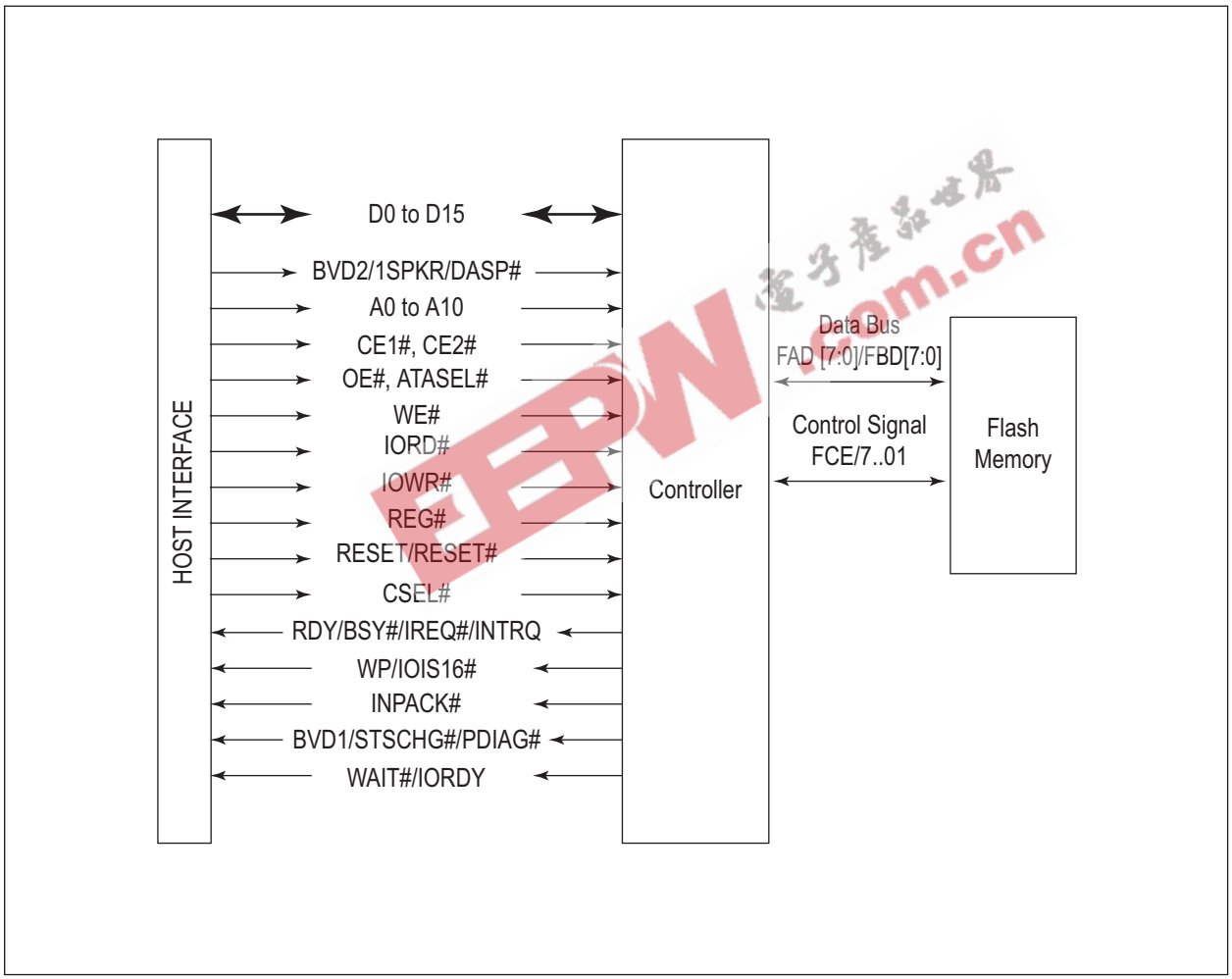
BLOCK DIAGRAM



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PIN ASSIGNMENTS AND PIN TYPE

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode[4]			
Pin Num	Signal Name	Pin Type	In ,Out Type	Pin Num	Signal Name	Pin Type	In ,Out Type	Pin Num	Signal Name	Pin Type	In ,Out Type
1	GND		Ground	1	GND		Ground	1	GND		Ground
2	D03	I/O	I1Z,OZ3	2	D03	I/O	I1Z,OZ3	2	D03	I/O	I1Z,OZ3
3	D04	I/O	I1Z,OZ3	3	D04	I/O	I1Z,OZ3	3	D04	I/O	I1Z,OZ3
4	D05	I/O	I1Z,OZ3	4	D05	I/O	I1Z,OZ3	4	D05	I/O	I1Z,OZ3
5	D06	I/O	I1Z,OZ3	5	D06	I/O	I1Z,OZ3	5	D06	I/O	I1Z,OZ3
6	D07	I/O	I1Z,OZ3	6	D07	I/O	I1Z,OZ3	6	D07	I/O	I1Z,OZ3
7	CE1#	I	I3U	7	CE1#	I	I3U	7	CSO#	I	I3Z
8	A10	I	I1Z	8	A10	I	I1Z	8	A10[2]	I	I1Z
9	OE#	I	I3U	9	OE#	I	I3U	9	ATA# SEL	I	I3U
10	A09	I	I1Z	10	A09	I	I1Z	10	A09[2]	I	I1Z
11	A08	I	I1Z	11	A08	I	I1Z	11	A08[2]	I	I1Z
12	A07	I	I1Z	12	A07	I	I1Z	12	A07[2]	I	I1Z
13	Vcc		Power	13	Vcc		Power	13	Vcc		Power
14	A06	I	I1Z	14	A06	I	I1Z	14	A06[2]	I	I1Z
15	A05	I	I1Z	15	A05	I	I1Z	15	A05[2]	I	I1Z
16	A04	I	I1Z	16	A04	I	I1Z	16	A04[2]	I	I1Z
17	A03	I	I1Z	17	A03	I	I1Z	17	A03[2]	1	I1Z
18	A02	I	I1Z	18	A02	I	I1Z	18	A02	I	I1Z
19	A01	I	I1Z	19	A01	I	I1Z	19	A01	I	I1Z
20	A00	I	I1Z	20	A00	I	I1Z	20	A00	I	I1Z
21	D00	I/O	I1Z, OZ3	21	D00	I/O	I1Z, OZ3	21	D00	I/O	I1Z, OZ3
22	D01	I/O	I1Z, OZ3	22	D01	I/O	I1Z, OZ3	22	D01	I/O	I1Z, OZ3
23	D02	I/O	I1Z, OZ3	23	D02	I/O	I1Z, OZ3	23	D02	I/O	I1Z, OZ3
24	WP	O	OT3	24	IOIS16#	O	OT3	24	IOIS16#	O	ON3
25	CD2#	O	Ground	25	CD2#	O	Ground	25	CD2#	O	Ground
26	CD1#	O	Ground	26	CD1#	O	Ground	26	CD1#	O	Ground
27	D11[1]	I/O	I1Z,OZ3	27	D11[1]	I/O	I1Z,OZ3	27	D11[1]	I/O	I1Z,OZ3
28	D12[1]	I/O	I1Z,OZ3	28	D12[1]	I/O	I1Z,OZ3	28	D12[1]	I/O	I1Z,OZ3
29	D13[1]	I/O	I1Z,OZ3	29	D13[1]	I/O	I1Z,OZ3	29	D13[1]	I/O	I1Z,OZ3
30	D14[1]	I/O	I1Z,OZ3	30	D14[1]	I/O	I1Z,OZ3	30	D14[1]	I/O	I1Z,OZ3
31	D15[1]	I/O	I1Z,OZ3	31	D15[1]	I/O	I1Z,OZ3	31	D15[1]	I/O	I1Z,OZ3
32	CE2[1]#	I	I3U	32	CE21#	I	I3U	32	CS1[1]#	I	I1Z
33	VS[1]#	O	Ground	33	VS[1]#	O	Ground	33	VS[1]#	O	Ground
34	IORD#	I	I3U	34	IORD#	I	I3U	34	IORD#	I	I3Z
35	IOWR#	I	I3U	35	IOWR#	I	I3U	35	IOWR#	I	I3Z
36	WE#	I	I3U	36	WE#	I	I3U	36	WE[3]#	I	I3U
37	RDY/BSY	O	OT1	37	IREQ	O	OT1	37	INTRQ	O	OZ1
38	Vcc		Power	38	Vcc		Power	38	Vcc		Power
39	CSEL#	I	I2Z	39	CSEL#	I	I2Z	39	CSEL#	I	I2U
40	VS2#	O	OPEN	40	VS2#	O	OPEN	40	VS2#	O	OPEN
41	RESET	I	I2Z	41	RESET	I	I2Z	41	RESET#	I	I2Z
42	WAIT#	O	OT1	42	WAIT#	O	OT1	42	IORDY	O	ON1
43	INPACK#	O	OT1	43	INPACK#	O	OT1	43	INPACK#	O	OZ1
44	REG#	I	I3U	44	REG#	I	I3U	44	REG[3]#	I	I3U
45	BVD2	I/O	I1U, OT1	45	SPKR#	I/O	I1U, OT1	45	DASP#	I/O	I1U, ON1

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PIN ASSIGNMENTS AND PIN TYPE (cont'd)

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode[4]			
Pin Num	Signal Name	Pin Type	In ,Out Type	Pin Num	Signal Name	Pin Type	In ,Out Type	Pin Num	Signal Name	Pin Type	In ,Out Type
46	BVD1	I/O	I1U, OT1	46	STSCHG#	I/O	I1U, OT1	46	PDIAG#	I/O	I1U, ON1
47	D08[1]	I/O	11Z, OZ3	47	D08[1]	I/O	I1Z, OZ3	47	D08[1]	I/O	I1Z, OZ3
48	D09[1]	I/O	11Z, OZ3	48	D09[1]	I/O	I1Z, OZ3	48	D09[1]	I/O	I1Z, OZ3
49	D10[1]	I/O	11Z, OZ3	49	D10[1]	I/O	11Z, OZ3	49	D10[1]	I/O	I1Z, OZ3
50	GND		Ground	50	GND		Ground	50	GND		Ground

Notes :

1. These signals are required only for 16 bit access and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.
2. Should be grounded by the host.
3. Should be tied to V_{CC} by the host.
4. Optional for CE + Cards, Required for CompactFlash Storage Cards.

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Rating	Units
V_{CC}	Power supply	-0.3 to 6.0	V
V_{IN}	Input voltage	-0.3 to V_{CC}+0.3	V
V_{OUT}	Output voltage	-0.3 to V_{CC}+0.3	V
T_{STG}	Storage temperature	-40 to 125	°C

DC CHARACTERISTICS:

I) Recommended Operating Conditions:

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Power supply	3.0	5.5	V
V_{IN}	Input voltage	0	V_{CC}	V
T_{OPR}	Operating temperature	-20	65	°C

II) General DC Characteristics:

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IL}	Input low current	no pull up/down	-1		1	µA
I_{IH}	Input high current	no pull up/down	-1		1	µA
I_{OZ}	Tri-state leakage current		-10		10	µA
C_{IN}	Input capacitance		4		pF	
C_{OUT}	Output capacitance		4		pF	
C_{BID}	Bi-direction capacitance		4		pF	

III) DC Electrical Characteristics:

Symbol	Parameter	Min	Typ	Max	Units
V_{IL}	Input low voltage			0.3V_{CC}	V
V_{IH}	Input high voltage	0.7V_{CC}			V
V_{IL}	Schmitt input low voltage		1.22		V
V_{IH}	Schmitt input high voltage		2.08		V
V_{OL}	Output low voltage			0.4	V
V_{OH}	Output high voltage	2.3		1	V
R_I	Input pull up/down resistance		75		kΩ

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AC CHARACTERISTICS:

Attribute Memory Read Timing Specification

Attribute Memory access time is defined as 300ns. Detailed timing specs are shown in Table below.

Speed Version			300 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**
Read Cycle Time	tc(R)	t_{AVAV}	300	
Address Access Time	ta(A)	t_{AVQV}		300
Card Enable Access Time	ta(CE)	t_{ELQV}		300
Output Enable Access Time	ta(OE)	t_{GLQV}		150
Output Disable Time from CE	tdis(CE)	t_{EHQZ}		100
Output Disable Time from OE	tdis(OE)	t_{GHQZ}		100
Address Setup Time	tsu(A)	t_{AVGL}	30	
Output Enable Time from CE	ten(CE)	t_{ELQNZ}	5	
Output Enable Time from OE	ten(OE)	t_{GLQNZ}	5	
Data Valid from Address Change	tv(A)	t_{AXQX}	0	

Note: All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system.
The CE# signal or both the OE# signal and the WE# signal must be de-asserted between consecutive cycle operations.

Configuration Register (Attribute Memory) Write Timing Specification

The Card Configuration write access time is defined as 250ns. Detailed timing specifications are shown in Table below.

Speed Version			250 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns**	**Max ns**
Write Cycle Time	tc(W)	t_{AVAV}	250	
Write Pulse Width	tw(WE)	t_{WLWH}	150	
Address Setup Time	tsu(A)	t_{AVWL}	30	
Write Recovery Time	trec(WE)	t_{WMAX}	30	
Data Setup Time for WE	tsu(D-WEH)	t_{DVWH}	80	
Data Hold Time	th(D)	t_{WMDX}	30	

Note: All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card or CF+ Card.

Common Memory Read Timing Specification

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Output Enable Access Time	ta(OE)	t_{GLQV}		125
Output Disable Time from OE	tdis(OE)	t_{GHQZ}		100
Address Setup Time	tsu(A)	t_{AVGL}	30	
Address Hold Time	th(A)	t_{GHAX}	20	
CE Setup before OE	tsu(CE)	t_{ELGL}	0	
CE Hold following OE	th(CE)	t_{GHEH}	20	
Wait Delay Falling from OE	tv(WT-OE)	t_{GLWTV}		35
Data Setup for Wait Release	tv(WT)	t_{QVWTH}		0
Wait Width Time	tw(WT)	t_{WTLWTH}		350 (3000 for CF+)

Note: The maximum load on -WAIT# is 1 LSTTL with 50pF total load. All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. The WAIT# signal may be ignored if the OE# cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12ps but is intentionally less in this specification.

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AC CHARACTERISTICS (cont'd):

I/O Input (Read) Timing Specification

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Delay after IORD	td(IORD)	t_{IGLQV}		100
Data Hold following IORD	th(IORD)	t_{IGHQX}	0	
IORD Width Time	tw(IORD)	t_{IGLIGH}	165	
Address Setup before IORD	tsuA(IORD)	t_{AVIGL}	70	
Address Hold following IORD	thA(IORD)	t_{IGHAX}	20	
CE Setup before IORD	tsuCE(IORD)	t_{ELIGL}	5	
CE Hold following IORD	thCE(IORD)	t_{IGHEH}	20	
REG Setup before IORD	tsuREG(IORD)	t_{RGLIGL}	5	
REG Hold following IORD	thREG(IORD)	t_{IGHRGH}	0	
INPACK Delay Falling from IORD	tdfINPACK(IORD)	t_{IGLIAL}	0	45
INPACK Delay Rising from IORD	tdrINPACK(IORD)	t_{IGHIAH}		45
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	t_{AVISL}		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	t_{AVISH}		35
Wait Delay Falling from IORD	tdWT(IORD)	t_{IGLWTL}		35
Data Delay from Wait Rising	td(WT)	t_{WTHQV}		0
Wait Width Time	tw(WT)	t_{WTLWTH}		350 (3000 for CF+)

Note: Maximum load on WAIT#, INPACK# and I0IS16# is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from WAIT# high to IORD# high is Onsec, but minimum IORD# width must still be met. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. Wait Width time meets PCMCIA specification of 12ps but is intentionally less in this spec.

I/O Output (Write) Timing Specification

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	t_{DVIWH}	60	
Data Hold following IOWR	th(IOWR)	t_{IWHDX}	30	
IOWR Width Time	tw(IOWR)	t_{IWLIWH}	165	
Address Setup before IOWR	tsuA(IOWR)	t_{AVIWL}	70	
Address Hold following IOWR	thA(IOWR)	t_{IWHAX}	20	
CE Setup before IOWR	tsuCE(IOWR)	t_{ELIWL}	5	
CE Hold following IOWR	thCE(IOWR)	t_{IWHEH}	20	
REG Setup before IOWR	tsuREG(IOWR)	t_{RGLIWL}	5	
REG Hold following IOWR	thREG(IOWR)	t_{IWHRGH}	0	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	t_{AVISL}		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	t_{AVISH}		35
Wait Delay Falling from IOWR	tdWT(IOWR)	t_{IWLWTL}		35
IOWR high from Wait high	tdrIOWR(WT)	t_{WTJIWH}	0	
Wait Width Time	tw(WT)	t_{WTLWTH}		350 (3000for CF+)

Note: The maximum load on WAIT#, INPACK#, and I0IS16# is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from WAIT# high to IOWR# high is Onsec, but minimum IOWR# width must still be met. Din signifies data provided by the system to the CompactFlash Storage Card or CF+ Card. The Wait Width time meets the PCMCIA specification of 12ps but is intentionally less in this specification.

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AC CHARACTERISTICS (cont'd):

True IDE Mode I/O Input (Read) Timing Specification

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Delay after IORD	td(IORD)	t_{IGLQV}		100
Data Hold following IORD	th(IORD)	t_{IGHQX}	0	
IORD Width Time	tw(IORD)	t_{IGLIGH}	165	
Address Setup before IORD	tsuA(IORD)	t_{AVIGL}	70	
Address Hold following IORD	thA(IORD)	t_{IGHAX}	20	
CE Setup before IORD	tsuCE(IORD)	t_{ELIGL}	5	
CE Hold following IORD	thCE(IORD)	t_{IGHEH}	20	
I0IS16 Delay Falling from Address	tdfIOIS16(ADR)	t_{AVISL}		35
I0IS16 Delay Rising from Address	tdrIOIS16(ADR)	t_{AVISH}		35

Note: The maximum load on -I0IS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from WAIT# high to IORD# high is 0 nsec, but minimum IORD# width must still be met. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system.

True IDE Mode I/O Output (Write) Timing Specification

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	t_{DVIWH}	60	
Data Hold following IOWR	th(IOWR)	t_{IWHDX}	30	
IOWR Width Time	tw(IOWR)	t_{IWLIWH}	165	
Address Setup before IOWR	tsuA(IOWR)	t_{AVIWL}	70	
Address Hold following IOWR	thA(IOWR)	t_{IWHAX}	20	
CE Setup before IOWR	tsuCE(IOWR)	t_{ELIWL}	5	
CE Hold following IOWR	thCE(IOWR)	t_{IWHEH}	20	
I0IS16 Delay Falling from Address	tdfIOIS16(ADR)	t_{AVISL}		35
I0IS16 Delay Rising from Address	tdrIOIS16(ADR)	t_{AVISH}		35

Note: The maximum load on -I0IS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from WAIT# high to IOWR# high is 0 nsec, but minimum IOWR# width must still be met. Din signifies data provided by the system to the CompactFlash Storage Card or CF+ Card.

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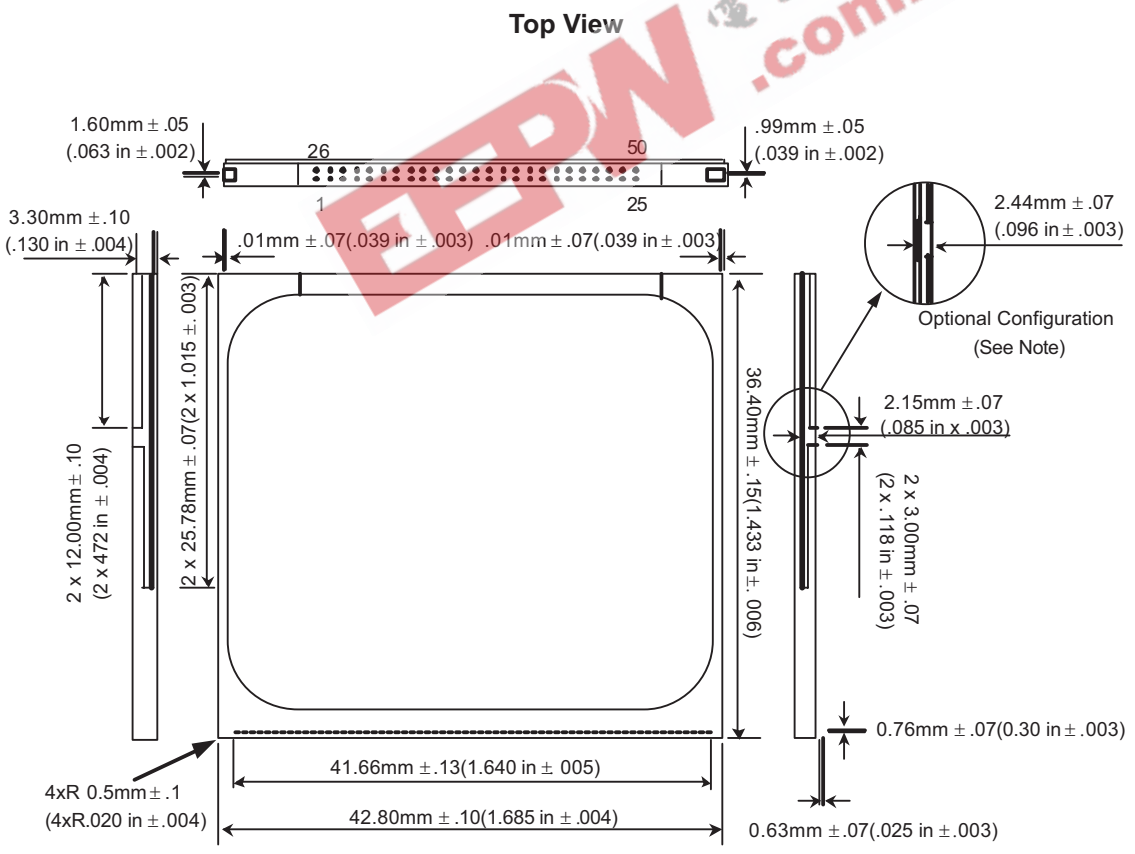
PHYSICAL SPECIFICATIONS

Length:	36.40 ± 0.15mm (1.433 ± .006in.)
Width:	42.80 ± 0.10mm (1.685 ± .004in.)
Thickness (Including Label Area)	3.3mm ± 0.10mm (.130 ± .004in)

PACKAGE DIMENSIONS



Note: The optional notched configuration was shown in the CF Specification Rev. 1.0. In specification Rev. 1.2, the notch was removed for ease of tooling. This optional configuration can be used but it is not recommended.

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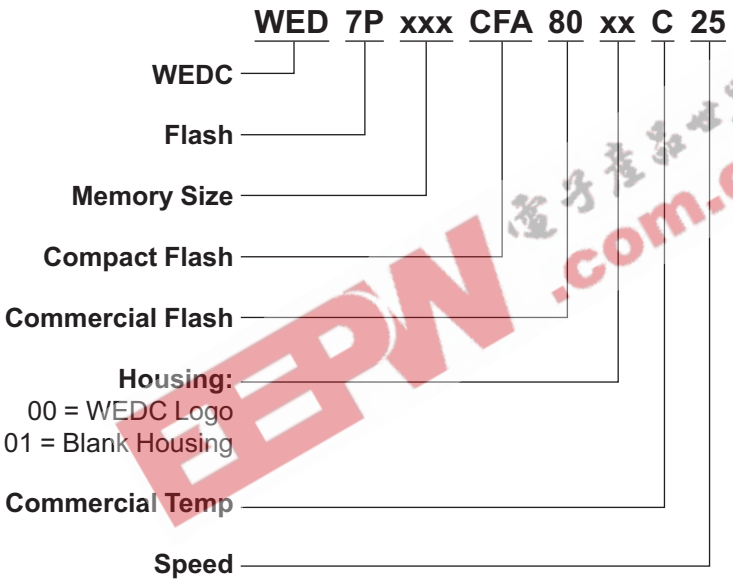
PART NUMBERING GUIDE



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Document Title

CompactFlash™ Card

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	March 2005	Final
Rev 1	1.1 Added "ED" to part marking	July 2005	Final

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