Winbond Electronics Corp.

ADVANCED VL-IDE DISK CONTROLLER

GENERAL DESCRIPTION

The W83759A is an advanced version of Winbond's popular VL-IDE interface chip, the W83759. The W83759A retains all of the features and compatibility of the W83759 (the chip meets the ANSI ATA 4.0 specification for IDE hard disk operation and the VESA VL-Bus 2.0 specification for PC local bus devices) while incorporating new features to meet Enhanced IDE, SFF-8011, ATA-2, and Fast-ATA specifications.

Supports Disk Capacity of Greater than 528 MB

The W83759A's driver can handle remapping from BIOS CHS mode to HDD LBA mode. This scheme enables users to break the 528 MB per drive barrier, allowing full use of BIOS INT13 CHS information in drives with a capacity of up to 8.4 GB.

High Speed Host Transfer Rate

The W83759A supports Enhanced IDE PIO mode 3 and Fast ATA PIO mode 3 and 4 timing; jumper settings or driver programming can be used to select the PIO mode and a 33 or 50 MHz VL-Bus clock. Different programming timing can be selected for different drives in the same system. The burst transfer rate is shown in the following table.

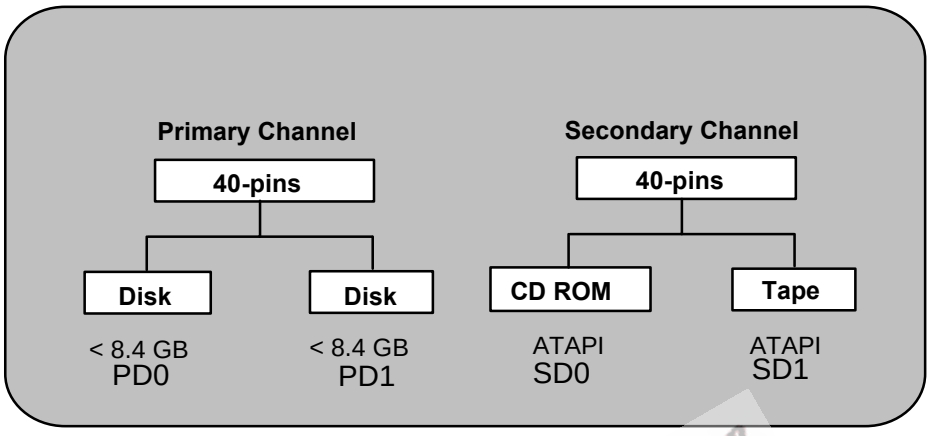
ATA PIO MODE	IDE COMMAND CYCLE TIME (nS)	BURST TRANSFER RATE (MB/sec)	IORDY THROTTLE CONTROL
0	600	3.33	Option
1	383	5.22	Option
2	240	8.33	Option
3	180	11.1	Required
4	120	16.6	Required

Dual IDE Channels

Like the W83759, the W83759A supports a secondary IDE address (170h-177h/376h) and IRQ15 for applications with four hard disk drives. Additionally, the primary and secondary channels can be independently enabled or disabled by jumper settings or software programming.

Non-disk IDE Peripherals

Because the command cycle can be programmed individually for each drive and dual IDE channels are supported, non-disk IDE peripherals (such as an ATAPI CD-ROM or tape drive) can be attached to the secondary IDE without affecting the transfer rate of the ATA disk drive. Sales of ATAPI IDE CD-ROMs are expected to grow rapidly as these devices become a standard part of many users' desktop PC setup.



The W83759A provides all of the next-generation ATA-IDE requirements, including support for high capacity disk drives, high speed host transfers, multiple IDE peripherals, and non-disk IDE peripherals. It makes high-performance, low-cost, easy-to-use IDE machines possible.

The W83759A is pin-to-pin backward compatible with the W83759. In addition to the advanced features described above, the W83759A supports automatic power-down, standby, and suspend APM power management states for green PC applications. This new chip is packaged in a 100-pin QFP.

The table below compares the W83759 and W83759A:

	W83759	W83759A
Dual Channel IDE	Yes	Yes
8.4 G Max. Cap.	Software Driving	Software Driving
PIO Mode 3, 4 Control	No	Yes*
DMA Mode Control	No	Yes*
IOCHRDY Control	No	Yes*
IDE Timing Control	Jumper	Jumper or Driver*
Prefetch Control	No	Yes*
Power Saving Control	No	Yes*
ATAPI Protocol	Software Driving	Software Driving

* All control is drive-by-drive (per drive selectability)

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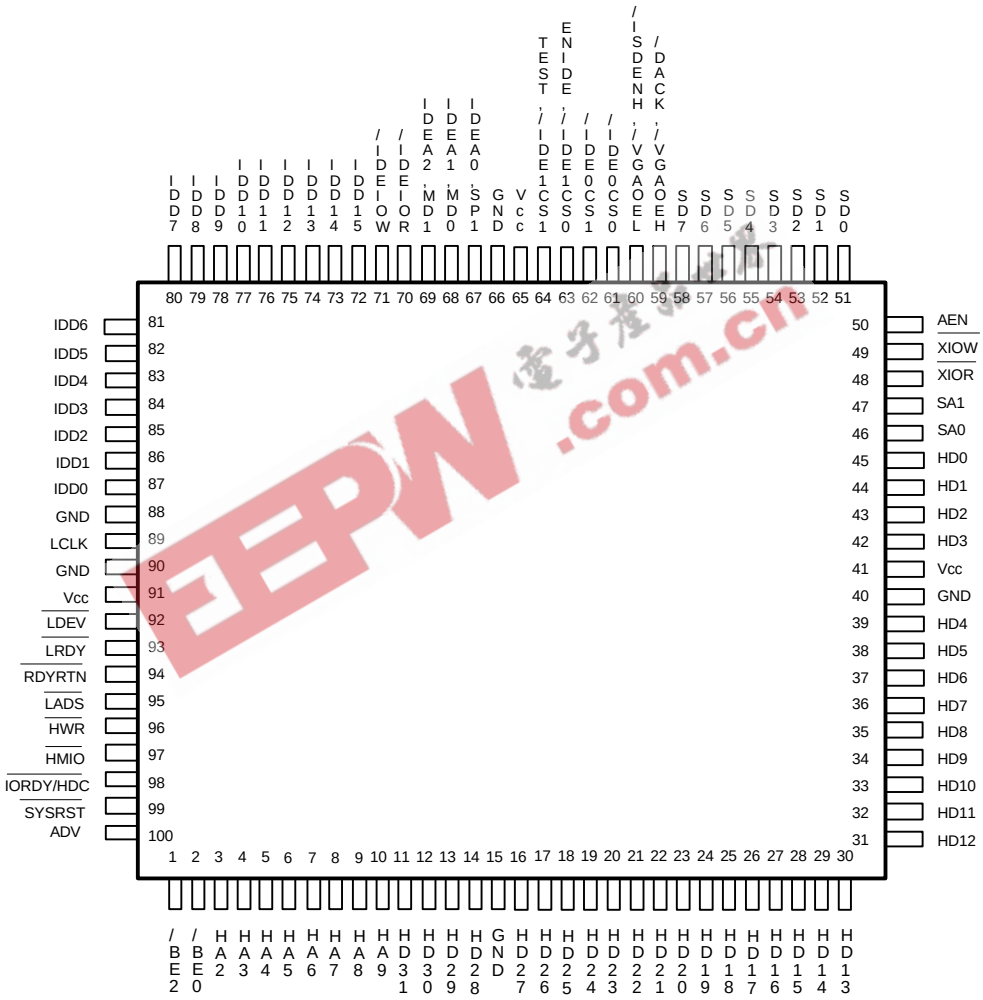
FEATURES

- Pin-to-pin backward compatible with W83759 VL-IDE Interface chip
- VESA VL-Bus Rev 2.0 compatible, connects directly to local bus and four IDE drives
- Direct interface to various ANSI ATA/ATA-2/FAST ATA/IDE-2/Enhanced IDE drives
- Supports 32 and 16-bit data transfer
- Fully software programmable for command active/recovery time and address setup, data hold time
- Built-in VL-Bus to 16-bit IO data buffer for special applications
- Fully supports Enhanced IDE features, including Fast PIO, Mode 3/4, IORDY flow control, prefetch control
- Supports dual channels to allow up to four drives or non-disk devices (ATAPI CD-ROM and tape drives)
- Pipeline pre-fetched reads and posted writes for concurrent disk and host operations
- Independent access timing for all drives (primary/secondary and master/slave)
- All Enhanced IDE new features may be disabled/enabled via driver or power-on setting by per drive selectability
- ATA/Mode 0-4 PIO speed may be set as default timing of each drive via power-on jumper setting
- Supports slave DMA mode protocol (reserved)
- Supports auto power-down, standby, suspend APM power management state for green PCs
- Primary and secondary channel can be independently enabled/disabled by software or jumper setting
- Supports drivers for DOS, Windows, OS/2, UNIX, and Netware
- Packaged in 100-pin QFP

PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PIN	TYPE	DESCRIPTION
VL-Bus Interface			
ADV	100	I-PU	Advanced mode indicator. When high, chip is in W83759A mode. When low, chip is in W83759 mode.
LCLK	89	I	VL-Bus clock.
$\overline{\text{SYSRST}}$	99	I	System reset. When active, the power-on setting pin acts as input.
$\overline{\text{LADS}}$	95	I	Address data strobe. An active low input signal indicates that there is a valid address and command on the bus.
IORDY /$\overline{\text{HDC}}$	98	I	In W83759A mode: Enhanced IDE IORDY flow control input. Used to throttle disk's PIO data transfers to improve PIO mode. In W83759 mode: Host data or code status. Used to distinguish between IO and interrupt or halt cycles.
$\overline{\text{HMIO}}$	97	I-PU	Host memory or I/O status. Used to distinguish between memory and I/O cycles.
$\overline{\text{HWR}}$	96	I	Host write or read status. Used to distinguish between write and read cycles.
$\overline{\text{BE2}}$ $\overline{\text{BE0}}$	1 2	I	Byte enable bits 2 and 0 from the host CPU address bus. These active low inputs specify which bytes will be valid for host read and write data transfers. When $\overline{\text{BE2}}$ is low, the host performs a 32-bit hard disk data transfer cycle when $\overline{\text{LDEV}}$ is active.
$\overline{\text{LDEV}}$	92	O	Local device. An active low output signal which indicates that the current host CPU command cycle is a valid W83759A I/O address (1F0h or 170h).
$\overline{\text{LRDY}}$	93	Tri-O	Local ready. An active low output that indicates when a CPU transfer has been completed. During a cycle $\overline{\text{LRDY}}$ will first be enabled and driven high. When the cycle is completed, $\overline{\text{LRDY}}$ will immediately be pulled low and will remain active for one T-state. Then it will drive high for one T-state before finally being disabled to end the sequence. This signal is shared with all other VL-Bus targets and driven by W83759A only during cycles W83759A has claimed as its own.

Pin Description, continued

SYMBOL	PIN	TYPE	DESCRIPTION
$\overline{\text{RDYRTN}}$	94	I	Ready return. An active low signal that indicates the end of the current host CPU transfer. Usually $\overline{\text{RDYRTN}}$ is tied directly to the $\overline{\text{RDY}}$ signal of the host CPU.
HA[9:2]	10-3	I	Host address bits 9 through 2 from the host address bus.
HD[31:0]	11–14 19–39 42–45	I/O	Host data. This is the 32-bit bidirectional data bus that connects to the host CPU. HD[7:0] define the lowest data byte, while D[31:24] define the most significant byte by the $\overline{\text{BE}}$[2:0] signals. The HD bus is normally in a high-impedance state and is driven by the W83759A only during data register (1F0h or 170h) read cycles and VGA ($\overline{\text{VGAOEH}}$ = 0 or $\overline{\text{VGAOEL}}$ = 0) read cycles.
Drive Interface			
PRDYEN /$\overline{\text{IDE0CS0}}$	61	I/O -PU	When $\overline{\text{SYSRST}}$ is active, this is an input that latches on the rising edge of $\overline{\text{SYSRST}}$. PRDYEN: A high input enables the IORDY flow control function of the primary channel (IDE0) and a low input disables the IDE0's flow control function. $\overline{\text{IDE0CS0}}$: When $\overline{\text{SYSRST}}$ is inactive, this pin is an active low output used to select the command block registers in the IDE0 drive (1F0h–1F7h).
SRDYEN /$\overline{\text{IDE0CS1}}$	62	I/O -PU	When $\overline{\text{SYSRST}}$ is active, this is an input that latches on the rising edge of $\overline{\text{SYSRST}}$. SRDYEN: A high input enables the IORDY flow control function of the secondary channel (IDE1) and a low disables the IDE1's flow control function. $\overline{\text{IDE0CS1}}$: When $\overline{\text{SYSRST}}$ is inactive, this pin is an active low output used to select the alternate status register of the control block registers in the IDE0 drive (3F6).

Pin Description, continued

SYMBOL	PIN	TYPE	DESCRIPTION
ENIDE /IDE1CS0	63	I/O -PU	When SYSRST is active, this is an input that latches on the rising edge of SYSRST . ENIDE: In W83759 mode (ADV = low), this power-on-setting pin controls if the chip enable or disable. In W83759A mode (ADV = high), this pin controls if the IDE0 channel enable or disable. A high input enables and a low input disables the IDE0 channel. IDE1CS0 : When SYSRST is inactive, this pin is an active low output and is used to select the command block registers in the IDE1 drive (170h–177h).
TEST /IDE1CS1	64	I/O -PU	When SYSRST is active, this is an input that latches on the rising edge of SYSRST . TEST: In W83759 mode, this power-on-setting pin controls whether both dual channels are enabled or only the primary channel is enabled. A high input enables IDE0 and IDE1 simultaneously and a low input enables IDE0 only. In W83759A mode, this pin controls whether the IDE1 channel enable or disable controls the IDE0 channel as ENIDE. IDE1CS1: When SYSRST is inactive, this pin is an active low output used to select the alternate status register of the control block registers in the IDE1 drive (376).
EMD1 /IDEIOR	70	I/O -PU	When SYSRST is active, this is an input that latches on the rising edge of SYSRST . EMD1: This power-on-setting pin combines with EMD0 to set the initial enhanced timing mode of hard disk access cycles when the enhanced mode is selected via the POSS3 configuration register. IDEIOR : Drive I/O read. An active low output that enables data to be read from the drive. The duration and repetition rate of IDEIOR cycles are determined by the type of IDE drive, as specified by MD1 and MD0, in W83759 mode or by EMD1 and EMD0 in W83759A enhanced mode.

Pin Description, continued

<table>
<tr><th>SYMBOL</th><th>PIN</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>$\overline{\text{EMD0}}$
/$\overline{\text{IDEIOW}}$</td><td>71</td><td>I/O
-PU</td><td>When $\overline{\text{SYSRST}}$ is active, this is an input that latches on the rising edge of $\overline{\text{SYSRST}}$.
$\overline{\text{EMD0}}$: This power-on-setting pin combines with $\overline{\text{EMD1}}$ to set the initial enhanced timing mode of hard disk access cycles when the enhanced mode is selected via the POSS3 configuration register.
<table>
<tr><th>ATA PIO mode</th><th>Access Time</th><th>$\overline{\text{EMD1}}$</th><th>$\overline{\text{EMD0}}$</th></tr>
<tr><td>2</td><td>240 nS</td><td>1</td><td>1</td></tr>
<tr><td>3</td><td>180 nS</td><td>1</td><td>0</td></tr>
<tr><td>3</td><td>180 nS</td><td>0</td><td>1</td></tr>
<tr><td>4</td><td>120 nS</td><td>0</td><td>0</td></tr>
</table>
$\overline{\text{IDEIOW}}$: Drive I/O write. An active low output that enables data to be written to the drive. The duration and repetition rate of $\overline{\text{IDEIOW}}$ cycles are determined by the type of IDE drive, as specified by $\overline{\text{IDEIOR}}$.</td></tr>
<tr><td>MD1
/IDEA2,
MD0
/IDEA1</td><td>69

68</td><td>I/O
-PD</td><td>When $\overline{\text{SYSRST}}$ is active, these pins function as inputs and latch on the rising edge of $\overline{\text{SYSRST}}$.
MD1, MD0: ATA mode of IDE Drive. MD0 and MD1 are used to select the hard disk access time.
<table>
<tr><th>ATA PIO mode</th><th>Access Time</th><th>$\overline{\text{EMD1}}$</th><th>$\overline{\text{EMD0}}$</th></tr>
<tr><td>0</td><td>600 nS</td><td>0</td><td>0</td></tr>
<tr><td>0+</td><td>500 nS</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>400 nS</td><td>1</td><td>0</td></tr>
<tr><td>2</td><td>240 nS</td><td>1</td><td>1</td></tr>
</table>
IDEA2, IDEA1: IDE drive address bits 2 and 1. Drive address bits 2 and 1 are outputs to the IDE connector for register selection in the drive.</td></tr>
</table>

Pin Description, continued

SYMBOL	PIN	TYPE	DESCRIPTION
SP1 /IDEA0	67	I/O -PD	When $\overline{\text{SYSRST}}$ is active, this pin is an input that latches on the rising edge of $\overline{\text{SYSRST}}$. SP1: VL-Bus speed select. A high input configures the W83759A to run at from 33 MHz to 50 MHz; a low input configures the W83759A to run at under 33 MHz. IDEA0: IDE drive address bit 0. Drive address bit 0 is output to the IDE connector for register selection in the drive.
IDD[15:0]	72–87	I/O -PU	When $\overline{\text{SYSRST}}$ is active, these pins function as inputs and latch on the rising edge of $\overline{\text{SYSRST}}$. As power-on setting pins, IDD[15:8] are latched to the POSS3 register and IDD[7:0] are latched to the POSS2 register. As the drive data bus, bits 15 through 0 are the 16-bit bidirectional data bus that connects to the IDE drive. IDD[7:0] define the lowest data byte. The IDD bus is normally in a pull-high state and is driven with valid data by the W83759A only during IDE or VGA ($\overline{\text{VGAOEH}}$ = 0 or $\overline{\text{VGAOEL}}$ = 0) write cycles.
ISA-Bus Interface			
SA[1:0]	47, 46	I	ISA address bits 1 and 0. Used to select the hard disk I/O registers.
SD[7:0]	58-51	I/O	These signals provide data bus bits 0 through 7 for the CPU and IDE I/O devices. SD0 is the least significant bit and SD7 is the most significant bit.
$\overline{\text{XIOR}}$	48	I	$\overline{\text{XIOR}}$ instructs the hard disk I/O device to drive its data onto the SD data bus.
$\overline{\text{XIOW}}$	49	I	$\overline{\text{XIOW}}$ instructs the hard disk I/O device to read the data on the SD data bus.
AEN	50	I	When this line is active (high), the DMA controller has control of the address bus. A low is the address enable.

Pin Description, continued

<table>
<tr><th>SYMBOL</th><th>PIN</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td colspan="4">Special Bus Control Interface</td></tr>
<tr><td>SUSP,
DACK,
VGAOEH</td><td>59</td><td>I-PU</td><td>This pin is a multi-function input pin.

SUSP: In suspend enable mode, indicates that the W83759A will enter the suspend state when low and resume operation when high.

DACK: In DMA transfer enable mode, used to indicate when the DMA transfer cycle occurs.

VGAOEH: In VGA buffer enable mode, this active low input controls the input enable for the data transceivers that connect the ID[15:0] pins to the HD[31:16] pins.</td></tr>
<tr><td>DMASL,
VGAOEL
/ISDENH</td><td>60</td><td>I/O
-PU</td><td>When SYSRST is active, this pin is an input that latches on the rising edge of SYSRST.

DMASL: This power-on setting pin combines with SUSPEN (IDD11 power-on setting pin) to determine which mode the W83759A is in.
<table>
<tr><th>DMASL</th><th>SUSPEN</th><th>Mode</th></tr>
<tr><td>1</td><td>X</td><td>VGA buffer enable</td></tr>
<tr><td>0</td><td>1</td><td>Suspend enable</td></tr>
<tr><td>0</td><td>0</td><td>DMA transfer enable</td></tr>
</table>
VGAOEL: In VGA buffer enable mode, this active low input controls the input enable for the data transceivers that connect the ID[15:0] pins to the HD[15:0] pins.

ISDENH: In DMA transfer enable mode, this output pin controls the activity of the high byte buffer between IDD[15:8] and SD[15:8].</td></tr>
<tr><td>Vcc</td><td>41, 65, 91</td><td></td><td>+5V power supply</td></tr>
<tr><td>GND</td><td>15, 40, 66, 88, 90</td><td></td><td>Ground reference</td></tr>
</table>

CONFIGURATION REGISTERS

Several configuration registers are implemented in the W83759A. These registers are accessible in single-chip mode through the index/data port. The index/data port address is 1B4h/1B8h or 134h/138h, depending on whether pin IDD0 is high or low at power-on.

When the W83759A is in multi-chip mode (IDD1 is low at power-on setting), an ID code should be written to 1B0h/130h (IDIN port). The W83759A will then enter the programming sequence if the ID code matches the chip ID (determined by IDD2, IDD3 at power-on setting) or leave the programming sequence if the ID code does not match. After the chip has entered the programming sequence, the chip ID can be read by reading 1BCh/13Ch (IDOUT port).

	IDD0_P is HIGH	IDD0_P is LOW
IDIN port (W/O)	1B0h*	130h**
Index port (R/W)	1B4h	134h
data port (R/W)	1B8h	138h
IDOUT port (R/O)	1BCh	13Ch

* The alias base addresses of 1B0h are XB0h and YB0h, where "X" means 0, 4, 8, C and "Y" means 1, 5, 9, D.

** The alias base addresses of 130h are X30h and Y30h, where "X" means 0, 4, 8, C and "Y" means 1, 5, 9, D.

Index map of configuration registers:

INDEX	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
80h(R/O) POSS1	ADV	SP1	MD1	MD0	PRDYEN	SRDYEN	IDEN1	IDEN0	8Fh
81h(R/W) POSP1	ADV_P	SP1_P	MD1_P	MD0_P	PRDYEN_P	SRDYEN_P	IDEN1_P	IDEN0_P	8Fh
82h(R/O) POSS2	PD0LEN	PD1LEN	SD0LEN	SD1LEN	DSL1	DSL0	CRLK#	CRSL	FFh
83h(R/W) POSP2	PD0LE_P	PD1LEN_P	SD0LEN_P	SD1LEN_P	DSL1_P	DSL0_P	CRLK#_P	CRSL_P	FFh
84h(R/O) POSS3	PD0EM#	PD1EM#	SD0EM#	SD1EM#	SUSPEN	STBY#	APD	SWAP#	FFh
85h(R/W) POSP3	PD0EM#_P	PD1EM#_P	SD0EM#_P	SD1EM#_P	SUSPEN_P	STBY#_P	APD_P	SWAP#_P	FFh
86h(R/W) ALTCTL	DMASL#_P	Reserved	EMD1	EMD0	PEMD1_P	PEMD0_P	SEMD1_P	SEMD0_P	80h
87h(R/O) REVID	DMASL#	Reserved	PDRV	SDRV	Rev 3	Rev 2	Rev 1	Rev 0	8Ah
88h(R/W) PD0TIM0	PD0ACT3	PD0ACT2	PD0ACT1	PD0ACT0	PD0RCV3	PD0RCV2	PD0RCV1	PD0RCV0	00h
89h(R/W) PD0TIM1	PD0AST1	PD0AST0	PD0DHT1	PD0DHT0	PD0PRE#	PD0DMA#	PD0RDY#	PD0ADV	00h
8Ah(R/W) PD1TIM0	PD1ACT3	PD1ACT2	PD1ACT1	PD1ACT0	PD1RCV3	PD1RCV2	PD1RCV1	PD1RCV0	00h
8Bh(R/W) PD1TIM1	PD1AST1	PD1AST0	PD1DHT1	PD1DHT0	PD1PRE#	PD1DMA#	PD1RDY#	PD1ADV	00h
8Ch(R/W) SD0TIM0	SD0ACT3	SD0ACT2	SD0ACT1	SD0ACT0	SD0RCV3	SD0RCV2	SD0RCV1	SD0RCV0	00h
8Dh(R/W) SD0TIM1	SD0AST1	SD0AST0	SD0DHT1	SD0DHT0	SD0PRE#	SD0DMA#	SD0RDY#	SD0ADV	00h
8Eh(R/W) SD1TIM0	SD1ACT3	SD1ACT2	SD1ACT1	SD1ACT0	SD1RCV3	SD1RCV2	SD1RCV1	SD1RCV0	00h
8Fh(R/W) SD1TIM1	SD1AST1	SD1AST0	SD1DHT1	SD1DHT0	SD1PRE#	SD1DMA#	SD1RDY#	SD1ADV	00h

CRX80h (POSS1) Read Only Power-on Setting Status 1

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADV	SP1	MD1	MD0	PRDYEN	SRDYEN	IDEN1	IDEN0

Bit 7 ADV

Power-on setting value of ADV pin
Initial application mode

0 No advanced mode application
1 Advanced mode application

Bit 6 SP1

Power-on setting value of IDEA0 pin
Select VESA bus operating CLK

0 VLCLK 33 MHz
1 VLCLK > 33 MHz

Bit 5, 4 MD1, MD0

Power-on setting value of IDEA2, IDEA1 pin
Default HDD host transfer mode

MD1	MD0	
0	0	Mode 0 (cycle time = 600 nS)
0	1	Mode 0+ (cycle time = 500 nS)
1	0	Mode 1 (cycle time = 400 nS)
1	1	Mode 2 (cycle time = 240 nS)

Bit 3 PRDYEN

Power-on setting value of IDE0CS0 pin
Initial state of primary channel IOCHRDY flow control

0 Disable IOCHRDY flow control
1 Enable IOCHRDY flow control

Bit 2 SRDYEN

Power-on setting value of IDE0CS1 pin
Initial state of secondary channel IOCHRDY flow control

0 Disable IOCHRDY flow control
1 Enable IOCHRDY flow control

Bit 1, 0 IDEN1, IDEN0

Power-on setting value of IDE1CS1, IDE1CS0 pins
Initial state of IDE ENable control

when ADV_P = 0

IDEN1	IDEN0	Primary IDE	Secondary IDE
X	0	disabled	disabled
0	1	enabled	disabled
1	1	enabled	enabled

Continued

when ADV_P = 1	IDEN1	IDEN0	Primary IDE	Secondary IDE
	0	0	disabled	disabled
	1	0	disabled	enabled
	0	1	enabled	disabled
	1	1	enabled	enabled

CRX81h (POSP1) Read / Write Power-on Setting Programming 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADV_P	SP1_P	MD1_P	MD0_P	PRDYEN_P	SRDYEN_P	IDEN1_P	IDEN0_P

After power-on, the content of the POSP1 register is equal to that of the POSS1 register. The host can program POSP1 to modify the power-on settings.

Bit 7 ADV_P Programming application mode
- 0 No advanced mode application
- 1 Advanced mode application

Bit 6 SP1_P Select VESA bus operating CLK
- 0 VLCLK 33 MHz
- 1 VLCLK > 33 MHz

Bit 5, 4 MD1_P, MD0_P Select default HDD host transfer mode

MD1_P	MD0_P	
0	0	Mode 0 (cycle time = 600 nS)
0	1	Mode 0+ (cycle time = 500 nS)
1	0	Mode 1 (cycle time = 400 nS)
1	1	Mode 2 (cycle time = 240 nS)

Bit 3 PRDYEN_P Primary channel IOCHRDY flow control
- 0 Disable IOCHRDY flow control
- 1 Enable IOCHRDY flow control

Bit 2 SRDYEN_P Secondary channel IOCHRDY flow control
- 0 Disable IOCHRDY flow control
- 1 Enable IOCHRDY flow control

Bit 1, 0 IDEN1_P, IDEN0_P IDE ENable control

Continued

when ADV_P = 0	IDEN1_P	IDEN0_P	Primary IDE	Secondary IDE
	X	0	disabled	disabled
	0	1	enabled	disabled
	1	1	enabled	enabled

when ADV_P = 1	IDEN1_P	IDEN0_P	Primary IDE	Secondary IDE
	0	0	disabled	disabled
	1	0	disabled	enabled
	0	1	enabled	disabled
	1	1	enabled	enabled

CRX82h (POSS2) Read Only Power-on Setting Status 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD0LEN	PD1LEN	SD0LEN	SD1LEN	DSL1	DSL0	$\overline{\text{CRLK}}$	CRSL

Bit 7 PD0LEN Power-on setting value of IDD7 pin
Initial Primary Drive 0 (PD0) local device control
0 Disable local device
1 Enable local device

Bit 6 PD1LEN Power-on setting value of IDD6 pin
Initial Primary Drive 1 (PD1) local device control
0 Disable local device
1 Enable local device

Bit 5 SD0LEN Power-on setting value of IDD5 pin
Initial Secondary Drive 0 (SD0) local device control
0 Disable local device
1 Enable local device

Bit 4 SD1LEN Power-on setting value of IDD4 pin
Initial Secondary Drive 1 (SD1) local device control
0 Disable local device
1 Enable local device

Continued

Bit 3, 2	DSL1, 0	Power-on setting value of IDD3, IDD2 pin Initial Device ID selection (used in multi-chip mode or CR protection scheme)

DSL1	DSL0	Device ID
0	0	60h
0	1	61h
1	0	62h
1	1	63h

Bit 1	$\overline{\text{CRLK}}$	Power-on setting value of IDD1 pin Initial Configuration Register locked control

0 CR is auto-locked (used in multi-chip mode)

1 CR is not auto-locked (used in single-chip mode)

Bit 0	CRSL	Power-on setting value of IDD0 pin Initial Configuration Register selection

0 CR port address: 130h, 134h, 138h, 13Ch

1 CR portaddress: 1B0h, 1B4h, 1B8h, 1BCh

CRX83h (POSP2) Read / Write Power-on Setting Programming 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD0LEN_P	PD1LEN_P	SD0LEN_P	SD1LEN_P	DSL1_P	DSL0_P	$\overline{\text{CRLK}}$ _P	CRSL_P

After power-on, the content of the POSP2 register is equal to that of the POSS2 register. The host can program POSP2 to modify the power-on settings.

Bit 7	PD0LEN_P	Primary Drive 0 (PD0) local device control

0 Disable local device

1 Enable local device

Bit 6	PD1LEN_P	Primary Drive 1 (PD1) local device control

0 Disable local device

1 Enable local device

Bit 5	SD0LEN_P	Secondary Drive 0 (SD0) local device control

0 Disable local device

1 Enable local device

Continued

Bit 4	SD1LEN_P	Secondary Drive 1(SD1) local device control 0 Disable local device 1 Enable local device
Bit 3, 2	DSL1, 0_P	Device ID selection (used in multi-chip mode or CR protection scheme) DSL1_P DSL0_P Device ID 0 0 60h 0 1 61h 1 0 62h 1 1 63h
Bit 1	$\overline{\text{CRLK}}$ _P	Configuration Register locked control 0 CR is auto-locked (multi-chip mode) 1 CR is not auto-locked (single-chip mode)
Bit 0	CRSL_P	Configuration Register selection 0 CR port address: 130h, 134h, 138h, 13Ch 1 CR port address: 1B0h, 1B4h, 1B8h, 1BCh

CRX84h (POSS3) Read Only Power-on Setting Status 3

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{\text{PD0EM}}$	$\overline{\text{PD1EM}}$	$\overline{\text{SD0EM}}$	$\overline{\text{SD1EM}}$	SUSPEN	STBY#	APD	$\overline{\text{SWAP}}$

Bit 7	$\overline{\text{PD0EM}}$	Power-on setting value of IDD15 pin Initial setting of PD0 enhanced timing enable 0 Enhanced timing 1 Programmable timing
Bit 6	$\overline{\text{PD1EM}}$	Power-on setting value of IDD14 pin Initial setting of PD1 enhanced timing enable 0 Enhanced timing 1 Programmable timing
Bit 5	$\overline{\text{SD0EM}}$	Power-on setting value of IDD13 pin Initial setting of SD0 enhanced timing enable 0 Enhanced timing 1 Programmable timing

Continued

Bit 4	$\overline{\text{SD1EM}}$	Power-on setting value of IDD12 pin Initial setting of SD1 enhanced timing enable 0 Enhanced timing 1 Programmable timing
Bit 3	SUSPEN	Power-on setting value of IDD11 pin Initial setting of SUSPend function 0 Support DMA mode if $\overline{\text{DMASL}}$ _P = 0 and ADV_P = 1 1 Support suspend function if $\overline{\text{DMASL}}$ _P = 0 and ADV_P = 1.
Bit 2	$\overline{\text{STBY}}$	Power-on setting value of IDD10 pin Initial setting of STandBy state 0 W83759A is in standby state 1 W83759A is in normal state
Bit 1	APD	Power-on setting value of IDD9 pin Initial setting of auto Power-down 0 Auto power-down off 1 Auto power-down on
Bit 0	$\overline{\text{SWAP}}$	Power-on setting value of IDD8 pin Initial primary, secondary channel connection select 0 Primary channel connect to IDE1 Secondary channel connect to IDE0 1 Primary channel connect to IDE0 Secondary channel connect to IDE1

CRX85h (POSP3) Read/ Write Power-on Setting Programming 3

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{\text{PD0EM}}$ _P	$\overline{\text{PD1EM}}$ _P	$\overline{\text{SD0EM}}$ _P	$\overline{\text{SD1EM}}$ _P	SUSPEN_P	$\overline{\text{STBY}}$ _P	APD_P	$\overline{\text{SWAP}}$ _P

Bit 7	$\overline{\text{PD0EM}}$ _P	Power-on setting programming of IDD15 pin Programmable setting of PD0 enhanced timing enable 0 Enhanced timing 1 Programmable timing

Continued

Bit 6	$\overline{\text{PD1EM}}$_P	Power-on setting programming of IDD14 pin Programmable setting of PD1 enhanced timing enable 0 Enhanced timing 1 Programmable timing
Bit 5	$\overline{\text{SD0EM}}$_P	Power-on setting programming of IDD13 pin Programmable setting of SD0 enhanced timing enable 0 Enhanced timing 1 Programmable timing
Bit 4	$\overline{\text{SD1EM}}$_P	Power-on setting programming of IDD12 pin Programmable setting of SD1 enhanced timing enable 0 Enhanced timing 1 Programmable timing
Bit 3	SUSPEN_P	Power-on setting value of IDD11 pin Programmable setting of SUSPend function 0 Support suspend function if $\overline{\text{DMASL}}$_P = 0 and ADV_P = 1 1 Support DMA transfer if $\overline{\text{DMASL}}$_P = 0 and ADV_P = 1
Bit 2	$\overline{\text{STBY}}$_P	Power-on setting value of IDD10 pin Programmable setting of STandBy state 0 W83759A is in standby state 1 W83759A is in normal state
Bit 1	APD_P	Power-on setting value of IDD9 pin Initial setting of auto power-down 0 Auto power-down off 1 Auto power-down on
Bit 0	$\overline{\text{SWAP}}$_P	Power-on setting programming of IDD8 pin Programmable primary, secondary channel connection select 0 Primary channel connect to IDE1 Secondary channel connect to IDE0 1 Primary channel connect to IDE0 Secondary channel connect to IDE1

Continued

CRX86h (ALTCTL) Read / Write Alternative Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{\text{DMASL}}$ _P	Reserved	EMD1	EMD0	PEMD1_P	PEMD0_P	SEMD1_P	SEMD0_P

Bit 7 $\overline{\text{DMASL}}$ _P

Power-on setting value of $\overline{\text{VGAOEL}}$ pin.
After power-on, this bit can be programmed to modify the DMA disable/enable power-on setting.

0 DMA mode enabled if SUSPEN_P = 0 and ADV_P = 1

1 DMA mode disabled

Bit 6 Reserved

0 (default)

Bit5–4 EMD1, 0 (Read Only)

Inverse of power-on setting value of $\overline{\text{IDEIOR}}$, $\overline{\text{IDEIOW}}$ pin
Initial setting of enhanced timing of IDE0 and IDE1

EMD1	EMD0	ATA PIO Mode	Cycle time (nS)
0	0	2	240
0	1	3	80
1	0	3	80
1	1	4	120

Bit3–2 PEMD1, 0_P

Initial setting of primary drive enhanced timing
After power-on, these bits can be programmed to modify the primary drive enhanced timing.

PEMD1_P	PEMD0_P	ATA PIO mode	Cycle time (nS)
0	0	2	240
0	1	3	180
1	0	3	180
1	`1	4	120

Bit1–0 SEMD1, 0_P

Initial setting of secondary drive enhanced timing
After power-on, these bits can be programmed to modify the secondary drive enhanced timing

SEMD1_P	SEMD0_P	ATA PIO Mode	Cycle time (nS)
0	0	2	240
0	1	3	180
1	0	3	180
1	1	4	120

CRX87h (REVID) Read Only Revision ID Number

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{\text{DMASL}}$	Reserved	PDRV	SDRV	Rev 3	Rev 2	Rev 1	Rev 0

Bit 7 $\overline{\text{DMASL}}$ Power-on setting value of $\overline{\text{VGAOEL}}$ pin.
Initial DMA enable/disable setting

0 DMA mode enabled if SUSPEN_P = 0 and ADV_P = 1

1 DMA mode disabled

Bit 6 Reserved (Read/Write) 0 (default)

Bit 5 PDRV Primary channel current drive select

0 Master drive (default)

1 Slave drive

Bit 4 SDRV Secondary channel current drive select

0 Master drive (default)

1 Slave drive

Bit 3-Bit 0 Rev 3–Rev 0 1010b (default in A version)

CRX88h (PD0TIM0) Read/Write Primary Drive0 Timing Control 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD0ACT3	PD0ACT2	PD0ACT1	PD0ACT0	PD0RCV3	PD0RCV2	PD0RCV1	PD0RCV0

Bit 7–Bit 4 PD0ACT3–0 PD0 Data Register Port (1F0h) Read/Write Active Time

	Read/Write active time (clocks)
0000	17/16
0001	3/2
0010	3/2
0011	4/3
0100	5/4
0101	6/5
0110	7/6
0111	8/7
1000	9/8
1001	10/9
1010	11/10
1011	12/11
1100	13/12
1101	14/13
1110	15/14
1111	16/15

Bit 3–Bit 0 PD0RCV3–0 PD0 Data Register Port (1F0h) Read/Write Recovery Time

	Write/Read recovery time (clocks)
0000	16/15
0001	2/1
0010	2/1
0011	3/2
0100	4/3
0101	5/4
0110	6/5
0111	7/6
1000	8/7
1001	9/8
1010	10/9
1011	11/10
1100	12/11
1101	13/12
1110	14/13
1111	15/14

CRX89h (PD0TIM1) Read/Write Primary Drive0 Timing Control 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD0AST1	PD0AST0	PD0DHT1	PD0DHT0	$\overline{\text{PD0PRE}}$	$\overline{\text{PD0DMA}}$	$\overline{\text{PD0RDY}}$	PD0ADV

Bit 7–Bit 6 PD0AST1–0 PD0 Data Register Port (1F0h) Address Setup Time

	Read/Write extra address setup time (clocks)
00	0
01	2
10	2
11	3

Bit 5–Bit 4 PD0DHT1–0 PD0 Data Register Port (1F0h) Data Hold Time

	Read/Write extra data hold time (clocks)
00	0
01	2
10	2
11	3

Bit 3 $\overline{\text{PD0PRE}}$ Prefetch/Post write control

0 Prefetch/Post write enabled

1 Prefetch/Post write disabled

Bit 2 $\overline{\text{PD0DMA}}$ PD0 DMA mode control

0 DMA mode enabled

1 DMA mode disabled

Bit 1 $\overline{\text{PD0RDY}}$ PD0 Data Register Port (1F0h) IOCHRDY Control

0 IOCHRDY enabled

1 IOCHRDY disabled

Bit 0 PD0ADV PD0 Data Register Port (1F0h) Advanced Timing Enable

0 Normal timing (depends on SP1, MD1, MD0 setting)

1 Advanced timing (depends on PD0TIM1–0 setting)

CRX8Ah (PD1TIM0) Read/Write Primary Drive1 Timing Control 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD1ACT3	PD1ACT2	PD1ACT1	PD1ACT0	PD1RCV3	PD1RCV2	PD1RCV1	PD1RCV0

Bit 7–Bit 4 PD1ACT3–0 PD1 Data Register Port (1F0h) Read/Write Active Time
Definition of these bits same as PD0ACT3–0

Bit 3–Bit 0 PD1RCV3–0 PD1 Data Register Port (1F0h) Read/Write Recovery Time
Definition of these bits same as PD0RCV3–0

CRX8Bh (PD1TIM1) Read/Write Primary Drive 1 Timing Control 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD1AST1	PD1AST0	PD1DHT1	PD1DHT0	$\overline{\text{PD1PRE}}$	$\overline{\text{PD1DMA}}$	$\overline{\text{PD1RDY}}$	PD1ADV

Bit 7-Bit 6 PD1AST1–0 PD1 Data Register Port (1F0h) Address Setup Time
Definition of these bits same as PD0AST1-0

Bit 5-Bit 4 PD1DHT1–0 PD1 Data Register Port (1F0h) Data Hold Time
Definition of these bits same as PD0DHT1–0

Bit 3 $\overline{\text{PD1PRE}}$ PD1 Prefetch/Post write control
0 Prefetch/Post write enabled
1 Prefetch/Post write disabled

Bit 2 $\overline{\text{PD1DMA}}$ PD1 DMA mode control
0 DMA mode enabled
1 DMA mode disabled

Bit 1 $\overline{\text{PD1RDY}}$ PD1 Data Register Port (1F0h) IOCHRDY Control
0 OCHRDY enabled
1 IOCHRDY disabled

Bit 0 PD1ADV PD1 Data Register Port (1F0h) Advanced Timing Enable
0 Normal timing (depends on SP1, MD1, MD0 setting)
1 Advanced timing (depends on PD1TIM1–0 setting)

CRX8Ch (SD0TIM0) Read/Write Secondary Drive 0 Timing Control 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SD0ACT3	SD0ACT2	SD0ACT1	SD0ACT0	SD0RCV3	SD0RCV2	SD0RCV1	SD0RCV0

Bit 7-Bit 4 SD0ACT3–0 SD0 Data Register Port (170h) Read/Write Active Time
Definition of these bits same as PD0ACT3–0

Bit 3-Bit 0 SD0RCV3–0 SD0 Data Register Port (170h) Read/Write Recovery Time
Definition of these bits same as PD0RCV3–0

CRX8Dh (SD0TIM1) Read/Write Secondary Drive 0 Timing Control 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SD0AST1	SD0AST0	SD0DHT1	SD0DHT0	$\overline{\text{SD0PRE}}$	$\overline{\text{SD0DMA}}$	$\overline{\text{SD0RDY}}$	SD0ADV

Bit 7-Bit 6 SD0AST1–0 SD0 Data Register Port (170h) Address Setup Time
Definition of these bits same as PD0AST1–0

Bit 5-Bit 4 SD0DHT1–0 SD0 Data Register Port (170h) Data Hold Time
Definition of these bits same as PD0RDHT1–0

Bit 3 $\overline{\text{SD0PRE}}$ SD0 Prefetch/Post write control
0 Prefetch/Post write enabled
1 Prefetch/Post write disabled

Bit 2 $\overline{\text{SD0DMA}}$ SD0 DMA mode control
0 DMA mode enabled
1 DMA mode disabled

Bit 1 $\overline{\text{SD0RDY}}$ SD0 Data Register Port (170h) IOCHRDY Control
0 IOCHRDY enabled
1 IOCHRDY disabled

Bit 0 SD0ADV SD0 Data Register Port (170h) Advanced Timing Enable
0 Normal timing (depends on SP1, MD1, MD0 setting)
1 Advanced timing (depends on SD0TIM1–0 setting)

CRX8Eh (SD1TIM0) Read/Write Secondary Drive 1 Timing Control 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SD1ACT3	SD1ACT2	SD1ACT1	SD1ACT0	SD1RCV3	SD1RCV2	SD1RCV1	SD1RCV0

Bit 7–Bit 4 SD1ACT3–0 SD1 Data Register Port (170h) Read/Write Active Time
Definition of these bits same as PD0RCV3-0

Bit 3–Bit 0 SD1RCV3–0 SD1 Data Register Port (170h) Read/Write Recovery Time
Definition of these bits same as PD0RCV3-0

CRX8Fh (SD1TIM1) Read/Write Secondary Drive 1 Timing Control 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SD1AST1	SD1AST0	SD1DHT1	SD1DHT0	$\overline{\text{SD1PRE}}$	$\overline{\text{SD1DMA}}$	$\overline{\text{SD1RDY}}$	SD1ADV

Bit 7–Bit 6 SD1AST1–0 SD1 Data Register Port (170h) Address Setup Time
Definition of these bits same as PD0RCV3–0

Bit 5–Bit 4 SD1DHT1–0 SD1 Data Register Port (170h) Data Hold Time
Definition of these bits same as PD0RCV3–0

Bit 3 $\overline{\text{SD1PRE}}$ SD1 Prefetch/Post write control
0 Prefetch/Post write enabled
1 Prefetch/Post write disabled

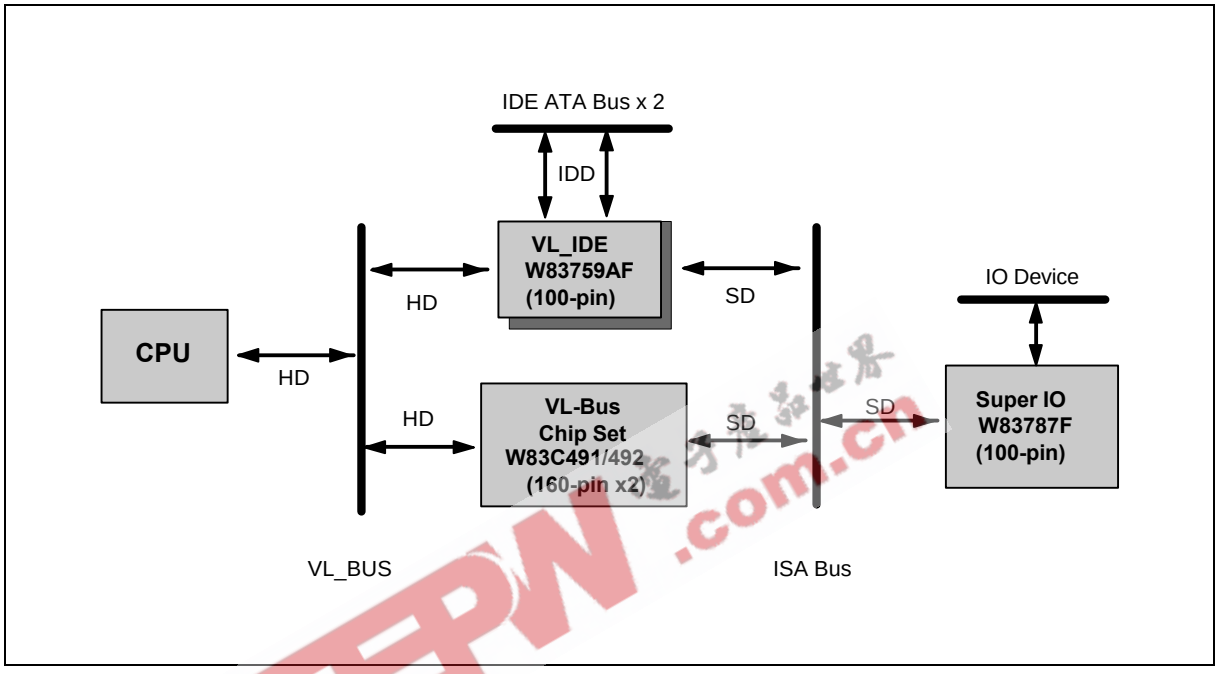
Bit 2 $\overline{\text{SD1DMA}}$ SD1 DMA mode control
0 DMA mode enabled
1 DMA mode disabled

Bit 1 $\overline{\text{SD1RDY}}$ SD1 Data Register Port (170h) IOCHRDY Control
0 IOCHRDY enabled
1 OCHRDY disabled

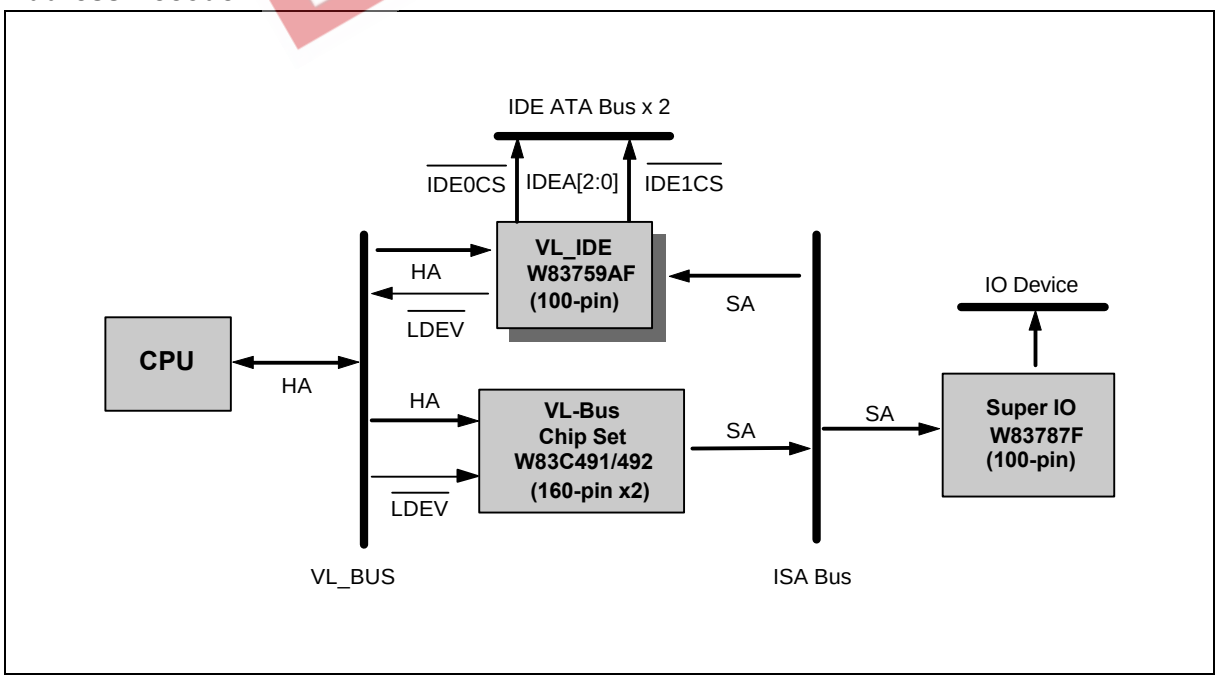
Bit 0 SD1ADV SD1 Data Register Port (170h) Advanced Timing Enable
0 Normal timing (depends on SP1, MD1, MD0 setting)
1 Advanced timing (depends on SD1TIM1–0 setting)

SYSTEM BLOCK DIAGRAM

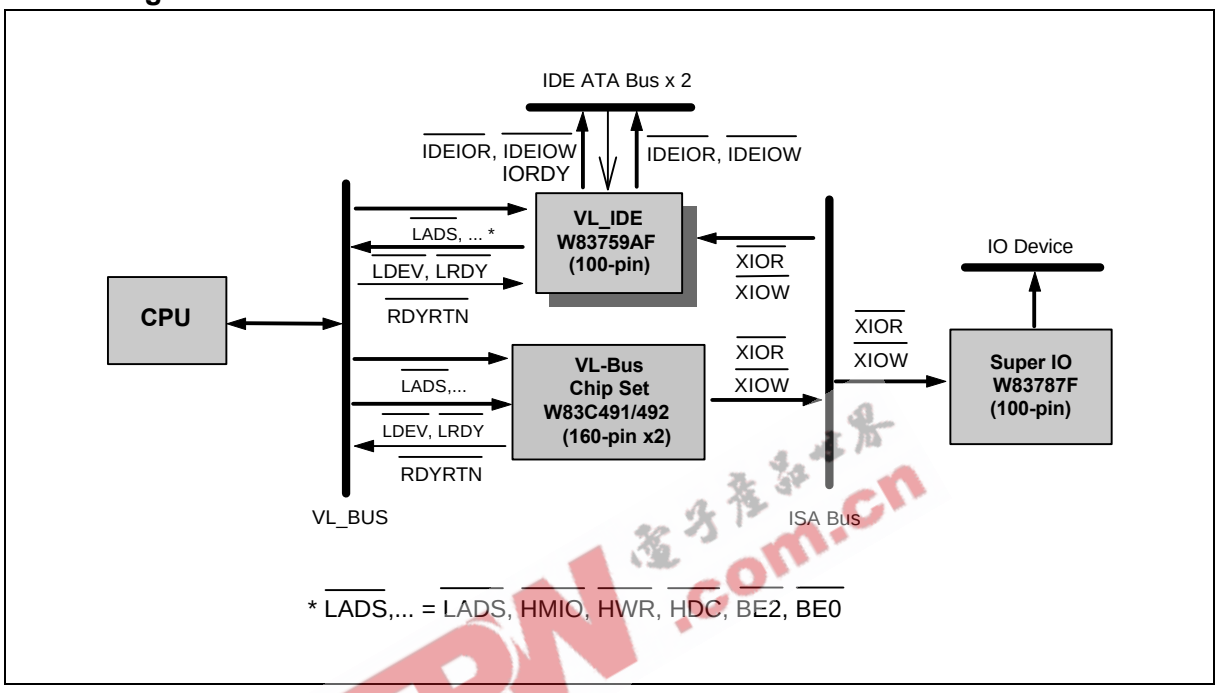
Data Flow



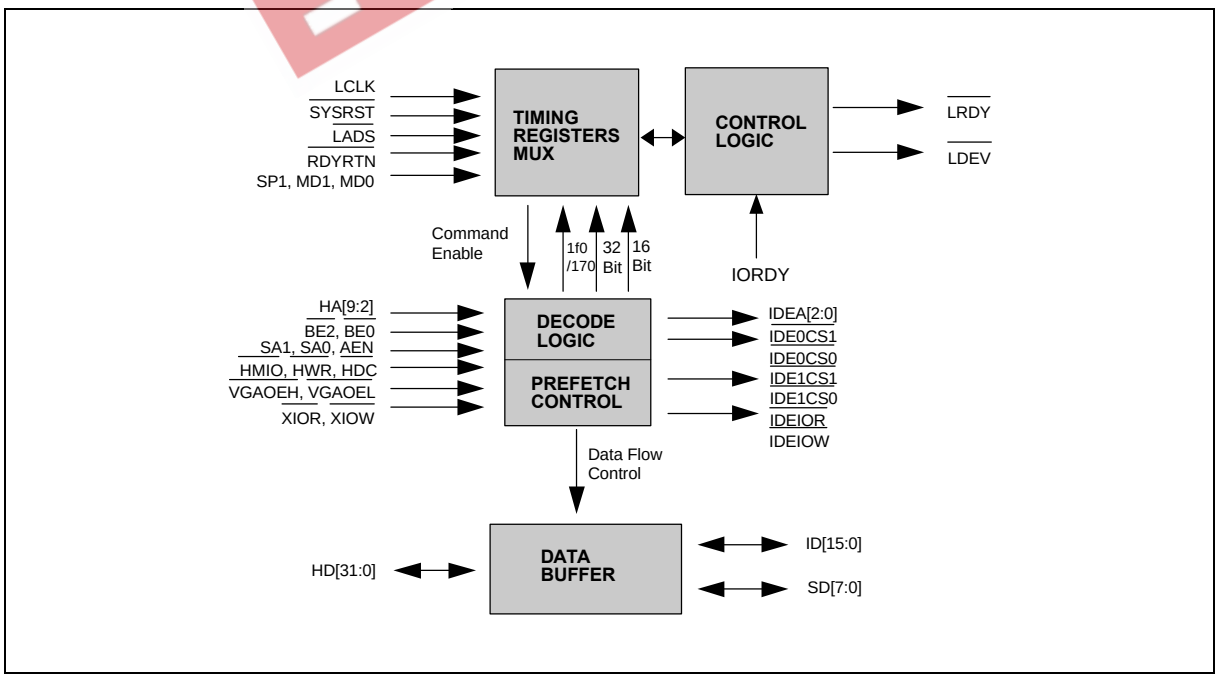
Address Decode



Control Signal



FUNCTION BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Reset Initialization

The CPU clock rate, hard disk access time, hard disk controller enable, and hard disk I/O select are latched at the rising edge of $\overline{\text{SYSRST}}$. These values are used to control the host and drive access signal timing. Additionally, the W83759A is initialized to a known state by an active low on $\overline{\text{SYSRST}}$. Any operation in progress is immediately terminated by $\overline{\text{SYSRST}}$.

Host in Terface

The W83759A operates as a slave device, responding only to cycles within the host I/O address space. The IDE drive data port at address 1F0h (170h) is a 16-bit port that requests a double-word data transfer at address 1F0h (170h). All byte swapping, conversion, word, and double-word assembly are done at the host interface. Table 1 summarizes the W83759A host interface cycle decoding.

Table 1. W83759A Cycle Definition

$\overline{\text{HMIO}}$	$\overline{\text{HDC}}$	$\overline{\text{HWR}}$	ADDRESS SPACE	HOST BUS CYCLE	W83759A CYCLE
0	1	0	1F0h–1F7h and 3F6h	I/O Read	IDE0 Read Cycle
0	1	1	1F0h–1F7h and 3F6h	I/O Write	IDE0 Write Cycle
0	1	0	170h–177h and 376h	I/O Read	IDE1 Read Cycle
0	1	1	170h–177h and 376h	I/O Write	IDE1 Write Cycle

a. CPU WRITE CYCLES

Table 2. W83759A Write Data Operation

BYTE ENABLE				W83759A INPUT DATA			I/O ADDRESS
$\overline{\text{BE3}}$	$\overline{\text{BE2}}$	$\overline{\text{BE1}}$	$\overline{\text{BE0}}$	HD[31:16]	HD[15:0]	SD[7:0]	
1	1	1	0	×	×	Valid	1F1–1F7 (171–177)
1	1	0	1	×	×	Valid	
1	0	1	1	×	×	Valid	
0	1	1	1	×	×	Valid	
1	1	0	0	×	Valid	×	1F0 (170)
0	0	0	0	Valid	Valid	×	

8-bit IDE Write Data Path:

CPU → Valid HD Byte → SD[7:0] → W83759A → ID[7:0]

16/32-bit IDE Write Data Path:

CPU → Valid HD Word → W83759A → ID[15:0]

b. CPU READ CYCLES

Table 3. W83759A Read Data Operation

BYTE ENABLE				W83759A OUTPUT DATA			I/O ADDRESS
$\overline{BE3}$	$\overline{BE2}$	$\overline{BE1}$	$\overline{BE0}$	HD[31:16]	HD[15:0]	SD[7:0]	
1	1	1	0	×	×	Valid	1F1–1F7 (171–177)
1	1	0	1	×	×	Valid	
1	0	1	1	×	×	Valid	
0	1	1	1	×	×	Valid	
1	1	0	0	×	Valid	×	1F0 (170)
0	0	0	0	Valid	Valid	×	

8-bit IDE Read Data Path:
CPU → Valid HD Byte → Chip Set → SD[7:0] → W83759A → ID[7:0]

16/32-bit IDE Read Data Path:
CPU → Valid HD Word → W83759A → ID[15:0]

Drive Interface

The W83759A is designed to work with standard IDE disk drives. For the IDE interface, the W83759A provides a 16-bit data path ID[15;0], address lines IDEA[2:0], decoded device select signals $\overline{IDE0CS0}$ ($\overline{IDE1CS0}$) and $\overline{IDE0CS1}$ ($\overline{IDE1CS1}$), and decoded command sigals $\overline{IDEIOR}$ and $\overline{IDEIOW}$.

During normal operation, the drive address outputs IDEA[2:0] are used to select a register in an IDE drive. These addresses are generated from $\overline{BE2}$, $\overline{BE0}$, HA2 and SA1, SA0. Table 4 summarizes the type enable decoding for normal operation.

Table 4. IDEA[2:0] Generation

HA2	$\overline{BE2}$	$\overline{BE0}$	SA1	SA0	IDEA[2:0]	I/O ADDRESS
0	1	0	×	×	000	1F0 (170) 16-bit
0	0	0	×	×	000	1F0 (170) 32-bit
0	×	×	0	1	001	1F1 (171)
0	×	×	1	0	010	1F2 (172)
0	×	×	1	1	011	1F3 (173)
1	×	×	0	0	100	1F4 (174)
1	×	×	0	1	101	1F5 (175)
1	×	×	1	0	110	1F6 (176)
1	×	×	1	1	111	1F7 (177)

Two drive chip select signals, $\overline{IDE0CS0}$ ($\overline{IDE1CS0}$) and $\overline{IDE0CS1}$ ($\overline{IDE1CS1}$), are generated from the local bus addresses and ISA bus address. The 16-bit data register may be read or written at I/O address 1F0h(170h). The 8-bit IDE command and status registers are at I/O addresses 1F1h through 1F7h (and 171h through 177h). The $\overline{IDEIOR}$ or $\overline{IDEIOW}$ commands are generated for all address

regions in which $\overline{\text{IDE0CS0}}$ ($\overline{\text{IDE1CS0}}$) and $\overline{\text{IDE0CS1}}$ ($\overline{\text{IDE1CS1}}$) are active. Table 5 summarizes the decoding of these sgnals.

Table 5. Drive Select Signal Operation

SELECT SIGNAL	ADDRESS RANGE
$\overline{\text{IDE0CS0}}$	I/O Address 1F0h through 1F7h
$\overline{\text{IDE0CS1}}$	I/O Address 3F6h
$\overline{\text{IDE1CS0}}$	I/O Address 170h through 177h
$\overline{\text{IDE1CS1}}$	I/O Address 376h

IDE Timing Control

Pin SP1 is used to set the VL-Bus speed. The IDE drive interface will maintain the same ATA PIO timing parameters for IDE drive 16-bit IO access cycles (1F0/170) regardless of whether the VL-Bus operates at 33 or 50 MHz.

In W83759 mode, IDE drive timing is controlled by pins MD1 and MD0, which are used to select the IDE drive PIO mode 0-2. The drive timing depends on the ATA specification for the IDE drive PIO mode selected.

In W83759A mode, IDE drive timing is controlled by pins EMD1 and EMD0, which are used to select the IDE drive PIO mode 2-4. The drive timing depends on the ATA specification for the IDE drive PIO mode selected.

Table 6 summarizes the ATA Rev. 4.0 and ATA-2 PIO timing parameters.

Table 7 and Table 8 summarize the W83759A PIO read/write command pulse and cycle timing when a 16-bit IDE IO access is performed. Because 8-bit IDE IO accesses are always passed to the ISA bus, the W83759A transceives data through the ISA data bus and induces IDE read/write commands from ISA $\overline{\text{XIOR}}$ / $\overline{\text{XIOW}}$. Thus the 8-bit command timing will always meet ATA timing specifications.

Table 6. ATA Rev. 4.0 and ATA-2 PIO Minimum Timing Parameters Unit: nS

ATA PIO	MODE 4		MODE 3		MODE 2		MODE 1		MODE 0	
8/16-bit IO access	Active Pulse	Cycle Time	Active Pulse	Cycle Time	Active Pulse	Cycle Time	Active Pulse	Cycle Time	Active Pulse	Cycle Time
16-bit	60	120	80	180	100	240	125	383	165	600
8-bit	60	120	80	180	290	290	290	383	290	600

Table 7. PIO Command Pulse and Cycle Timing (W83759 mode) Unit: LCLK

SP1	MD1	MD0	IDE WRITE ACTIVE PULSE	IDE READ ACTIVE PULSE	READ/WRITE CYCLE TIME	IDE MODE SELECT
0	0	0	6 (180)	7 (210)	22 (660)	Mode 0
0	0	1	6 (180)	7 (210)	19 (570)	Mode 0+

Table 7. PIO Command Pulse and Cycle Timing, continued

SP1	MD1	MD0	IDE WRITE ACTIVE PULSE	IDE READ ACTIVE PULSE	READ/WRITE CYCLE TIME	IDE MODE SELECT
0	1	0	8 (240)	9 (270)	13 (390)	Mode 1
0	1	1	4 (120)	5 (150)	9 (270)	Mode 2
1	0	0	9 (180)	10 (200)	31 (620)	Mode 0
1	0	1	9 (180)	10 (200)	27 (540)	Mode 0+
1	1	0	7 (140)	8 (160)	19 (380)	Mode 1
1	1	1	6 (120)	7 (140)	13 (260)	Mode 2

Note: It is recommended that SP be set to 0 when LCLK is 33 MHz. The initial default value is SP1 = 0. The timing value (nS) is based on LCLK = 20 nS when SP1 = 1 and LCLK = 30 nS when SP1 = 0.

Table 8. PIO Command Pulse and Cycle Timing (W83759A mode)

Unit: LCLK

SP1	EMD1	EMD0	IDE WRITE ACTIVE PULSE	IDE READ ACTIVE PULSE	READ/WRITE CYCLE TIME	IDE MODE SELECT
0	0	0	4 (120)	5 (150)	8 (240)	Mode 2
0	0	1	3 (90)	4 (120)	6 (180)	Mode 3
0	1	0	3 (90)	4 (120)	6 (180)	Mode 3
0	1	1	2 (60)	3 (90)	4 (120)	Mode 4
1	0	0	4 (80)	5 (100)	11 (220)	Mode 2
1	0	1	4 (80)	5 (100)	9 (180)	Mode 3
1	1	0	3 (60)	4 (80)	7 (140)	Mode 4-
1	1	1	2 (40)	3 (60)	5 (100)	Mode 4+

Note: It is recommended that SP be set to 0 when LCLK is 33 MHz. The initial default value is SP1 = 0. The timing value (nS) is based on LCLK = 20 nS when SP1 = 1 and LCLK = 30 nS when SP1 = 0.

Prefetch Control

The W83759A IDE command prefetch feature provides concurrent operations by pipelined read-ahead of the next data word(s) from the drive while the host is transferring previously requested disk data into system memory. This reduces the amount of time that the host must pause and wait for data to be accessed. While the host is writing data to memory, the W83759A reads data from the disk drive. As soon as the host reads the W83759A data, new data are requested by the W83759A from the disk drive. This prefetch feature is active only for disk data at the 1F0h and 170h IO addresses and does not oprate on other disk register data.

Power-saving Control

The W83759A provides three power-saving modes. In the initial-level power-saving mode, all of the drive's control, address, data, and other signals enter a logic 1 standby state when no IDE disk cycle is active. This reduces unnecessary power use and decreases the amount of EMI radiation generated by driving the long IDE cable continuously.

After power on, the W83759A automatically enters the "Auto-Power-Down" (APD) mode. In this mode the only active logic inside the W83759A is the host address decoder and bus tracking state machine. Power is saved by not switching logic inside the W83759A that is not being utilized. Whenever an IDE transfer cycle is detected, the W83759A leaves APD mode and the entire chip becomes active. The W83759A enters APD mode again after the completion of an IDE transfer cycle.

To support deep-green systems, the W83759A also provides advanced power saving modes, standby mode, and suspend mode. When standby mode is enabled ($\overline{STBY}$ bit goes low), all of the logic inside the W83759A is stopped until standby mode is disabled ($\overline{STBY}$ bit goes high). When suspend mode is enabled (SUSPEN bit goes high and $\overline{DMASL}$ is low on $\overline{SYSRST}$ rising), the W83759A will enter suspend state when $\overline{SUSP}$ goes low and return to normal state when $\overline{SUSP}$ goes high.

ABSOLUTE MAXIMUM RATINGS

(V_{DD} = 5 V ± 5%, V_{SS} = 0V)

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.3 to 7.0	V
Input Voltage	V_{SS}-0.3 to V_{DD} +0.3	V
Operating Temperature (Ta)	0 to + 70	°C
Storage Temperature	-55 to + 150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC CHARACTERISTICS

(TA = 0° C to +70° C, V_{DD} = 5V ± 5%, V_{SS} = 0V)

PARAMETER	SYM.	CONDITIONS	MIN.	MAX.	UNIT
Input Low Voltage	V_{IL}		-0.3	0.8	V
Input High Voltage	V_{IH}		2.0	V_{DD} + 0.3	V
Input High Leakage with Pull-Down	I_{LIHD}	V_{IN} = V_{DD}	-	+500	µA
Input Low Leakage with Pull-Up	I_{LILU}	V_{IN} = 0V	-	-500	µA
Input High Leakage	I_{LIH}	V_{IN} = V_{DD}	-	+10	µA
Input Low Leakage	I_{LIL}	V_{IN} = 0V	-	-10	µA
Output Low Voltage	V_{OL}	I_{OL} = 8 mA ($\overline{LDEV}$, SD, IDE pins) I_{OL} = 6 mA (other pins)	-	0.4	V
Output High Voltage	V_{OH}	I_{OL} = -8 mA ($\overline{LDEV}$, SD, IDE pins) I_{OL} = -6 mA (other pins)	2.4	V_{DD}	V
Input Capacitance	C_{IN}		-	5	pF
Output Capacitance	C_{OUT}		-	10	pF

DC Characteristics, continued

PARAMETER	SYM.	CONDITIONS	MIN.	MAX.	UNIT
Operating Current	IDD	FLCLK = 50 MHz	-	25	mA
Standby Current	ISTBY	All input and I/O pins pulled high, LCLK = VDD	-	800	µA

AC CHARACTERISTICS

All AC timing is measured from the 0.8V and 2.0V on the source signal to the 0.8V and 2.0V level on the signal under test.

AC specifications are given for the following testing conditions:

VDD = 5V ± 5%, Temp. = 0° C to 70° C
VL-Bus shared signal loading = 100 pF
VL-Bus non-shared signal loading = 33 pF
ISA Bus signal loading = 240 pF
IDE device interface loading = 30 pF

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	FIG.
t1	LCLK Period	20	-	nS	Fig. 1
t2	LCLK High Time	5	-	nS	Fig. 1
t3	LCLK Low Time	5	-	nS	Fig. 1
t4	$\overline{\text{SYSRST}}$ Pulse Width	16	-	LCLK	Fig. 1
t5	POS Pin to $\overline{\text{SYSRST}}$ Setup Time	200	-	nS	Fig. 1
t6	POS Pin Hold Time from $\overline{\text{SYSRST}}$	10	-	nS	Fig. 1
t7	$\overline{\text{LADS}}$ to LCLK Setup Time	6	-	nS	Fig. 2
t8	$\overline{\text{LADS}}$ Hold Time from LCLK	3	-	nS	Fig. 2
t9	$\overline{\text{LDEV}}$ Active Delay from Address	39		nS	Fig. 2
t10	VESA IO Read Host Data Drive Delay	5	16	nS	Fig. 2, 4
t11	$\overline{\text{HMIO}}$, $\overline{\text{HDC}}$, $\overline{\text{HWR}}$ to LCLK Setup Time when $\overline{\text{LDEV}}$ asserted at T2	5	-	nS	Fig. 2, 3
t12	$\overline{\text{HMIO}}$, $\overline{\text{HDC}}$, $\overline{\text{HWR}}$ to LCLK Setup Time when $\overline{\text{LDEV}}$ asserted at T2	10	-	nS	Fig. 2, 3
t13	$\overline{\text{LRDY}}$ Active Delay from LCLK	5	16	nS	Fig. 2, 3
t14	$\overline{\text{LRDY}}$ Inactive Delay from LCLK	6	18	nS	Fig. 2, 3
t15	$\overline{\text{RDYRTN}}$ to LCLK Setup Time	6	-	nS	Fig. 2, 3
t16	$\overline{\text{RDYRTN}}$ Hold Time from LCLK	3	-	nS	Fig. 2, 3
t17	VESA IO Write Host Data Valid Delay	-	20	nS	Fig. 3
t18	VESA IO Write Host Data Hold Time	0	-	nS	Fig. 3, 5

AC Characteristics, continued

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	FIG.
t19	IDEA[2:0] Valid Delay from Address Valid	-	18	nS	Fig. 4, 5
t20	IDEA[2:0] Invalid Delay from Address Change	5	18	nS	Fig. 4, 5
t21	$\overline{\text{IDE0CS0}}$, $\overline{\text{IDE1CS0}}$ Valid Delay from Address valid	-	18	nS	Fig. 4, 5
t22	$\overline{\text{IDE0CS0}}$, $\overline{\text{IDE1CS0}}$ Invalid Delay from Address Change	5	18	nS	Fig. 4, 5
t23	$\overline{\text{IDEIOR}}$, $\overline{\text{IDEIOW}}$ Active Delay from LCLK	-	22	nS	Fig. 4, 5
t24	$\overline{\text{IDEIOR}}$, $\overline{\text{IDEIOW}}$ Inactive Delay from LCLK	-	24	nS	Fig. 4, 5
t25	IDE Read IDD Data Hold Time from LCLK	0	-	nS	Fig. 4
t26	IDE Read IDD to HD Delay	-	16	nS	Fig. 4
t27	IDE Read HD Float Delay from LCLK	10	30	nS	Fig. 4
t28	IDE Write IDD Drive Delay	-	20	nS	Fig. 5
t29	IDE Write IDD Float Delay	10	30	nS	Fig. 5
t30	IDEA[2:0] Valid Delay from A2 SA[1:0] Valid	-	20	nS	Fig. 6, 7
t31	IDEA[2:0] Invalid Delay from A2 SA[1:0] Change	5	20	nS	Fig. 6, 7
t32	$\overline{\text{IDE0CS1}}$, $\overline{\text{IDE1CS1}}$ Valid Delay from Address Valid	-	17	nS	Fig. 6, 7
t33	$\overline{\text{IDE0CS1}}$, $\overline{\text{IDE1CS1}}$ Invalid Delay from Address Change	4	17	nS	Fig. 6, 7
t34	ISA IDE Read IDD to SD Delay	8	18	nS	Fig. 6
t35	ISA IDE Read IDD Data Hold Time from $\overline{\text{IDEIOR}}$	5	-	nS	Fig. 6
t36	ISA IDE Write SD to IDD Delay	8	18	nS	Fig. 7
t37	ISA IDE Wrtie SD Data Hold Time from $\overline{\text{XIOW}}$	30	-	nS	Fig. 7
t38	VGA Read IDD to HD Delay	-	16	nS	Fig. 8
t39	VGA Read HD Float Delay from $\overline{\text{VGAOEL}}$	-	20	nS	Fig. 8
t40	VGA Write HD to IDD Delay	-	16	nS	Fig. 9
t41	VGA Write HD Float Delay from $\overline{\text{VGAOEH}}$	-	20	nS	Fig. 9
t42	ISA IDD Read $\overline{\text{IDEIOR}}$ Active Delay from $\overline{\text{XIOR}}$	-	20	nS	Fig. 6
t43	ISA IDD Read $\overline{\text{IDEIOR}}$ Inactive Delay from $\overline{\text{XIOR}}$	-	20	nS	Fig. 6
t44	ISA IDE Write $\overline{\text{IDEIOW}}$ Active Delay from $\overline{\text{XIOW}}$	-	20	nS	Fig. 7
t45	ISA IDE Write $\overline{\text{IDEIOW}}$ Inactive Delay from $\overline{\text{XIOW}}$	-	20	nS	Fig. 7

TIMING WAVEFORMS

All AC timing is measured from the 0.8V and 2.0V on the source signal to the 0.8V and 2.0V level on the signal under test.

LCLK, $\overline{\text{SYSRST}}$, Timing

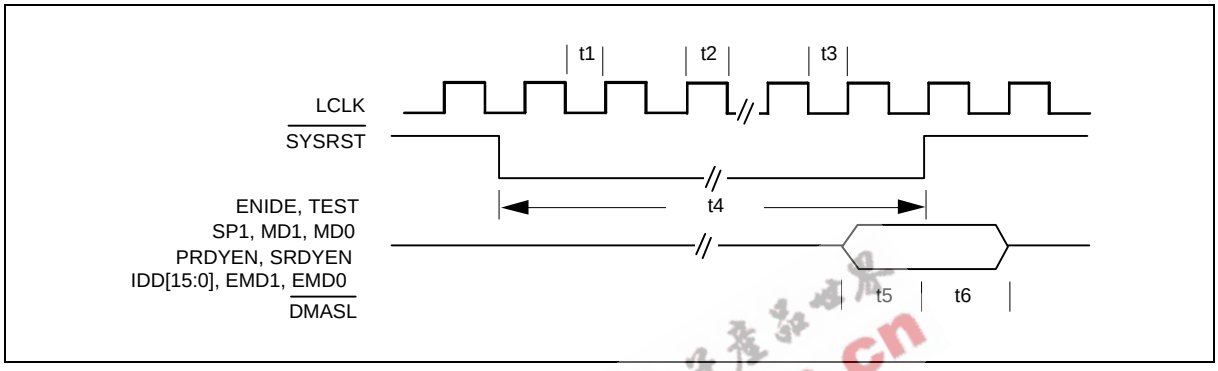


Figure 1

Note: ENIDE, TEST, SP1, MD1, MD0, PRDYEN, SRDYEN, IDD[15:0], EMD1, EMD0, $\overline{\text{DMASL}}$ are POS (Power-On Setting) pins. When $\overline{\text{SYSRST}}$ is low they are tri-stated as inputs.

VESA IO Read Timing

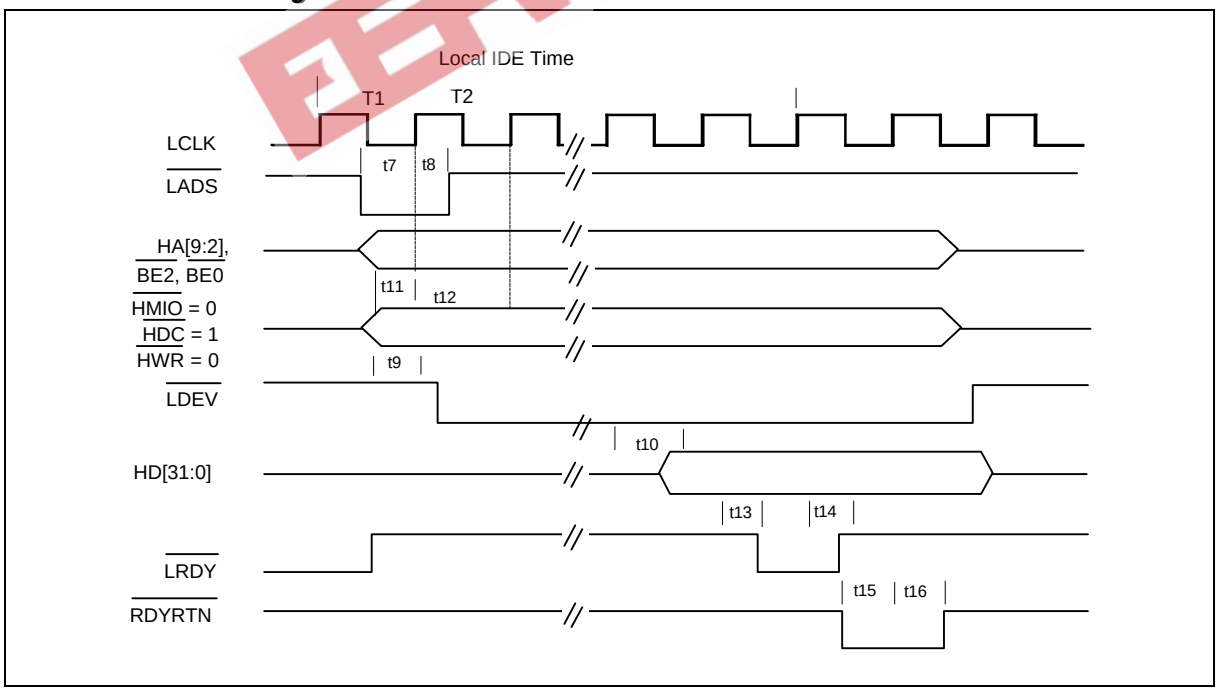


Figure 2

Note: Local IDE cycle time is determined by SP1, MD1, and MD0 or by SP1, EMD1 and EMD0 at power-on. After power-on the driver can program the timing register to tune the timing.

VESA IO Write Timing

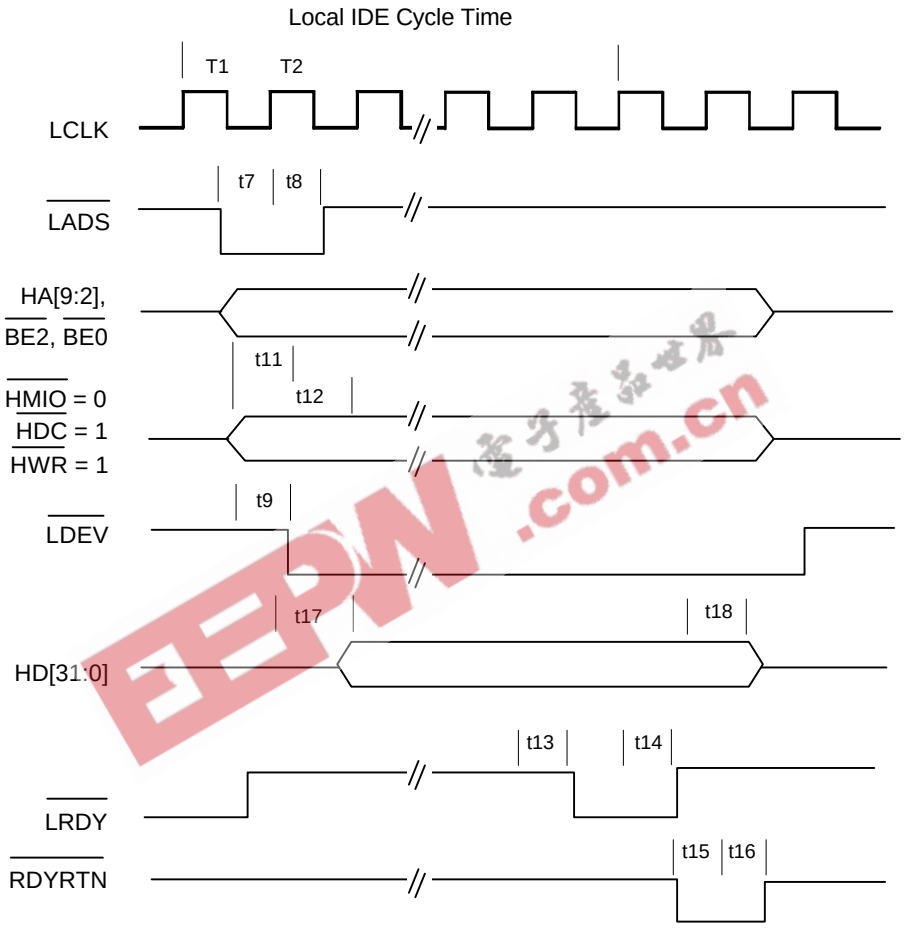


Figure 3

IDE IO Read Timing

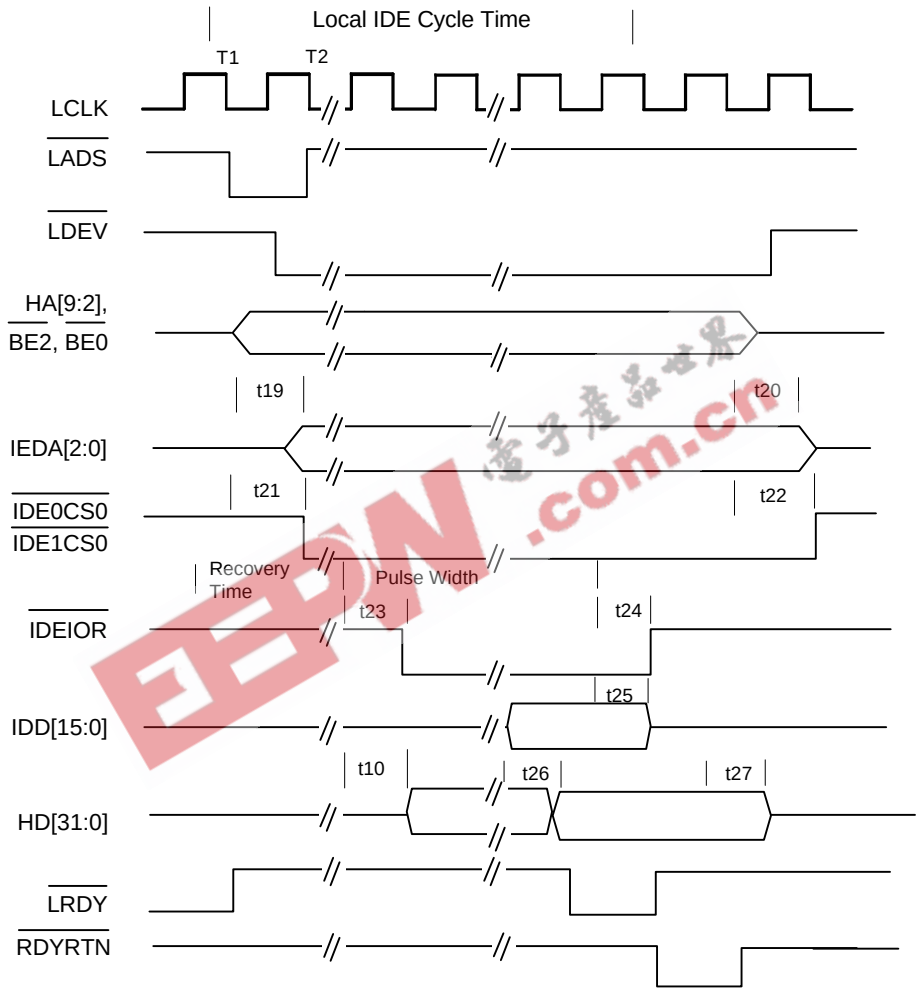


Figure 4

Note: At power-on the recovery time and pulse width are determined by SP1, MD1, and MD0, or by SP1, EMD1 and EMD0 as indicated in Table 7. and Table 8. After power-on the driver can program the timing register to tune the timing.

Example: When SP = 1 and MD1 = MD0 = 0, the $\overline{\text{IDEIOR}}$ pulse width is 10 LCLK and recovery time is 21 LCLK (cycle time is 31 LCLK).

IDE IO Write Timing

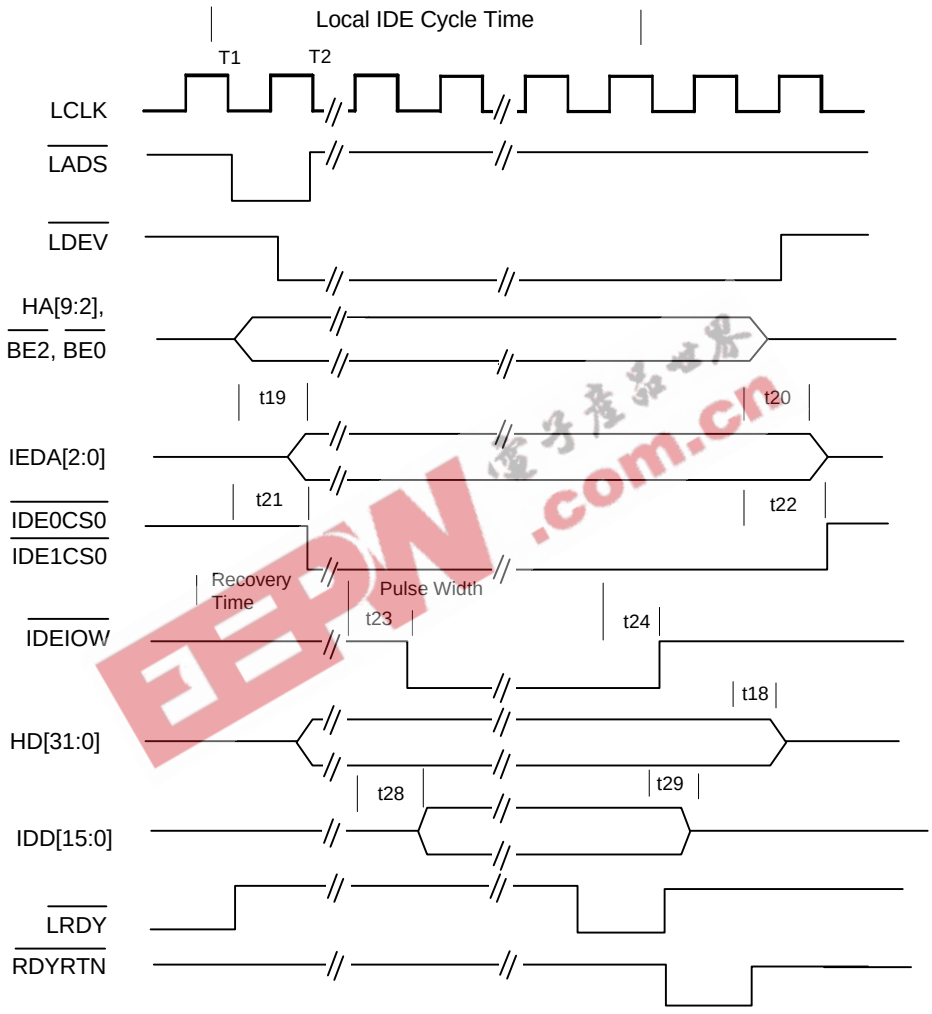


Figure 5

Note: At power-on the recovery time and pulse width are determined by SP1, MD1, and MD0 or by SP1, EMD1, and EMD0 as indicated in Table 7 and Table 8. After power-on the driver can program the timing register to tune the timing.

Example: When SP = 1 and MD1 = MD0 = 0, the $\overline{\text{IDEIOW}}$ pulse width is 9 LCLK and recovery time is 22 LCLK (cycle time is 31 LCLK).

ISA IO Read Timing

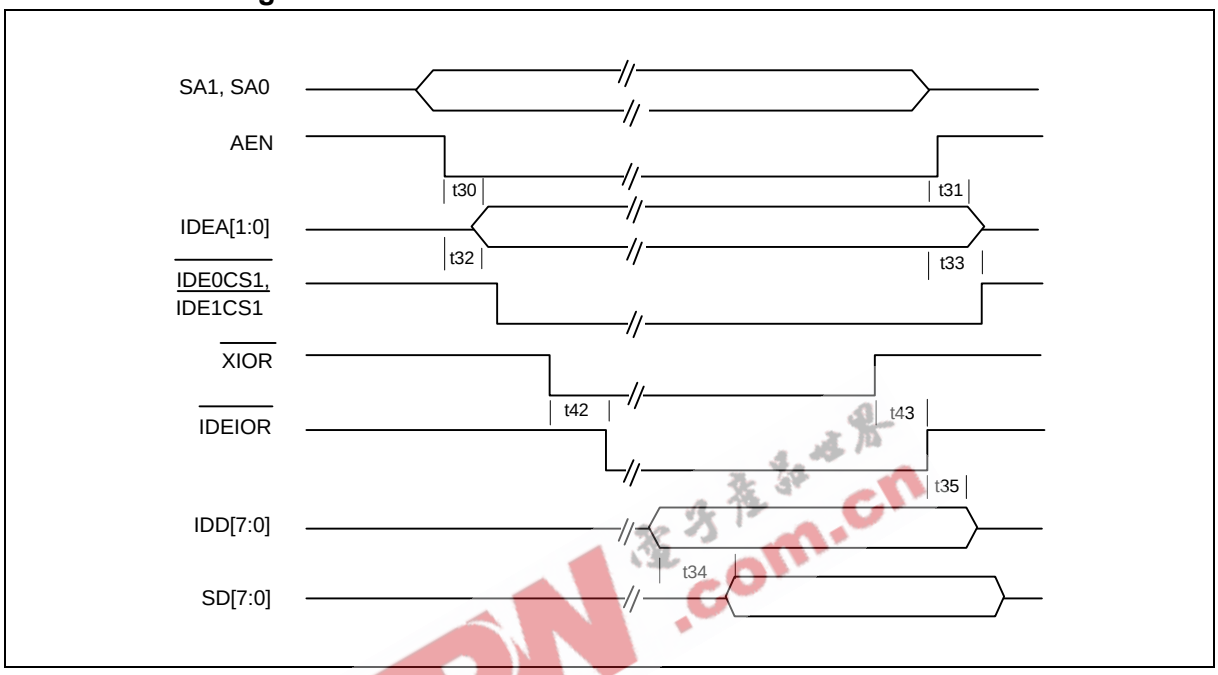


Figure 6

ISA IO Write Timing

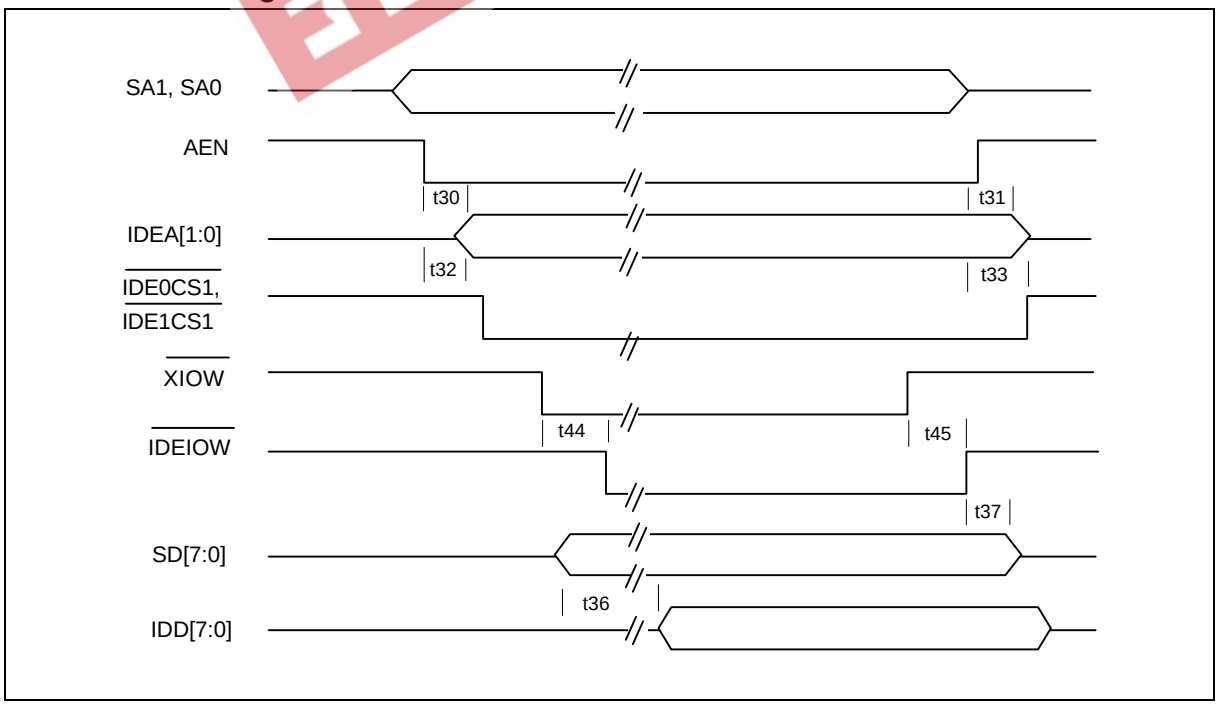


Figure 7

$\overline{\text{VGAOEL}}$ Read Timing

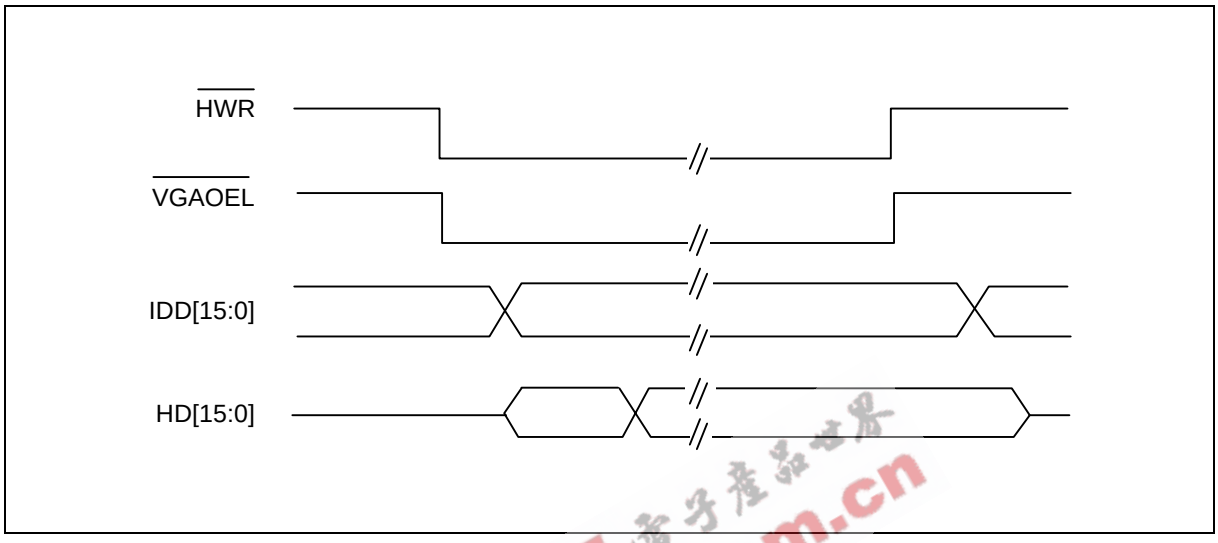


Figure 8

$\overline{\text{VGAOEH}}$ Write Timing

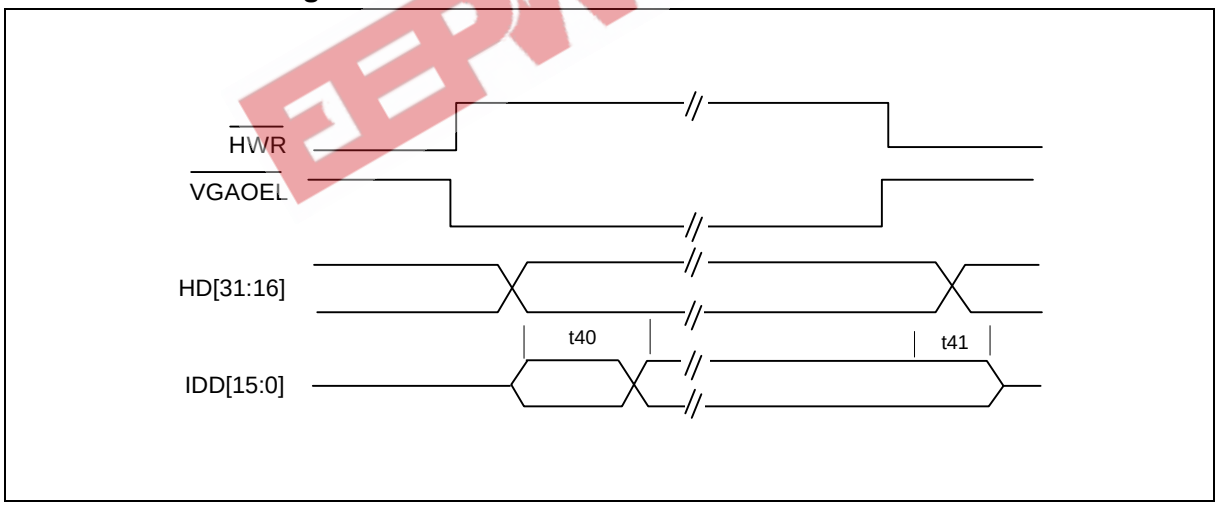
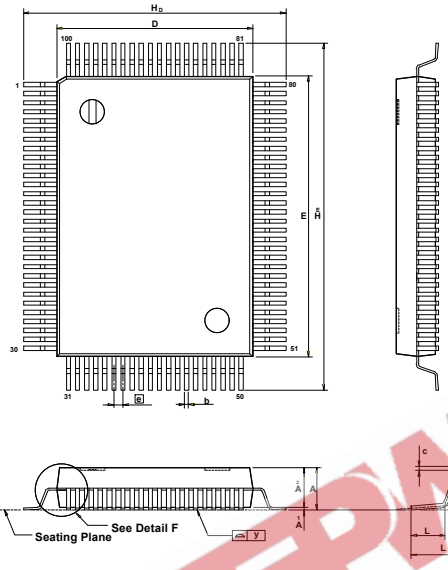


Figure 9

PACKAGE DIMENSION

100-pin QFP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom	Max.	Min.	Nom	Max.
A	—	—	0.130	—	—	3.30
A_1	0.004	—	—	0.10	—	—
A_2	0.107	0.112	0.117	2.73	2.85	2.97
b	0.010	0.012	0.016	0.25	0.30	0.40
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.546	0.551	0.556	13.87	14.00	14.13
E	0.782	0.787	0.792	19.87	20.00	20.13
G	0.020	0.026	0.032	0.50	0.65	0.80
H_D	0.728	0.740	0.752	18.49	18.80	19.10
H_E	0.964	0.976	0.988	24.49	24.80	25.10
L	0.039	0.047	0.055	1.00	1.20	1.40
L_1	0.087	0.094	0.103	2.21	2.40	2.62
y	—	—	0.004	—	—	0.10
θ	0°	—	12°	0°	—	12°

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

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