# 512Kx32 SRAM 3.3V MULTI-CHIP PACKAGE

## FEATURES

- Access Times of 12, 15, 17, 20ns
- Packaging
  - 143 PBGA, 16mm x 18mm, 288mm$^2$
- Organized as 512Kx32; User Configurable as 1Mx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges
- Low Voltage Operation:
  - 3.3V ± 10% Power Supply
- Low Power Data Retention 'L' Option
- TTL Compatible Inputs and Outputs
- Fully Static Operation:
  - No clock or refresh required.
- Three State Output.



### PIN CONFIGURATION FOR WEDPS512K32V-XBX

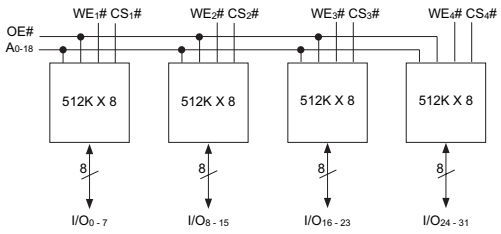
**Top View**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | - | A2 | A1 | A0 | GND | GND | VCC | VCC | A18 | A17 | A16 | GND |
| B | CS2# | A3 | A4 | D14 | D15 | NC | CS4# | D24 | D25 | OE# | A15 | NC |
| C | D9 | D8 | NC | D12 | D13 | GND | VCC | D26 | D27 | WE4# | D31 | D30 |
| D | D10 | D11 | GND | GND | GND | GND | VCC | VCC | VCC | VCC | D28 | D29 |
| E | WE2# | GND | GND | GND | GND | GND | VCC | VCC | VCC | VCC | VCC | NC |
| F | GND | GND | GND | GND | GND | GND | VCC | VCC | VCC | VCC | VCC | VCC |
| G | VCC | VCC | VCC | VCC | VCC | VCC | GND | GND | GND | GND | GND | GND |
| H | CS1# | VCC | VCC | VCC | VCC | VCC | GND | GND | GND | GND | GND | NC |
| J | D1 | D0 | VCC | VCC | VCC | VCC | GND | GND | GND | GND | D23 | D22 |
| K | D2 | D3 | NC | D7 | D5 | VCC | GND | D17 | D16 | CS3# | D20 | D21 |
| L | WE1# | A6 | A5 | D6 | D4 | NC | WE3# | D19 | D18 | A14 | A13 | NC |
| M | GND | A7 | A8 | A9 | vcc | vcc | GND | GND | A10 | A11 | A12 | vcc |

### Pin Description

| | |
|---|---|
| $I/O_{0-31}$ | Data Inputs/Outputs |
| $A_{0-18}$ | Address Inputs |
| $WE_{1-4}$# | Write Enables |
| $CS_{1-4}$# | Chip Selects |
| OE# | Output Enable |
| $V_{CC}$ | Power Supply |
| GND | Ground |
| NC | Not Connected |

### Block Diagram



## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating Temperature | $T_A$ | -55 | +125 | °C |
| Storage Temperature | $T_{STG}$ | -65 | +150 | °C |
| Signal Voltage Relative to GND | $V_G$ | -0.5 | 4.6 | V |
| Junction Temperature | $T_J$ | | 150 | °C |
| Supply Voltage | $V_{CC}$ | -0.5 | 4.6 | V |

## TRUTH TABLE

| CS# | OE# | WE# | Mode | Data I/O | Power |
|---|---|---|---|---|---|
| H | X | X | Standby | High Z | Standby |
| L | L | H | Read | Data Out | Active |
| L | X | L | Write | Data In | Active |
| L | H | H | Out Disable | High Z | Active |

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 3.0 | 3.6 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | $V_{CC}$ + 0.3 | V |
| Input Low Voltage | $V_{IL}$ | -0.3 | +0.8 | V |

## BGA THERMAL RESISTANCE

| Parameter | Symbol | Max | Unit | Note |
|---|---|---|---|---|
| Junction to Ambient (No Airflow) | Theta JA | 16.9 | °C/W | 1 |
| Junction to Ball | Theta JB | 11.3 | °C/W | 1 |
| Junction to Case (Top) | Theta JC | 9.8 | °C/W | 1 |

NOTE: Refer to Application Note "PBGA Thermal Resistance Correlation" at www.wedc.com in the application notes section for modeling conditions.

## CAPACITANCE

Ta = +25°C

| Parameter | Symbol | Conditions | Max | Unit |
|---|---|---|---|---|
| OE# capacitance | $C_{OE}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 30 | pF |
| $WE_{1-4}$# capacitance | $C_{WE}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 10 | pF |
| $CS_{1-4}$# capacitance | $C_{CS}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 10 | pF |
| Data I/O capacitance | $C_{I/O}$ | $V_{I/O}$ = 0 V, f = 1.0 MHz | 10 | pF |
| Address input capacitance | $C_{AD}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 30 | pF |

This parameter is guaranteed by design but not tested.

## DC CHARACTERISTICS

$V_{CC}$ = 3.3V ± 0.3V, -55°C ≤ $T_A$ ≤ +125°C

| Parameter | Symbol | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | $V_{IN}$ = GND to $V_{CC}$ | | 10 | µA |
| Output Leakage Current | $I_{LO}$ | CS# = $V_{IH}$, OE# = $V_{IH}$, $V_{OUT}$ = GND to $V_{CC}$ | | 10 | µA |
| Operating Supply Current (x 32 Mode) | $I_{CC}$ x 32 | CS# = $V_{IL}$, OE# = $V_{IH}$, f = 5MHz, $V_{CC}$ = 3.6V | | 400 | mA |
| Standby Current | $I_{SB}$ | CS# = $V_{IH}$, OE# = $V_{IH}$, f = 5MHz, $V_{CC}$ = 3.6V | | 120 | mA |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 4.0mA | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -4.0mA | 2.4 | | V |

NOTE: DC test conditions: $V_{IH}$ = $V_{CC}$ -0.3V, $V_{IL}$ = 0.3V.
Contact factory for low power option.

## DATA RETENTION CHARACTERISTICS (WEDPS512K32LV-XBX only)

-55°C ≤ $T_A$ ≤ +125°C

| Parameter | Symbol | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| Data Retention Voltage | $V_{CC}$ | $V_{CC}$ = 2.19V | 2.19 | | V |
| Data Retention Current | $I_{CCDR}$ | CS = $V_{CC}$ - 0.2V | | 8.0 | mA |

## AC CHARACTERISTICS

$V_{CC}$ = 3.3V, -55°C ≤ $T_A$ ≤ +125°C

| Parameter Read Cycle | Symbol | -12 | | -15 | | -17 | | -20 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | $t_{RC}$ | 12 | | 15 | | 17 | | 20 | | ns |
| Address Access Time | $t_{AA}$ | | 12 | | 15 | | 17 | | 20 | ns |
| Output Hold from Address Change | $t_{OH}$ | 0 | | 0 | | 0 | | 0 | | ns |
| Chip Select Access Time | $t_{ACS}$ | | 12 | | 15 | | 17 | | 20 | ns |
| Output Enable to Output Valid | $t_{OE}$ | | 7 | | 8 | | 8 | | 10 | ns |
| Chip Select to Output in Low Z | $t_{CLZ}$[1] | 1 | | 1 | | 1 | | 1 | | ns |
| Output Enable to Output in Low Z | $t_{OLZ}$[1] | 0 | | 0 | | 0 | | 0 | | ns |
| Chip Disable to Output in High Z | $t_{CHZ}$[1] | | 7 | | 8 | | 8 | | 10 | ns |
| Output Disable to Output in High Z | $t_{OHZ}$[1] | | 7 | | 8 | | 8 | | 10 | ns |

1. This parameter is guaranteed by design but not tested.

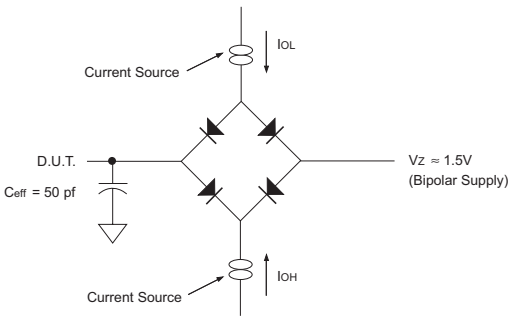
## AC CHARACTERISTICS

$V_{CC}$ = 3.3V, -55°C ≤ $T_A$ ≤ +125°C

| Parameter Write Cycle | Symbol | -12 | | -15 | | -17 | | -20 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | $t_{WC}$ | 12 | | 15 | | 17 | | 20 | | ns |
| Chip Select to End of Write | $t_{CW}$ | 10 | | 12 | | 12 | | 14 | | ns |
| Address Valid to End of Write | $t_{AW}$ | 10 | | 12 | | 12 | | 14 | | ns |
| Data Valid to End of Write | $t_{DW}$ | 8 | | 9 | | 9 | | 10 | | ns |
| Write Pulse Width | $t_{WP}$ | 10 | | 12 | | 14 | | 14 | | ns |
| Address Setup Time | $t_{AS}$ | 0 | | 0 | | 0 | | 0 | | ns |
| Address Hold Time | $t_{AH}$ | 0 | | 0 | | 0 | | 0 | | ns |
| Output Active from End of Write | $t_{OW}$[1] | 2 | | 2 | | 3 | | 3 | | ns |
| Write Enable to Output in High Z | $t_{WHZ}$[1] | | 7 | | 8 | | 8 | | 9 | ns |
| Data Hold Time | $t_{DH}$ | 0 | | 0 | | 0 | | 0 | | ns |

1. This parameter is guaranteed by design but not tested.

## FIGURE 4 – AC TEST CIRCUIT

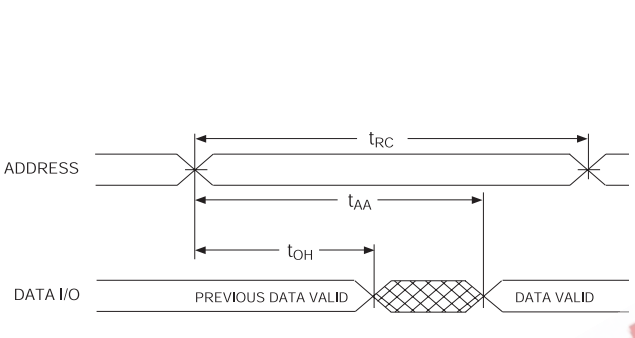



### AC Test Conditions

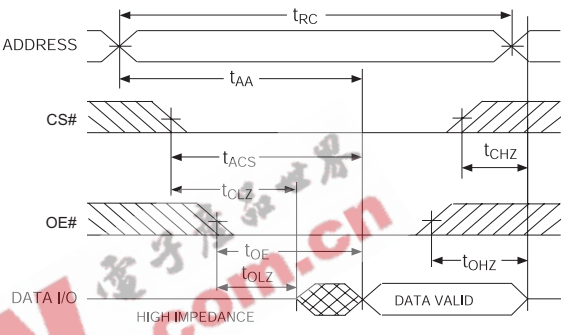
| Parameter | Typ | Unit |
|---|---|---|
| Input Pulse Levels | $V_{IL}$ = 0, $V_{IH}$ = 3.0 | V |
| Input Rise and Fall | 5 | ns |
| Input and Output Reference Level | 1.5 | V |
| Output Timing Reference Level | 1.5 | V |

Notes:
$V_Z$ is programmable from -2V to +7V.
$I_{OL}$ & $I_{OH}$ programmable from 0 to 16mA.
Tester Impedance Z0 = 75 Ω.
$V_Z$ is typically the midpoint of $V_{OH}$ and $V_{OL}$.
$I_{OL}$ & $I_{OH}$ are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

## TIMING WAVEFORM - READ CYCLE

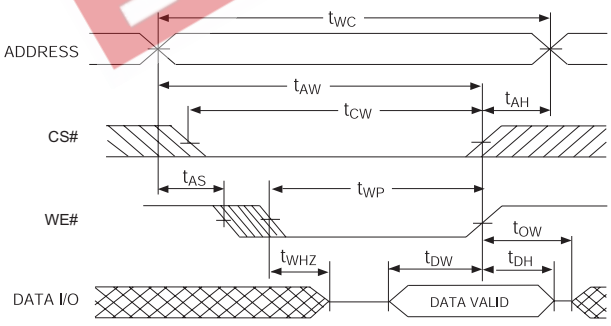



READ CYCLE 2, (CS# = OE# = $V_{IL}$, WE# = $V_{IH}$)



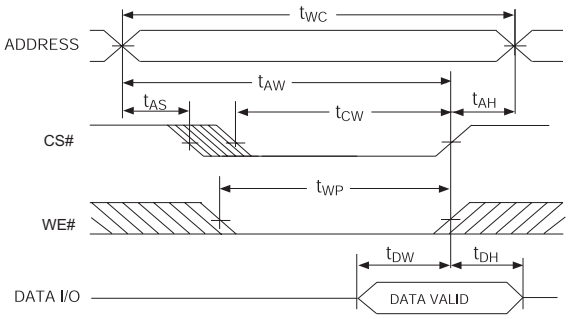

READ CYCLE 2 (WE# = $V_{IH}$)

## WRITE CYCLE - WE# CONTROLLED



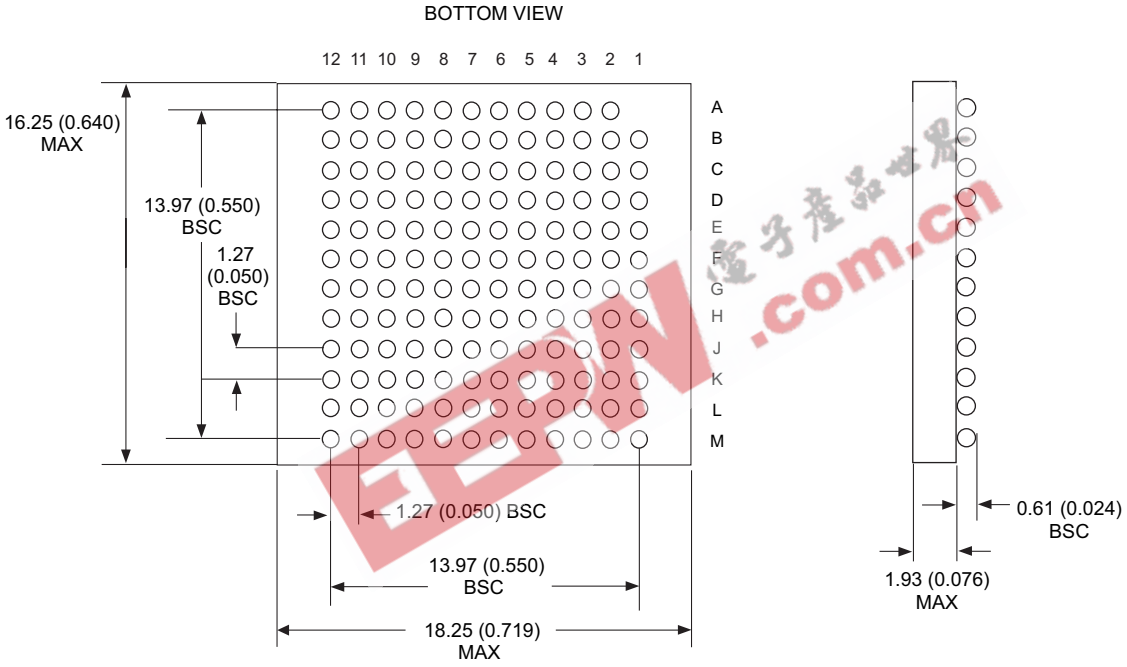

WRITE CYCLE 1, WE# CONTROLLED

## WRITE CYCLE - CS# CONTROLLED



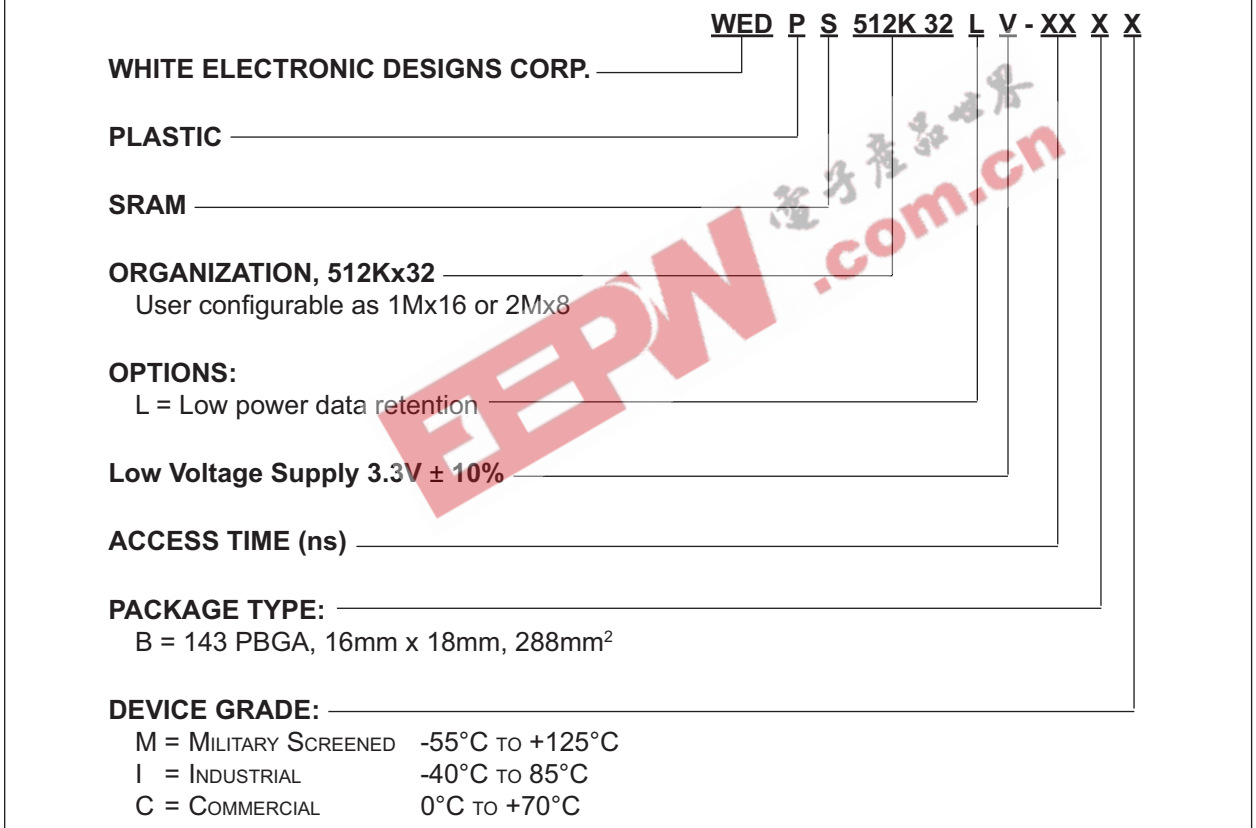

WRITE CYCLE 2, CS# CONTROLLED

## PACKAGE 756: 143 BALL GRID ARRAY




ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

## ORDERING INFORMATION



## Document Title

512K x 32 SRAM PBGA Multi-Chip Package

## Revision History

| Rev # | History | Release Date | Status |
|---|---|---|---|
| Rev 0 | Initial Release | March 2002 | Advanced |
| Rev 1 | Changes (Pg. 1)<br>1.1 Switch Rows and Columns header position | March 2002 | Advanced |
| Rev 2 | Changes (Pg. 1)<br>2.1 Switch Rows and Columns header position (Pg. 1) | May 2002 | Advanced |
| Rev 3 | Changes (Pg. 1, 5)<br>3.1 Remove excess white space from package drawing for to create a consistent accurate style. | May 2002 | Advanced |
| Rev 4 | Changes (Pg. 1, 2, 7)<br>4.1 Add Thermal Resistance Table<br>4.2 Change product status to Final | January 2003 | Final |
| Rev 5 | Changes (Pg. 1, 2, 6, 7)<br>5.1 Add low power data retention option | June 2004 | Final |