



# 32Kx8 Static RAM

## Features

- **Low Voltage Range**  
— 4.5V–5.5V Operation
- **Low active power**  
— 275 mW (max.)
- **Low standby power**  
— 28 μW (max.)
- **Easy memory expansion with CE and OE features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

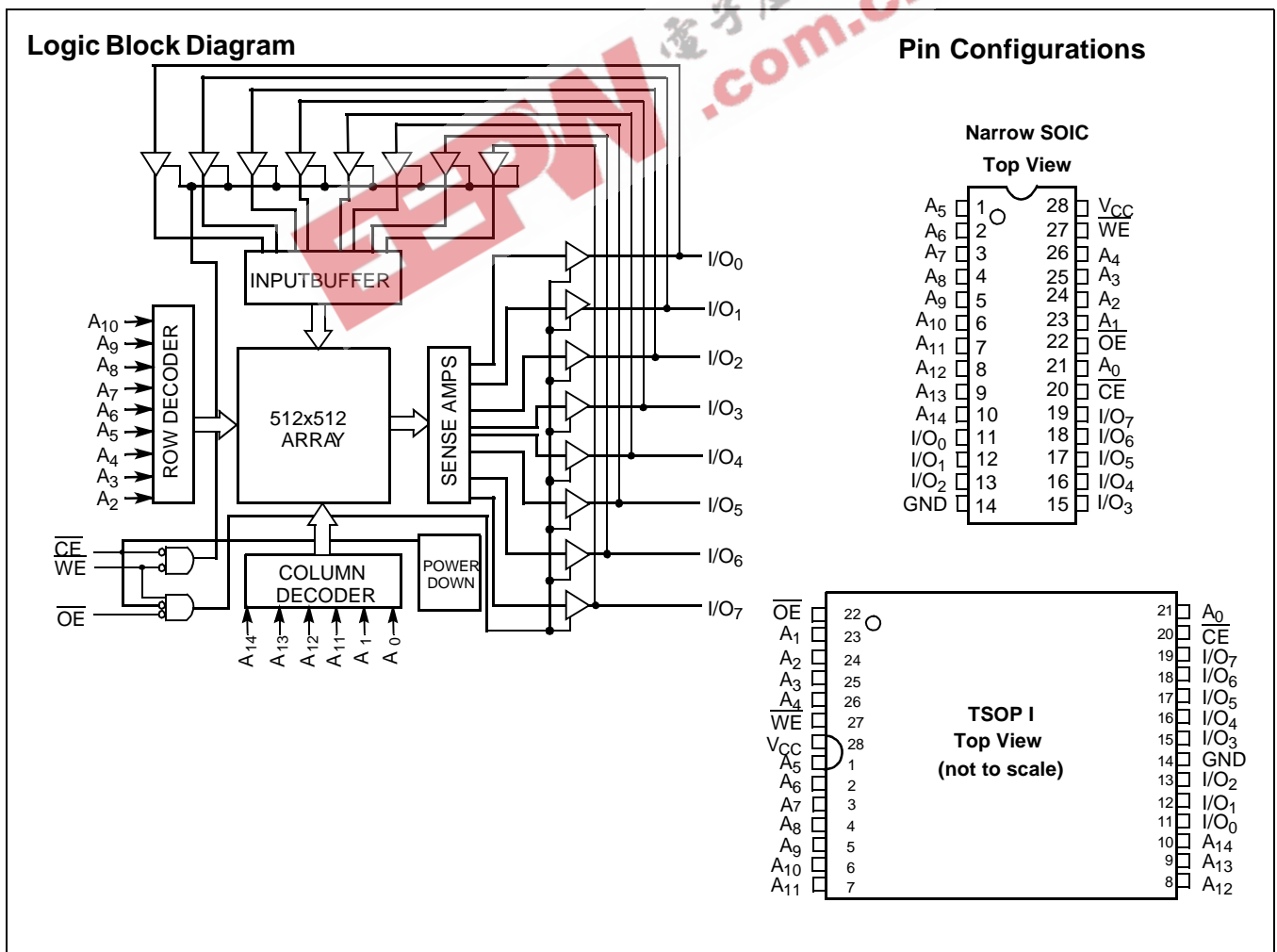
## Functional Description

The WCMS0808C1X is a high-performance CMOS static RAM organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and active

LOW output enable ( $\overline{OE}$ ) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 99.9% when deselected. The WCMS0808C1X is in the standard 450-mil-wide (300-mil body width) SOIC and packages.

An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When  $\overline{CE}$  and  $\overline{WE}$  inputs are both LOW, data on the eight data input/output pins ( $I/O_0$  through  $I/O_7$ ) is written into the memory location addressed by the address present on the address pins ( $A_0$  through  $A_{14}$ ). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{CE}$  and  $\overline{OE}$  active LOW, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH.





**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied..... 0°C to +70°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14)..... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State<sup>[1]</sup>..... -0.5V to V<sub>CC</sub> + 0.5V

DC Input Voltage<sup>[1]</sup>..... -0.5V to V<sub>CC</sub> + 0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40°C to +85°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range

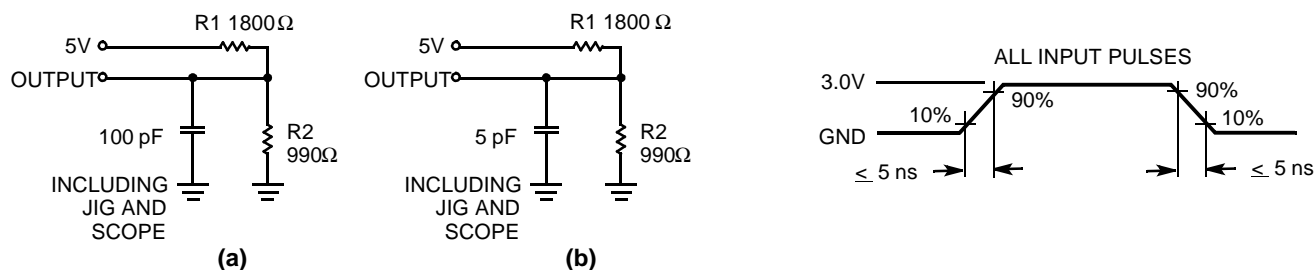
Parameter	Description	Test Conditions	WCMS0808C1X			Unit
			Min.	Typ <sup>[2]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -1.0 mA	2.4			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 2.1 mA			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2		V <sub>CC</sub> + 0.5V	V
V <sub>IL</sub>	Input LOW Voltage		-0.5		0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-0.5		+0.5	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-0.5		+0.5	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		25	50	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current—TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		0.3	0.5	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0		0.1	10	μA

**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Note:**

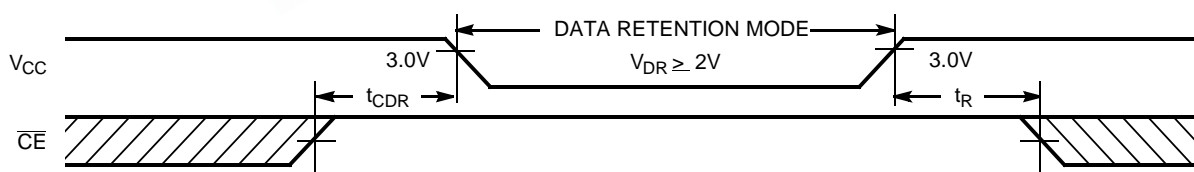
1. V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.
2. Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions (T<sub>A</sub> = 25°C, V<sub>CC</sub>). Parameters are guaranteed by design and characterization, and not 100% tested.
3. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


Equivalent to: THÉVENIN EQUIVALENT  
 $639\Omega$   
 OUTPUT  $\text{---} 1.77\text{V}$

**Data Retention Characteristics**

Parameter	Description	Conditions <sup>[4]</sup>	Min.	Typ. <sup>[2]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention	$V_{CC} = 3.0\text{V}$ , $CE \geq V_{CC} - 0.3\text{V}$ , $V_{IN} \geq V_{CC} - 0.3\text{V}$ or $V_{IN} \leq 0.3\text{V}$	2.0			V
$I_{CCDR}$	Data Retention Current			0.1	10	$\mu\text{A}$
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[3]}$	Operation Recovery Time		$t_{RC}$			ns

**Data Retention Waveform**

**Note:**

4. No input may exceed  $V_{CC}+0.5\text{V}$ .

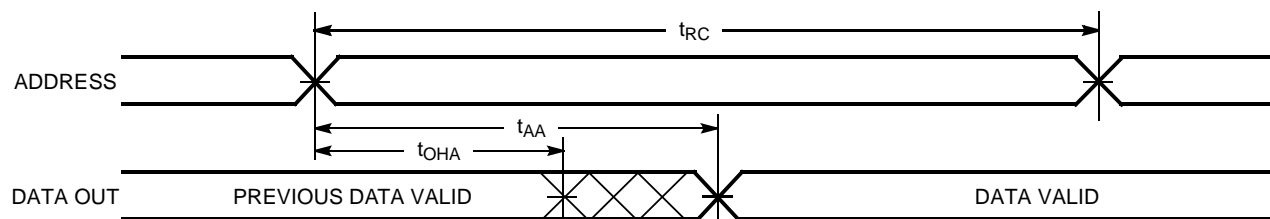
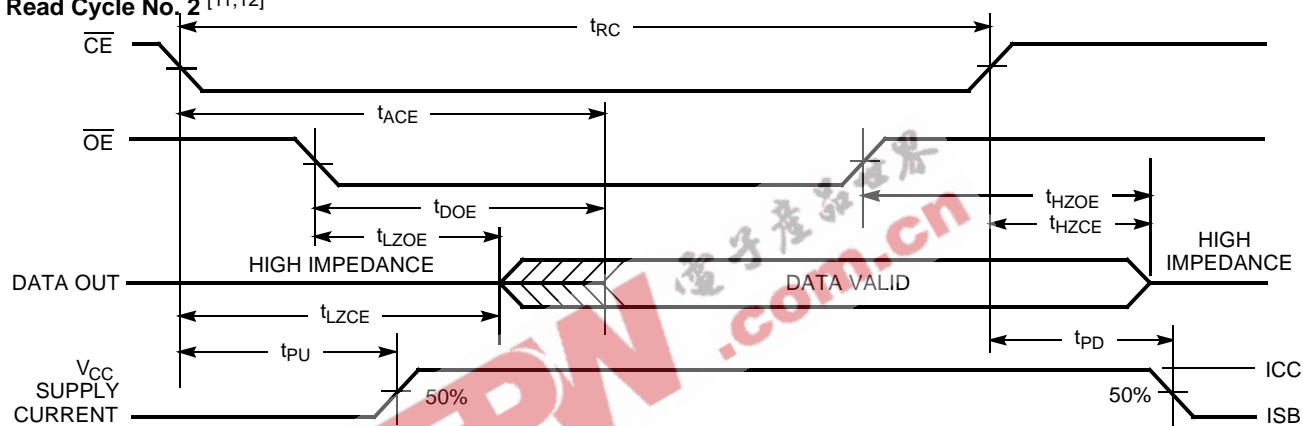


Switching Characteristics Over the Operating Range<sup>[10]</sup>

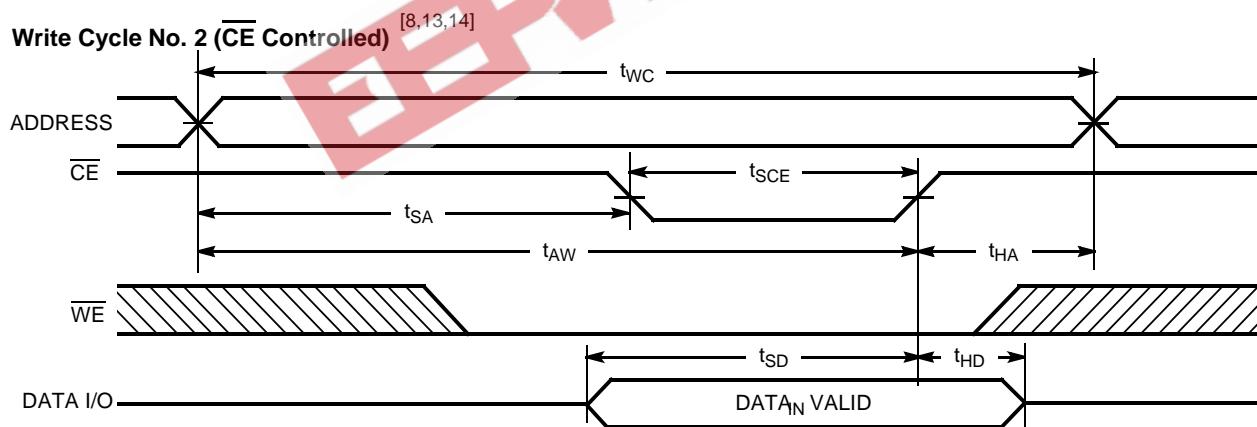
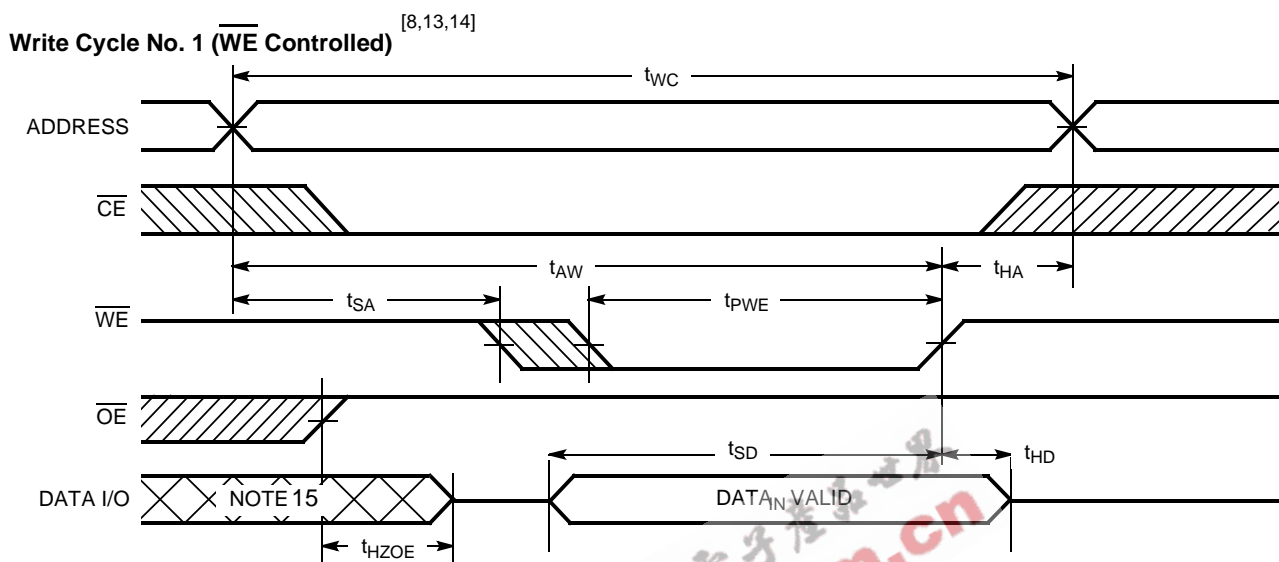
Parameter	Description	WCMS0808C1X		Unit
		Min.	Max.	
READ CYCLE				
t <sub>RC</sub>	Read Cycle Time	70		ns
t <sub>AA</sub>	Address to Data Valid		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	5		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[6]</sup>	5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	5		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		25	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		70	ns
WRITE CYCLE <sup>[8, 9]</sup>				
t <sub>WC</sub>	Write Cycle Time	70		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	60		ns
t <sub>AW</sub>	Address Set-Up to Write End	60		ns
t <sub>HA</sub>	Address Hold from Write End	0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	50		ns
t <sub>SD</sub>	Data Set-Up to Write End	30		ns
t <sub>HD</sub>	Data Hold from Write End	0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		25	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	5		ns

Notes:

5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 100-pF load capacitance.
6. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
7. t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 (WE controlled, OE LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

**Switching Waveforms**
**Read Cycle No. 1** <sup>[10,11]</sup>

**Read Cycle No. 2** <sup>[11,12]</sup>

**Notes:**

10. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

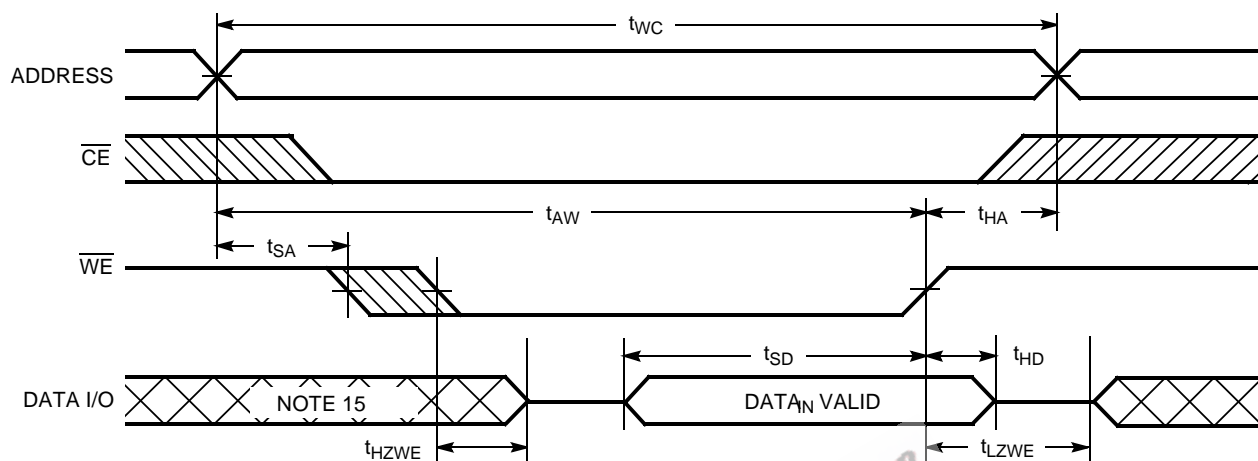
**Switching Waveforms (continued)**

**Notes:**

13. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
14. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.



Switching Waveforms (continued)

Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) <sup>[9,14]</sup>



Note:

15. During this period, the I/Os are in output state and input signals should not be applied.

Truth Table

CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	X	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Deselect, Output Disabled	Active ( $I_{CC}$ )

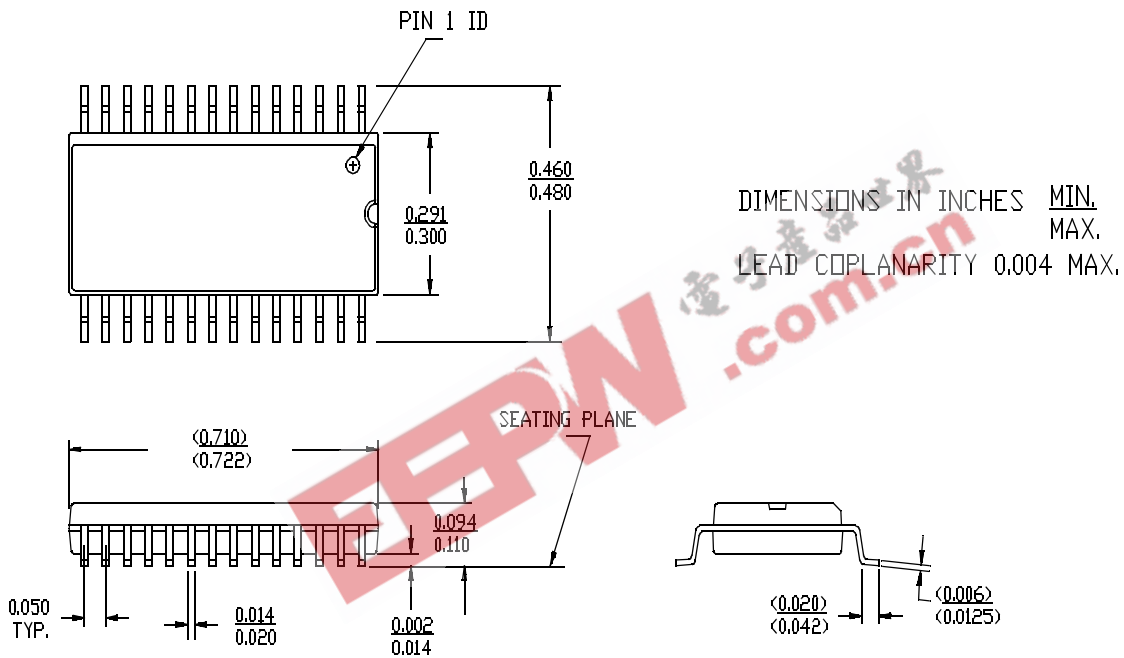


Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	WCMS0808C1X-NF70	N28	28-Lead 450-Mil (300-Mil Body Width) Narrow SOIC	Industrial
	WCMS0808C1X-TF70	T28	28-Lead Thin Small Outline Package (TSOP)	

Package Diagrams

28-Lead 450-Mil (300-Mil Body Width) SOIC, N28





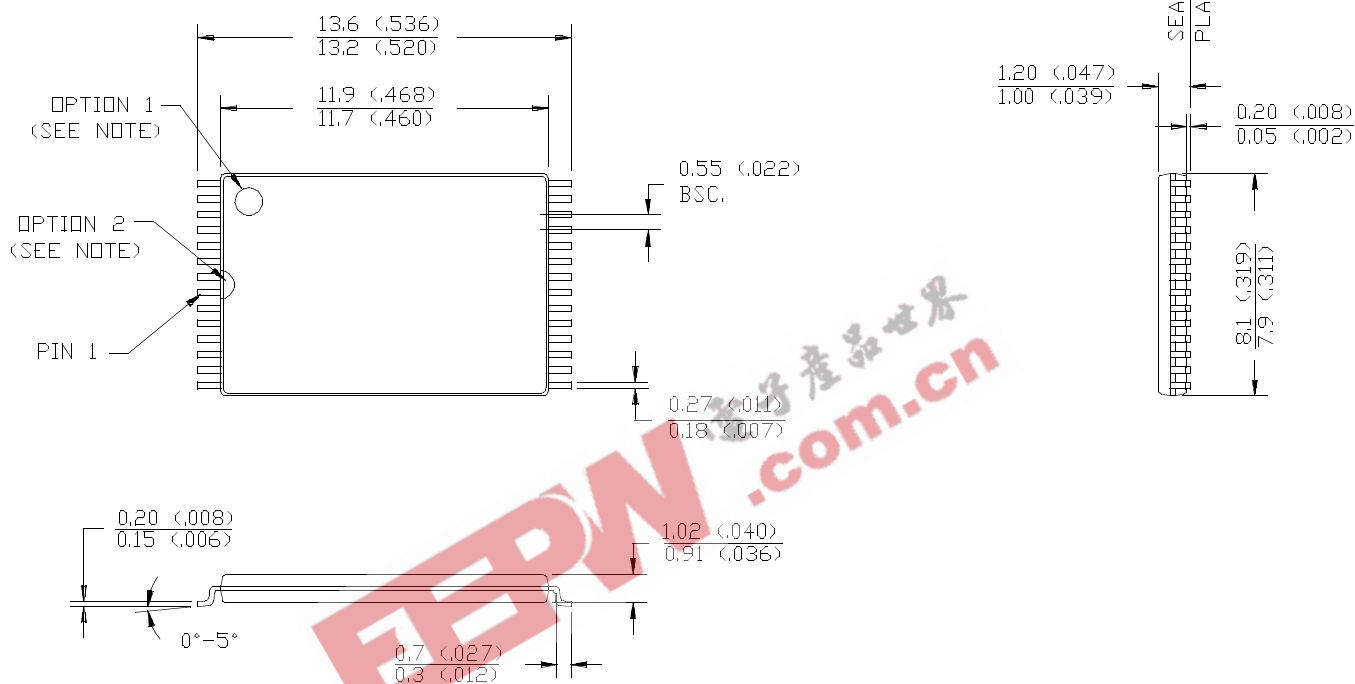


Package Diagrams (continued)

28-Lead Thin Small Outline Package, T28

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2

DIMENSION IN MM (INCH)  
MAX.  
MIN.



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**WCMS0808C1X**

**32Kx8 Static RAM**

Document Title: WCMS0808C1X, 32K x 8 Static RAM					
REV.	Spec #	ECN #	Issue Date	Orig. of Change	Description of Change
**	38-14010	115225	1/17/02	MGN	New Datasheet

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