128Kx8 MONOLITHIC SRAM, SMD 5962-96691

FEATURES

- Access Times 70, 85, 100, 120ns
- Revolutionary, Center Power/Ground Pinout JEDEC Approved
  - 32 lead Ceramic SOJ (Package 101)
- Evolutionary, Corner Power/Ground Pinout JEDEC Approved
  - 32 pin Ceramic DIP (Package 300)
  - 32 lead Ceramic SOJ (Package 101)
  - 32 lead Ceramic Flat Pack (Package 206)
- MIL-STD-883 Compliant Devices Available
- Commercial, Industrial and Military Temperature Range
- 5 Volt Power Supply
- Low Power CMOS
- 2V Data Retention Devices Available (Low Power Version)
- TTL Compatible Inputs and Outputs

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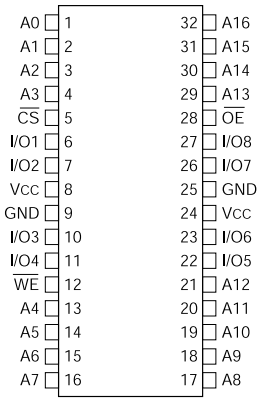
REVOLUTIONARY PINOUT

32 CSOJ (DR)

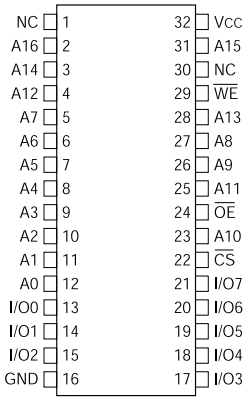
TOP VIEW



EVOLUTIONARY PINOUT

32 DIP (C)
32 CSOJ (DE)
32 FLATPACK (FE)

TOP VIEW



PIN DESCRIPTION

A_{0-16}	Address Inputs
I/O_{0-7}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5.0V Power
GND	Ground

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

CAPACITANCE
(TA = +25°C)

Parameter	Symbol	Condition	Package	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V, f = 1.0MHz	32 Pin CSOJ, DIP, Flat Pack Evolutionary	12	pF
			32 Pin CSOJ Revolutionary	20	pF
Output capicitance	C_{OUT}	V_{OUT} = 0V, f = 1.0MHz	32 Pin CSOJ, DIP, Flat Pack Evolutionary	12	pF
			32 Pin CSOJ Revolutionary	20	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS
(VCC = 5.0V, GND = 0V, TA = -55°C TO +125°C)

Parameter	Sym	Conditions	-70		-85		-100		-120		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10		10		10		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10		10		10		10	µA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		30		30		30		30	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		5		5		5		5	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA, Vcc = 4.5		0.4		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA, Vcc = 4.5	2.4		2.4		2.4		2.4		V

NOTE: DC test conditions: VIH = VCC -0.3V, VIL = 0.3V

DATA RETENTION CHARACTERISTICS
(TA = -55°C TO +125°C)

Parameter	Symbol	Conditions	-70		-85		-100		-120		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Data Retention Supply Voltage	V_{DR}	$\overline{CS}$ ≥ V_{CC} -0.2V	2.0	5.5	2.0	5.5	2.0	5.5	2.0	5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		1		1		1		1	mA

AC CHARACTERISTICS
(VCC = 5.0V, TA = -55°C To +125°C)

Parameter Read Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		120		ns
Address Access Time	t_{AA}		70		85		100		120	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns
Chip Select Access Time	t_{ACS}		70		85		100		120	ns
Output Enable to Output Valid	t_{OE}		35		45		50		60	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	3		3		3		3		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		25		25		35		35	ns
Output Disable to Output in High Z	t_{OHZ}[1]		25		25		35		35	ns

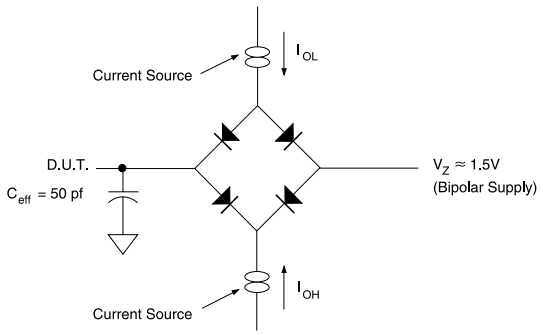
1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS
(VCC = 5.0V, TA = -55°C To +125°C)

Parameter Write Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		120		ns
Chip Select to End of Write	t_{CW}	60		75		80		100		ns
Address Valid to End of Write	t_{AW}	60		75		80		100		ns
Data Valid to End of Write	t_{DW}	30		35		40		50		ns
Write Pulse Width	t_{WP}	50		55		70		80		ns
Address Setup Time	t_{AS}	0		0		0		0		ns
Address Hold Time	t_{AH}	5		5		5		5		ns
Output Active from End of Write	t_{OW}[1]	5		5		5		5		ns
Write Enable to Output in High Z	t_{WHZ}[1]		25		30		35		35	ns
Data Hold Time	t_{DH}	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

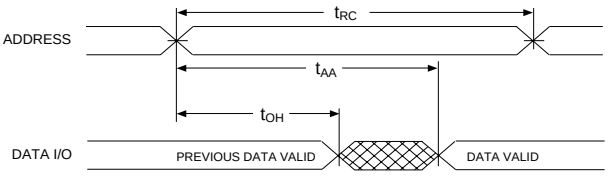


AC TEST CONDITIONS

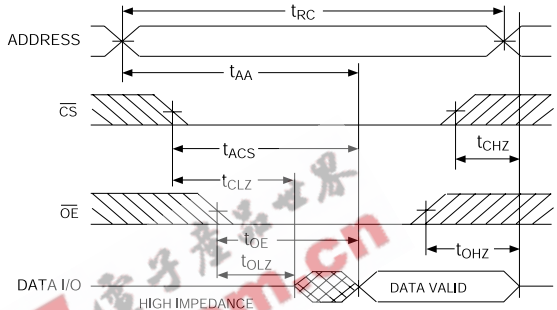
Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
VZ is programmable from -2V to +7V.
IOL & IOH programmable from 0 to 16mA.
Tester Impedance Z0 = 75Ω.
VZ is typically the midpoint of VOH and VOL.
IOL & IOH are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

TIMING WAVEFORM - READ CYCLE

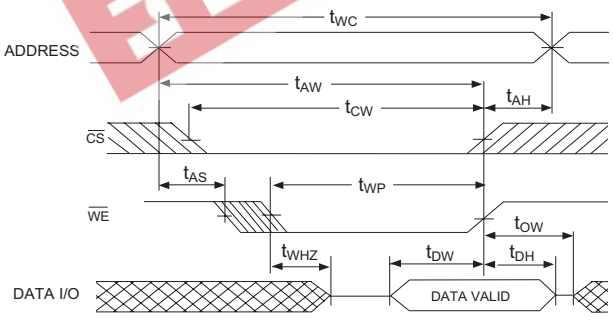


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



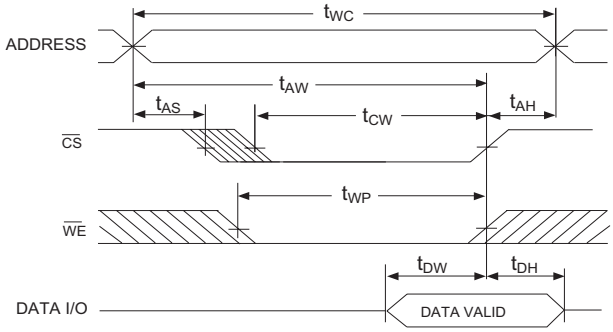
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

WRITE CYCLE - $\overline{WE}$ CONTROLLED



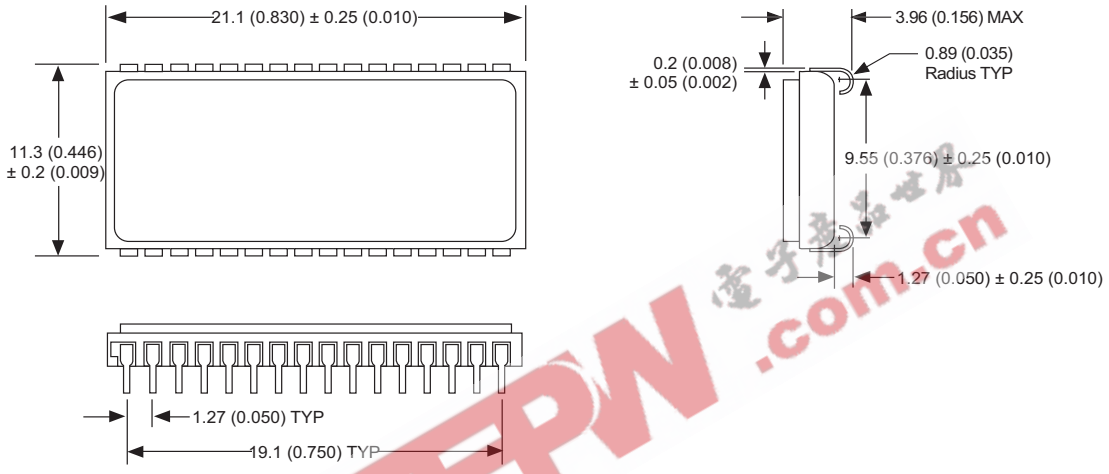
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

WRITE CYCLE - $\overline{CS}$ CONTROLLED



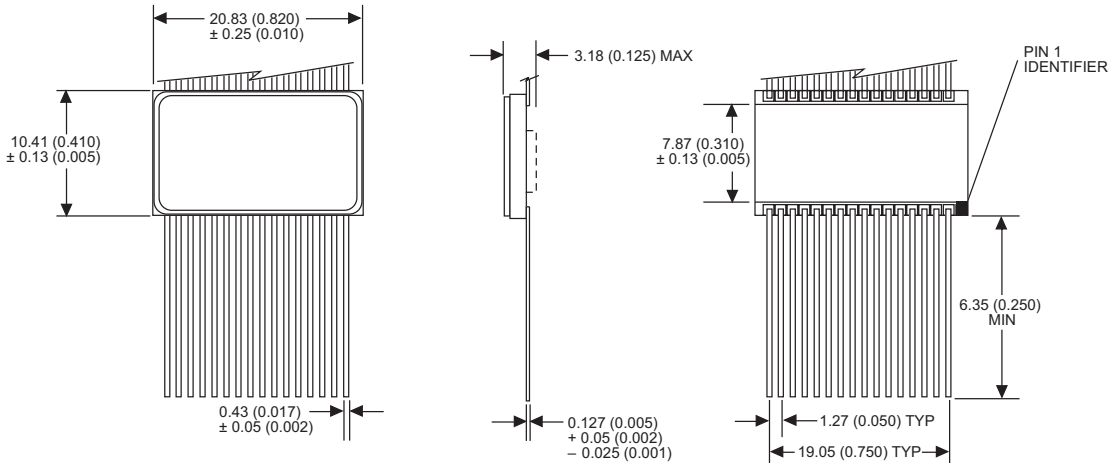
WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

PACKAGE 101: 32 LEAD, CERAMIC SOJ



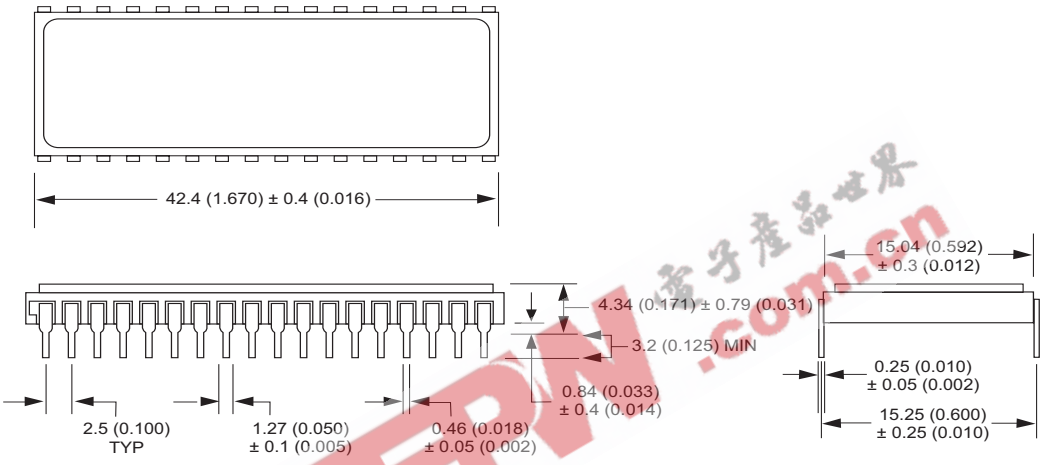
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 206: 32 LEAD, CERAMIC FLAT PACK



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

DATA RETENTION CHARACTERISTICS
(TA = -55°C TO +125°C)
LOW POWER VERSION ONLY

Parameter	Symbol	Conditions	Min	Max	Units
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geq V_{CC}$ -0.2V	2.0	5.5	V
Data Retention Current	I_{CCDR3}	V_{CC} = 2V		750	µA

ORDERING INFORMATION

W M S 128K 8 X - XXX X X X

LEAD FINISH:
Blank = Gold plated leads
A = Solder dip leads

DEVICE GRADE:
M = Military Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C

PACKAGE:
C = 32 Pin Ceramic .600" DIP (Package 300)
DE = 32 Lead Ceramic SOJ (Package 101) Evolutionary
DR = 32 Lead Ceramic SOJ (Package 101) Revolutionary
FE = 32 Lead Ceramic Flat Pack (Package 206)

ACCESS TIME (ns)

IMPROVEMENT MARK
L = Low Power for 2V Data Retention

ORGANIZATION, 128K x 8

SRAM

MONOLITHIC

WHITE ELECTRONIC DESIGNS CORP.

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DEVICE TYPE	SPEED	PACKAGE	SMD NO.
128K x 8 SRAM Monolithic	120ns	32 lead SOJ Revol (DR)	5962-96691 01HUX
128K x 8 SRAM Monolithic	100ns	32 lead SOJ Revol (DR)	5962-96691 02HUX
128K x 8 SRAM Monolithic	85ns	32 lead SOJ Revol (DR)	5962-96691 03HUX
128K x 8 SRAM Monolithic	70ns	32 lead SOJ Revol (DR)	5962-96691 04HUX
128K x 8 SRAM Monolithic	120ns	32 lead SOJ Evol (DE)	5962-96691 01HTX
128K x 8 SRAM Monolithic	100ns	32 lead SOJ Evol (DE)	5962-96691 02HTX
128K x 8 SRAM Monolithic	85ns	32 lead SOJ Evol (DE)	5962-96691 03HTX
128K x 8 SRAM Monolithic	70ns	32 lead SOJ Evol (DE)	5962-96691 04HTX
128K x 8 SRAM Monolithic	120ns	32 pin DIP (C)	5962-96691 01HYX
128K x 8 SRAM Monolithic	100ns	32 pin DIP (C)	5962-96691 02HYX
128K x 8 SRAM Monolithic	85ns	32 pin DIP (C)	5962-96691 03HYX
128K x 8 SRAM Monolithic	70ns	32 pin DIP (C)	5962-96691 04HYX
128K x 8 SRAM Monolithic	120ns	32 pin Flatpack (FE)	5962-96691 01HNX
128K x 8 SRAM Monolithic	100ns	32 pin Flatpack (FE)	5962-96691 02HNX
128K x 8 SRAM Monolithic	85ns	32 pin Flatpack (FE)	5962-96691 03HNX
128K x 8 SRAM Monolithic	70ns	32 pin Flatpack (FE)	5962-96691 04HNX

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