

## 24-Bit, 192kHz Stereo ADC

### DESCRIPTION

The WM8786 is a stereo audio ADC with differential inputs designed for high performance recordable media applications. Data is provided as a PCM output.

Stereo 24-bit multi-bit sigma-delta ADCs are used with digital audio output word lengths of 16 to 32 bits, and sampling rates from 8kHz to 192kHz. The device also has a high pass filter to remove residual DC offsets.

The device is hardware controlled. Pin programming provides access to all features including oversampling rate, audio format, powerdown, master/slave control and digital signal manipulation. The device is supplied in a 20-lead SSOP package.

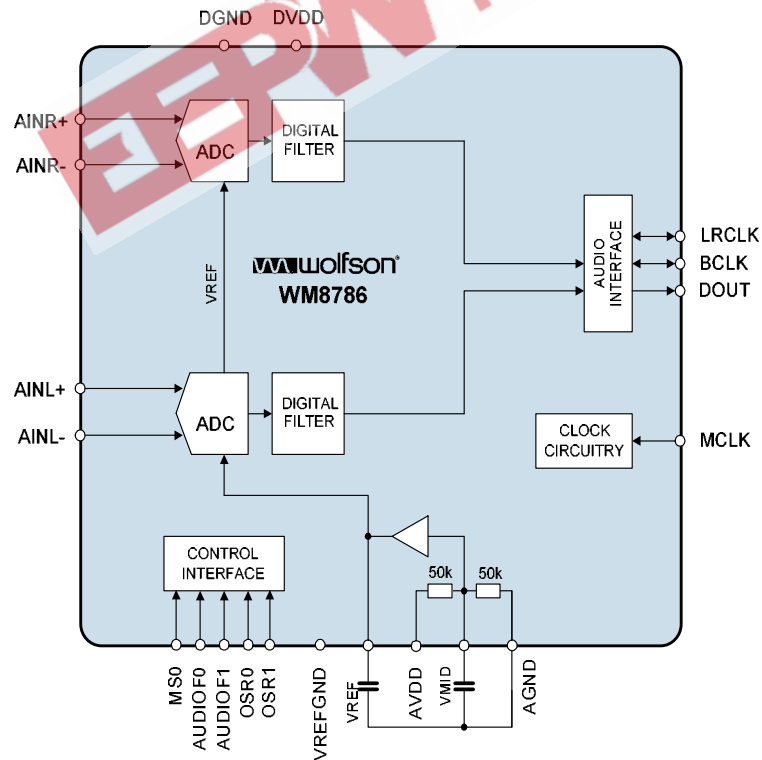
### FEATURES

- SNR 111dB ('A' weighted @ 48kHz)
- THD -102dB (at -0.1dB)
- Sampling Frequency: 8 – 192kHz
- Hardware Control Interface
- Master or Slave Clocking Mode
- Programmable Audio Data Interface Modes
  - I<sup>2</sup>S, Left, Right Justified or DSP
  - 24-Bit Word Length
- Supply Voltages
  - Analogue 4.5 to 5.5V
  - Digital core: 2.7V to 3.6V
- 20-lead SSOP package

### APPLICATIONS

- Recordable DVD Players
- Personal Video Recorders
- High End Sound Cards
- Studio Audio Processing Equipment

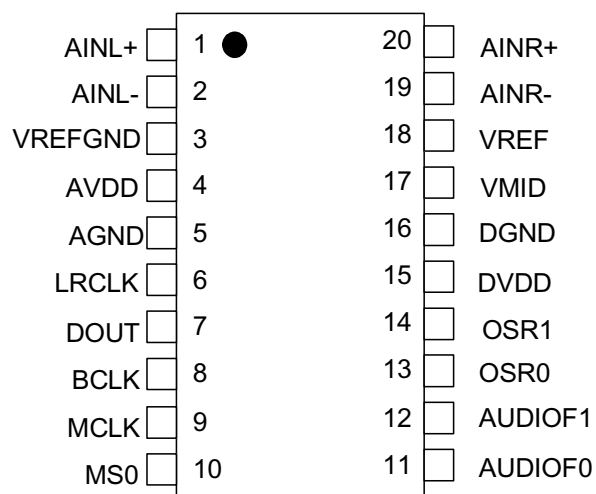
### BLOCK DIAGRAM



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## PIN CONFIGURATION



## ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8786GEDS/V	-25°C to +85°C	20-pin SSOP (Pb-free)	MSL3	260°C
WM8786GEDS/RV	-25°C to +85°C	20-pin SSOP, (Pb-free, tape and reel)	MSL3	260°C

**Note:**

Reel quantity = 2,000

## PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	AINL+	Analogue Input	Left Channel Positive Input
2	AINL-	Analogue Input	Left Channel Negative Input
3	VREFGND	Analogue Reference	Negative Reference Connection
4	AVDD	Supply	Analogue Supply
5	AGND	Supply	Analogue Ground (return path for AVDD)
6	LRCLK	Digital Input / Output	Audio Interface Left / Right Clock
7	DOUT	Digital Output	ADC Digital Audio Data
8	BCLK	Digital Input / Output	Audio Interface Bit Clock
9	MCLK	Digital Input	Master Clock
10	MS0 (pull down pad)	Digital Input	Master/Slave Control 0 = Slave Mode Audio Interface 1 = Master Mode Audio Interface @ 256fs (or @128fs in quad rate)
11	AUDIOF0	Digital Input	Audio Format Selection 00 = 24 bit right justified audio data format 01 = 24 bit left audio data format 10 = I <sup>2</sup> S audio data format 11 = DSP audio data format
12	AUDIOF1	Digital Input	
13	OSR0 (pull down pad)	Digital Input	Oversampling Rate Control 00 = Single rate (48kHz) 01 = Dual rate (96kHz) 10 = Quad rate (192kHz) 11 = Not valid
14	OSR1	Digital Input	
15	DVDD	Supply	Digital Supply
16	DGND	Supply	Digital Ground (return path for DVDD)
17	VMID	Analogue Output	Midrail Voltage Decoupling Capacitor
18	VREF	Analogue Reference	Reference Voltage Decoupling Capacitor
19	AINR-	Analogue Input	Right Channel Negative Input
20	AINR+	Analogue Input	Right Channel Positive Input

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+3.63V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs	DGND -0.3V	DVDD + 0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Master Clock Frequency		40MHz
Operating temperature range, T <sub>A</sub>	-25°C	+85°C
Storage temperature after soldering	-65°C	+150°C

### Notes

1. Analogue and digital grounds must always be within 0.3V of each other.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		2.7		3.6	V
Analogue supply range	AVDD		4.5		5.5	V
Ground	DGND,AGND			0		V

## ELECTRICAL CHARACTERISTICS

## Test Conditions

DVDD = 3.3V, AVDD = 5.0V,  $T_A = +25^\circ\text{C}$ , 1kHz signal, A-weighted,  $f_s = 48\text{kHz}$ , MCLK = 256fs, 24-bit audio data, Slave Mode unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ADC Performance</b>						
Full Scale Input Signal Level (for ADC 0dB Input)				2.0		$V_{\text{rms}}$
Input resistance				10		k $\Omega$
Input capacitance				10		pF
Signal to Noise Ratio (Note 1,2,4)	SNR	A-weighted, @ $f_s = 48\text{kHz}$	104	111		dB
		Unweighted, @ $f_s = 48\text{kHz}$		108		dB
Signal to Noise Ratio (Note 1,2,4)	SNR	A-weighted, @ $f_s = 96\text{kHz}$		111		dB
		Unweighted, @ $f_s = 96\text{kHz}$		108		dB
Signal to Noise Ratio (Note 1,2,4)	SNR	A-weighted, @ $f_s = 192\text{kHz}$		111		dB
		Unweighted, @ $f_s = 192\text{kHz}$		108		dB
Total Harmonic Distortion	THD	1kHz, -0.1dB Full Scale @ $f_s = 48\text{kHz}$		-102		dB
		1kHz, -0.1dB Full Scale @ $f_s = 96\text{kHz}$		-102		dB
		1kHz, -0.1dB Full Scale @ $f_s = 192\text{kHz}$		-102		dB
Total Harmonic Distortion	THD	1kHz, -0.1dB Full Scale @ $f_s = 48\text{kHz}$		0.0008		%
		1kHz, -0.1dB Full Scale @ $f_s = 96\text{kHz}$		0.0008		%
		1kHz, -0.1dB Full Scale @ $f_s = 192\text{kHz}$		0.0008		%
Dynamic Range	DNR	-60dBFS	104	111		dB
Channel Level Matching		20kHz signal		0.1		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp, applied to AVDD, DVDD		50		dB
		20Hz to 20kHz 100mVpp		45		dB
<b>Digital Logic Levels (CMOS Levels)</b>						
Input LOW level	$V_{\text{IL}}$				0.3 x DVDD	V
Input HIGH level	$V_{\text{IH}}$		0.7 x DVDD			V
Input leakage current			-1	$\pm 0.2$	+1	$\mu\text{A}$
Input capacitance				5		pF
Output LOW	$V_{\text{OL}}$	$I_{\text{OL}}=1\text{mA}$			0.1 x DVDD	V
Output HIGH	$V_{\text{OH}}$	$I_{\text{OH}}=-1\text{mA}$	0.9 x DVDD			V
<b>Analogue Reference Levels</b>						
Midrail Reference Voltage	VMID	AVDD to VMID and VMID to VREFGND	-3%	AVDD/2	+3%	V
Potential Divider Resistance	$R_{\text{VMID}}$	AVDD to VMID and VMID to GND		50		k $\Omega$
Buffered Reference Voltage	VREF		-3%	0.8 x AVDD	+3%	V

**Test Conditions**

DVDD = 3.3V, AVDD = 5.0V, T<sub>A</sub> = +25°C, 1kHz signal, A-weighted, fs = 48kHz, MCLK = 256fs, 24-bit audio data, Slave Mode unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Supply Current</b>						
Analogue supply current				27		mA
Digital supply current				5		mA
Power Down				22		uA

**Note:**

1. VMID is decoupled with 10uF and 0.1uF capacitors close to the device package. Smaller capacitors may reduce performance.

**TERMINOLOGY**

1. Signal-to-noise ratio (dB) – Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, over a 20Hz to 20kHz bandwidth. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
5. All performance measurements are done with a 20kHz low pass filter, and where noted an A-weight filter, except where noted. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although this is not audible, it may affect dynamic specification values.

## SIGNAL TIMING REQUIREMENTS

### SYSTEM CLOCK TIMING

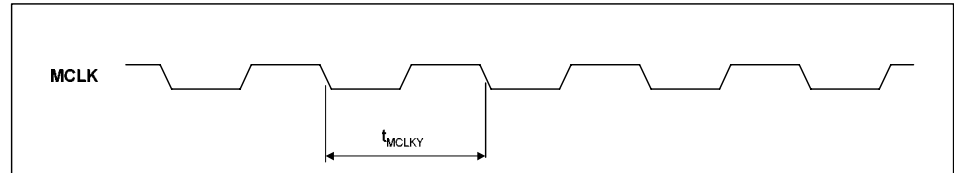


Figure 1 System Clock Timing Requirements

#### Test Conditions

DVDD = 3.3V, DGND = 0V,  $T_A = +25^\circ\text{C}$ , Slave Mode,  $f_s = 48\text{kHz}$ , MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
<b>System Clock Timing Information</b>					
MCLK System clock cycle time	$T_{MCLKY}$	25			ns
MCLK duty cycle	$T_{MCLKDS}$	60:40		40:60	

### AUDIO INTERFACE TIMING – MASTER MODE, PCM DATA

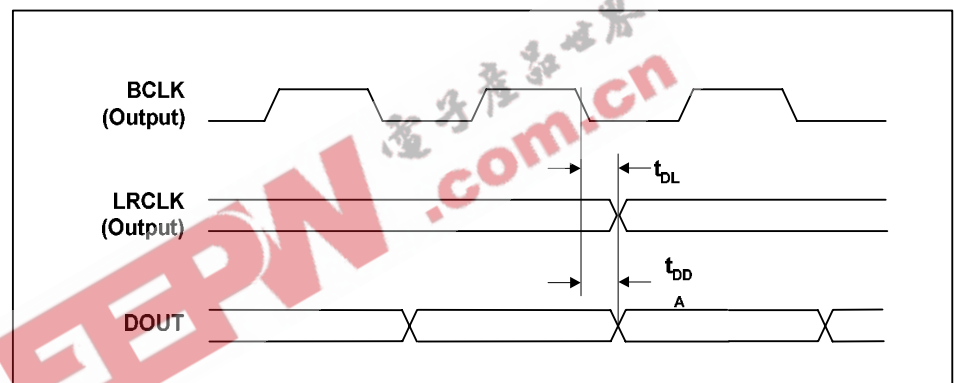


Figure 2 Digital Audio Data Timing – Master Mode (see Control Interface)

#### Test Conditions

DVDD = 3.3V, DGND = 0V,  $T_A = +25^\circ\text{C}$ , Master Mode,  $f_s = 48\text{kHz}$ , MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
<b>Audio Data Input Timing Information</b>					
LRCLK propagation delay from BCLK falling edge	$t_{DL}$	0		10	ns
DOUT propagation delay from BCLK falling edge	$t_{DDA}$	0		11	ns



## AUDIO INTERFACE TIMING – SLAVE MODE, PCM DATA

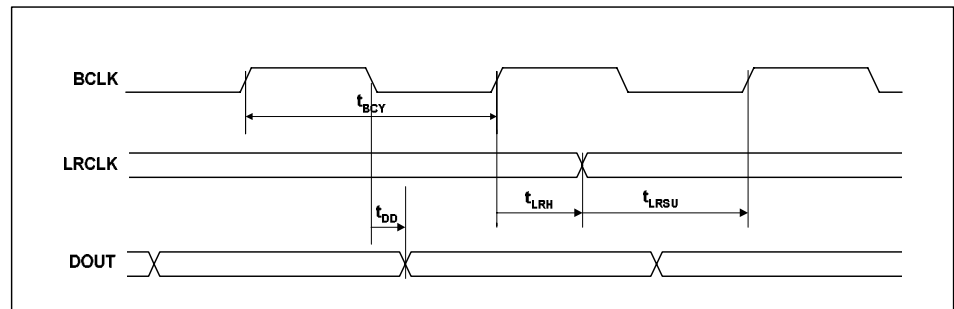


Figure 3 Digital Audio Data Timing – Slave Mode

## Test Conditions

DVDD = 3.3V, DGND = 0V,  $T_A = +25^\circ\text{C}$ , Slave Mode,  $f_s = 48\text{kHz}$ ,  $\text{MCLK} = 256\text{fs}$ , 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
<b>Audio Data Input Timing Information</b>					
BCLK cycle time	$t_{\text{BCY}}$	25			ns
LRCLK set-up time to BCLK rising edge	$t_{\text{LRSU}}$	10			ns
LRCLK hold time from BCLK rising edge	$t_{\text{LRH}}$	10			ns
DOUT propagation delay from BCLK falling edge	$t_{\text{DD}}$	0		11	ns

**POWER-ON RESET**

The WM8786 has an internal power-on reset circuit. The reset sequence is entered at power-on or power-up (DVDD). Until the internal reset is removed, DOUT is forced to zero. DOUT remains zero for a count equal to 32 sample clocks, after power up. (This count is driven by MCLK and is independent of any external LRCLK).

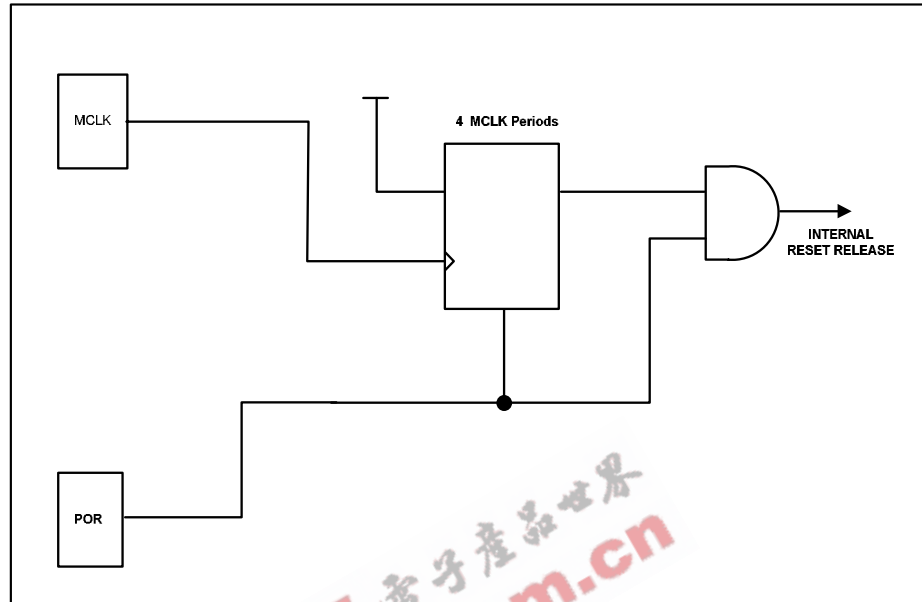


Figure 4 POR Circuit

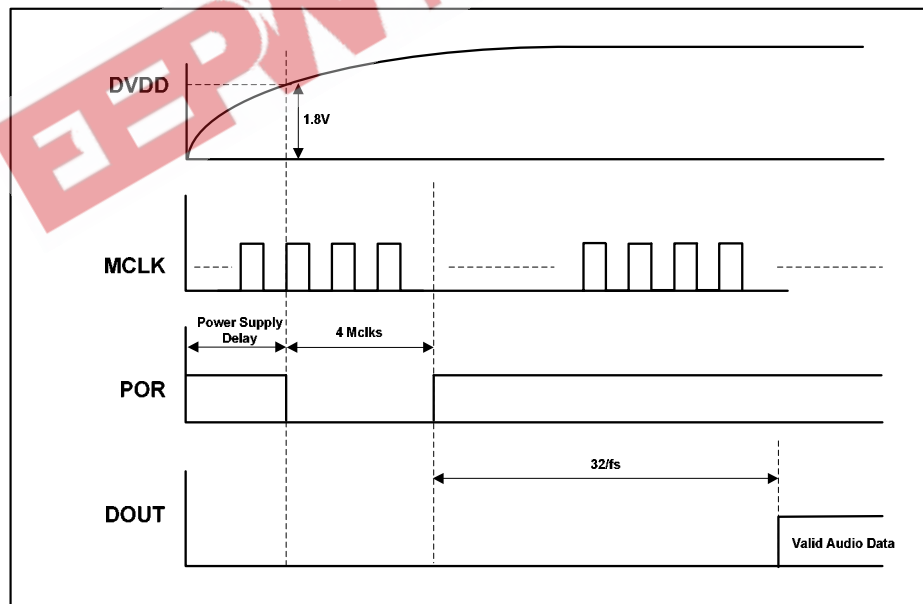


Figure 5 POR Timing

## DIGITAL FILTER CHARACTERISTICS

The WM8786 digital filter characteristics scale with sample rate.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ADC Sample Rate (Single Rate - 48kHz typically)</b>					
Passband	+/- 0.005dB	0		0.454fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.005	dB
Stopband		0.546fs			
Stopband Attenuation	f > 0.546fs	-85			dB
Group Delay			32/fs		s
<b>ADC Sample Rate (Dual Rate - 96kHz typically)</b>					
Passband	+/- 0.005dB	0		0.454fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.005	dB
Stopband		0.546fs			
Stopband Attenuation	f > 0.546fs	-85			dB
Group Delay			32/fs		s
<b>ADC Sample Rate (Quad Rate - 192kHz typically)</b>					
Passband	+/- 0.005dB	0		0.25fs	
	-3dB		0.45fs		
	-6dB		0.5fs		
Passband Ripple				+/- 0.005	dB
Stopband		0.75fs			
Stopband Attenuation	f > 0.75fs	-85			dB
Group Delay			10/fs		s
High Pass Filter Corner Frequency	-3dB		3.7		Hz
	-0.5dB		10.4		
	-0.1dB		21.6		

Table 1 Digital Filter Characteristics

## TERMINOLOGY

1. Stop Band Attenuation (dB) - the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

**FILTER RESPONSES**

**SINGLE RATE 48k**

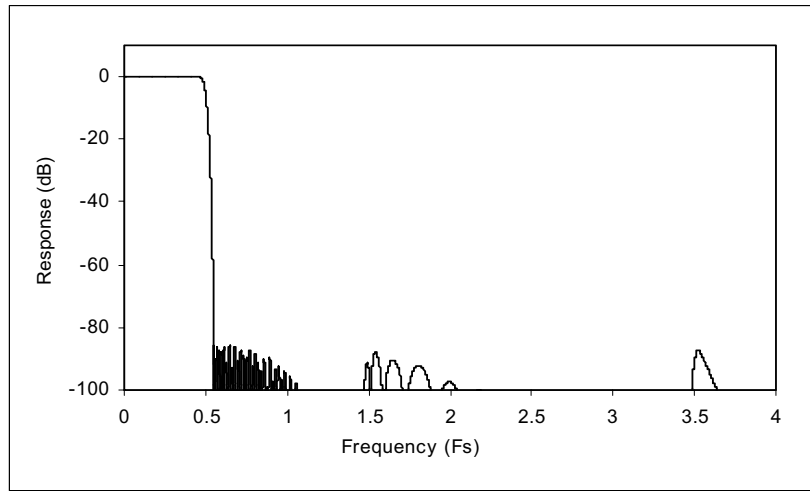


Figure 6 Single Rate 48k Filter Response

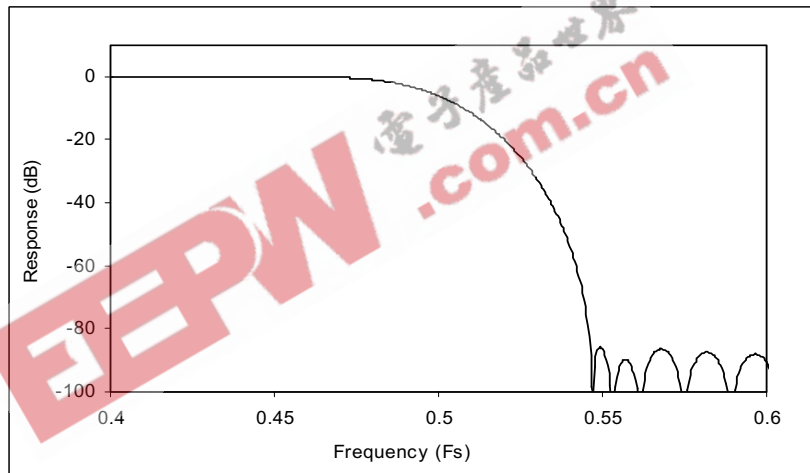


Figure 7 Single Rate 48k Filter Response

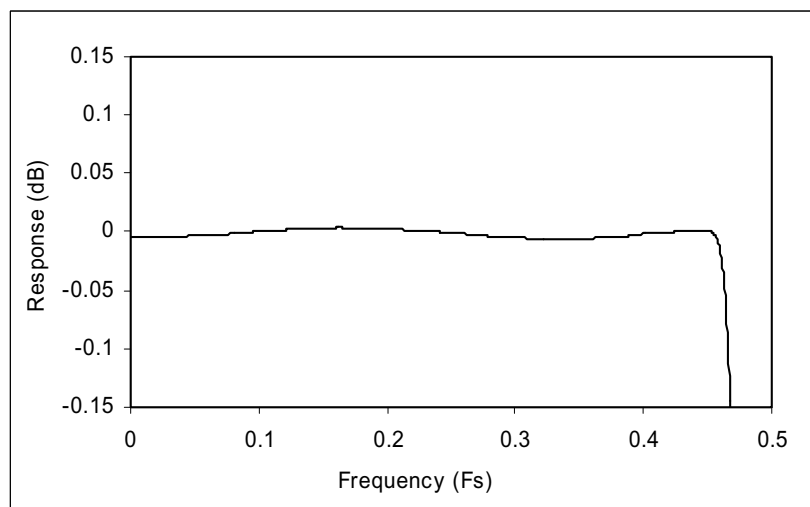


Figure 8 Single Rate 48k Filter Response

DUAL RATE 96k

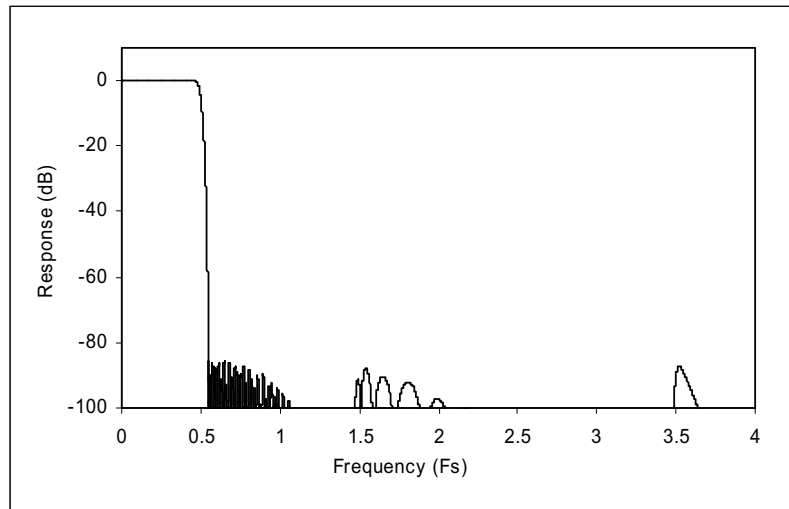


Figure 9 Dual Rate 96k Filter Response

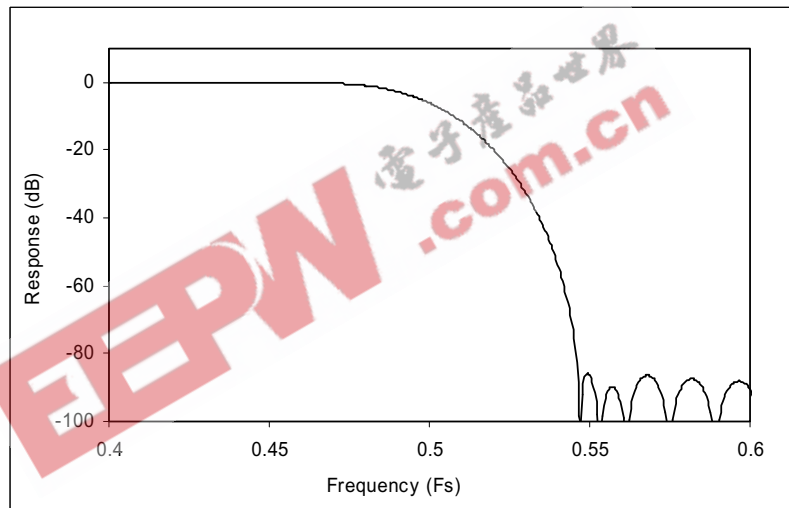


Figure 10 Dual Rate 96k Filter Response

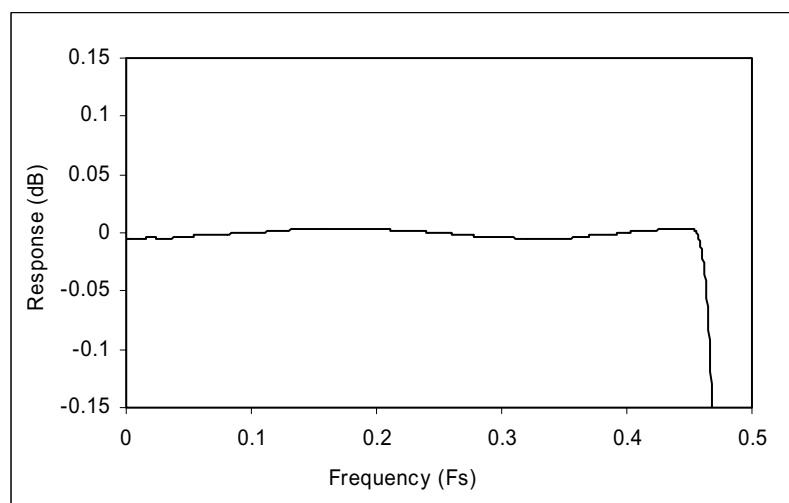


Figure 11 Dual Rate 96k Filter Response

QUAD RATE 192k

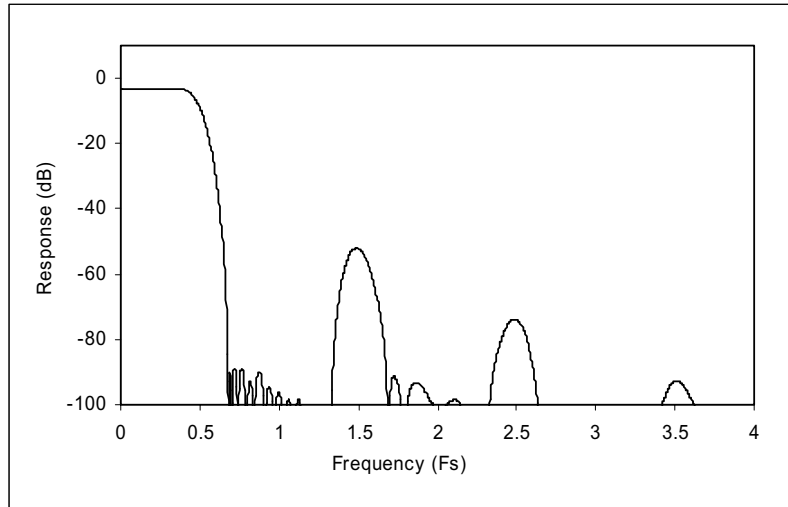


Figure 12 Quad Rate 192k Filter Response

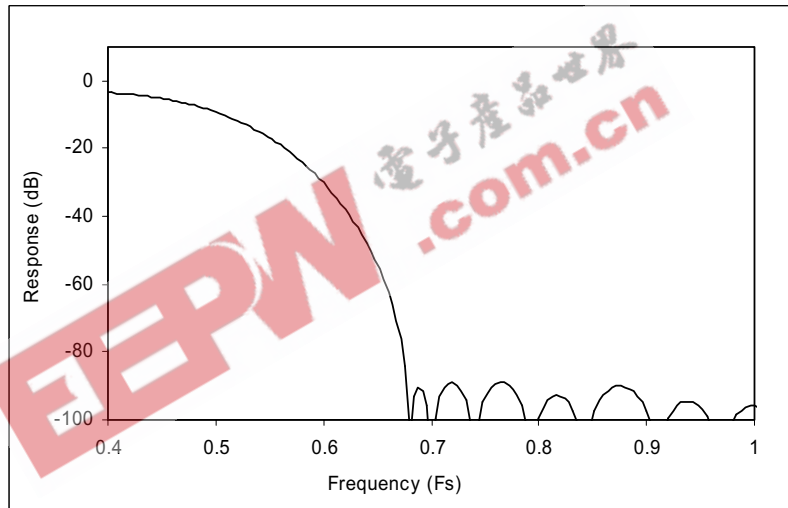


Figure 13 Quad Rate 192k Filter Response

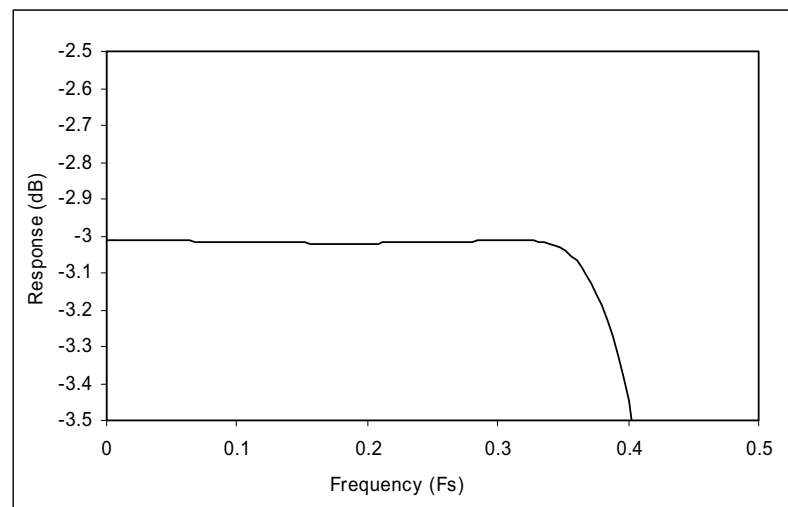


Figure 14 Quad Rate 192k Filter Response

## DEVICE DESCRIPTION

### INTRODUCTION

The WM8786 is a high performance stereo audio ADC designed for demanding recording applications such as DVD recorders, studio mixers, PVRs, and AV amplifiers. The WM8786 consists of stereo line level inputs, followed by a sigma-delta modulator and digital filtering.

The WM8786 uses a multi-bit high-order oversampling architecture delivering high SNR operating at oversampling ratios from 128fs to 32fs according to the sample rate. Sample rates from 8kHz to 192kHz are supported. The WM8786 supports master clock rates from 128fs to 768fs.

The digital filter is a high performance linear phase FIR filter. The digital filters are optimised for each sample rate. Also included is a high pass filter to remove residual DC offsets from the input signal.

The output from the ADC is available on a configurable digital audio interface. It supports a number of audio data formats including I<sup>2</sup>S, Left justified and Right justified or DSP, and can operate in master or slave modes.

The WM8786 functionality is controlled in hardware via specific pins. It is fully compatible and an ideal partner for a range of industry standard microprocessors, controllers and DSPs.

The WM8786 can be powered down to reduce system power consumption.

### DIGITAL AUDIO INTERFACE

The digital audio interface uses three pins:

- DOUT: ADC data output
- LRCLK: ADC data alignment clock
- BCLK: Bit clock, for synchronisation

The digital audio interface takes the data from the internal ADC digital filters and places it on DOUT and LRCLK. DOUT is the formatted digital audio data stream output from the ADC digital filters with left and right channels multiplexed together. LRCLK is an alignment clock that controls whether Left or Right channel data is present on the DOUT line. DOUT and LRCLK are synchronous with the BCLK signal with each data bit transition signified by a BCLK high to low transition. DOUT is always an output. BCLK and LRCLK may be inputs or outputs depending whether the device is in Master or Slave mode. (see Master and Slave Mode Operation, below).

Four different audio data formats are supported:

- Left justified
- Right justified
- I<sup>2</sup>S
- DSP

They are described in Audio Data Formats, below. Refer to the Electrical Characteristic section for timing information.

### MASTER AND SLAVE MODE OPERATION

The WM8786 can be configured as either a master or slave mode device. As a master device the WM8786 generates BCLK and LRCLK and thus controls sequencing of the data transfer on DOUT. In slave mode, the WM8786 responds with data to clocks it receives over the digital audio interface. The mode can be selected using the MS0 pin. Master and slave modes are illustrated below.

MS0 PIN STATUS	INTERFACE FORMAT
Low	Slave
High	Master (@256fs in oversampling ratio = single or dual rate)
High	Master (@192fs in oversampling ratio = quad rate)

Table 2 Control Interface Mode Selection

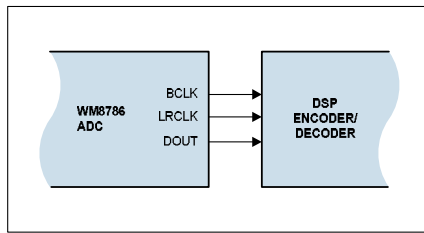


Figure 15a Master Mode

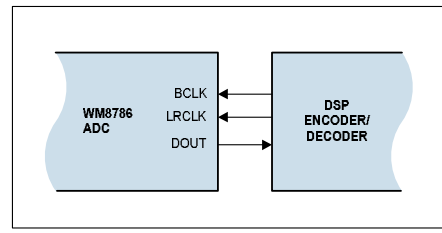


Figure 15b Slave Mode

**AUDIO DATA FORMATS**

In Left Justified mode, the MSB is available on the first rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

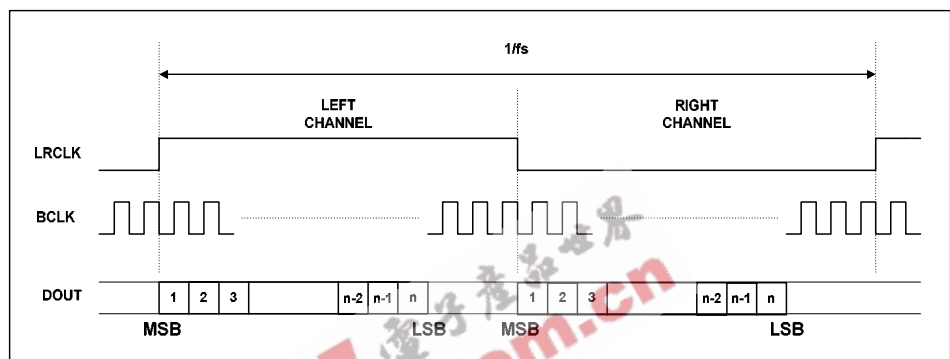


Figure 16 Left Justified Audio Interface (assuming n-bit word length)

In Right Justified mode, the LSB is available on the last rising edge of BCLK before an LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.

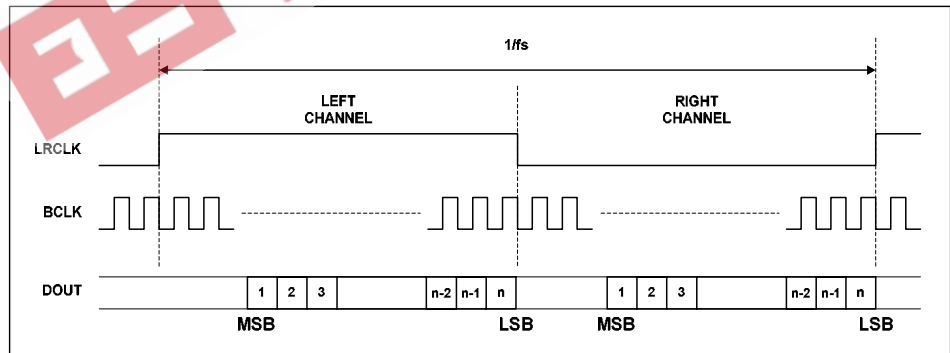


Figure 17 Right Justified Audio Interface (assuming n-bit word length)



In I<sup>2</sup>S mode, the MSB is available on the second rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

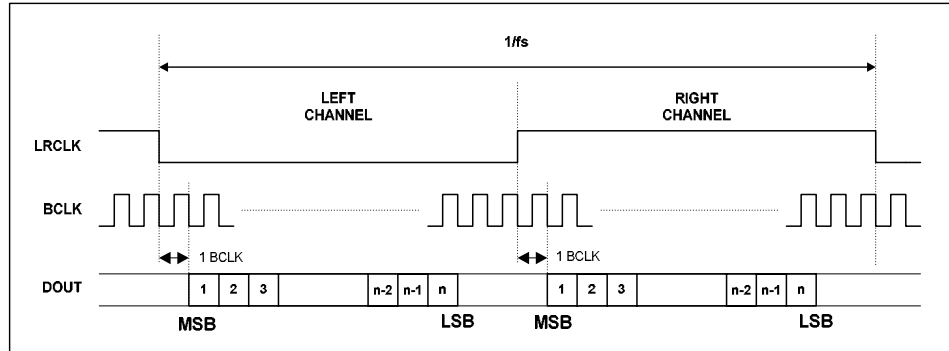


Figure 18 I<sup>2</sup>S Justified Audio Interface (assuming n-bit word length)

In DSP/PCM mode, the left channel MSB is available on the 2<sup>nd</sup> rising edge of BCLK following a rising edge of LRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRC output will resemble the frame pulse shown in Figure 19. In device slave mode, Figure 20 it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

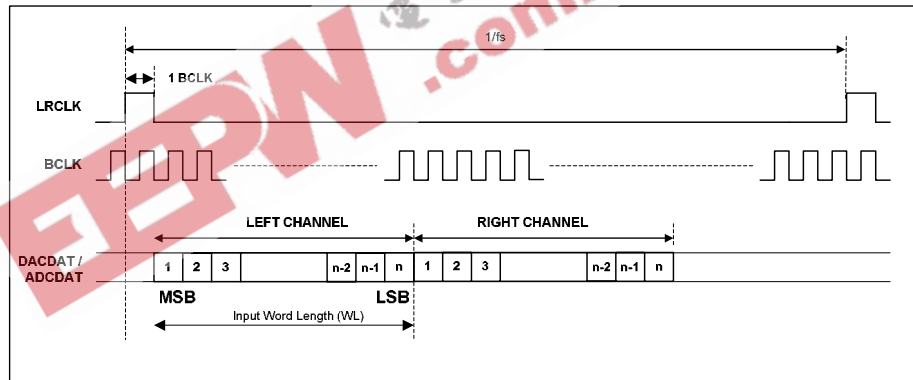


Figure 19 DSP/PCM Mode Audio Interface (mode A, Master)

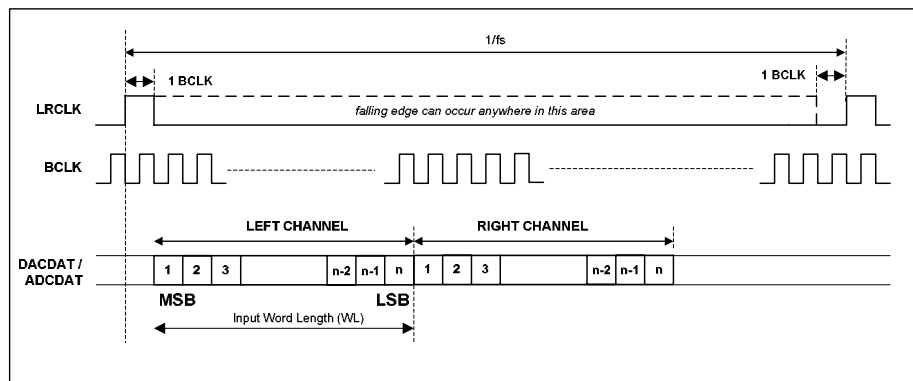


Figure 20 DSP/PCM Mode Audio Interface (mode A, Slave)

## AUDIO INTERFACE CONTROL

### AUDIO INTERFACE CONTROL

The audio interface is controlled using the AUDIOF0 and AUDIOF1 pins. Dynamically changing the audio format may cause erroneous operation of the interfaces and is therefore not recommended.

All ADC data is signed 2's complement. The length of the digital audio data is always 24 bits.

AUDIOF1 PIN STATUS	AUDIOF0 PIN STATUS	AUDIO INTERFACE FORMAT
Low	Low	24-bit right justified
Low	High	24-bit left justified
High	Low	24-bit I <sup>2</sup> S
High	High	24-bit DSP

Table 3 Audio Interface Format Selection

## OVERSAMPLING RATIOS AND SIGMA-DELTA MODULATOR FREQUENCY

For correct operation of the device and optimal performance, the user must select the appropriate ADC modulator oversampling ratio. The oversampling ratio is selected using the OSR0 and OSR1 pins.

OSR1 PIN STATUS	OSR0 PIN STATUS	OVERSAMPLING RATIO CONTROL
Low	Low	Single Rate (128fs)
Low	High	Dual Rate (64fs)
High	Low	Quad Rate (32fs)
High	High	Not Valid

Table 4 Oversampling Ratio Selection

The WM8786 can operate at sample rates from 8kHz to 192kHz. The WM8786 uses a sigma-delta modulator that operates at frequencies between 1.024MHz and 6.144MHz

SAMPLING RATE (LRCLK)	OVERSAMPLING RATIO	SIGMA-DELTA MODULATOR FREQUENCY (MHZ)
8kHz	Single Rate (128fs)	1.024
32kHz	Single Rate (128fs)	4.096
44.1kHz	Single Rate (128fs)	5.6448
48kHz	Single Rate (128fs)	6.144
96kHz	Dual Rate (64fs)	6.144
192kHz	Quad Rate (32fs)	6.144

Table 5 Sigma-delta Modulator Frequency

## MASTER CLOCK AND AUDIO SAMPLE RATES

The master clock (MCLK) is used to operate the digital filters and the noise shaping circuits. The WM8786 supports a wide range of master clock frequencies, and can generate many commonly used audio sample rates directly from the master clock. The following tables show the recommended Master clock frequencies for different sample rates.

In Master Mode, with oversampling ratio = single rate or dual rate, Master clock frequency of 256 is supported.

SAMPLING RATE (LRCLK)	OVERSAMPLING RATIO	MASTER CLOCK FREQUENCY (MHz)
		256fs
32kHz	Single Rate	8.192
44.1kHz	Single Rate	11.2896
48kHz	Single Rate	12.288
96kHz	Dual Rate	24.576

**Table 6 Master Mode: Recommended Master Clock Frequency Selection**

In Master Mode, with oversampling ratio = quad rate, Master clock frequency of 192 is supported.

SAMPLING RATE (LRCLK)	OVERSAMPLING RATIO	MASTER CLOCK FREQUENCY (MHz)
		128fs
192kHz	Quad Rate	24.576

**Table 7 Master Mode: Recommended Master Clock Frequency Selection**

In Slave Mode, Master clock frequencies of 128fs, 192fs, 256fs, 384fs, 512fs and 768fs are supported. The WM8786 automatically detects the audio sample rate, in slave mode.

SAMPLING RATE (LRCLK)	OVERSAMPLING RATIO	MASTER CLOCK FREQUENCY (MHz)					
		128fs	192fs	256fs	384fs	512fs	768fs
32kHz	Single Rate	-	-	8.192	12.288	16.384	24.576
44.1kHz	Single Rate	-	-	11.2896	16.9344	22.5792	33.8688
48kHz	Single Rate	-	-	12.288	18.432	24.576	36.864
96kHz	Dual Rate	-	-	24.576	36.864	-	-
192kHz	Quad Rate	24.576	36.864	-	-	-	-

**Table 8 Slave Mode: Recommended Master Clock Frequency Selection**

## MLCK AND LRCLK PHASE RELATIONSHIP

The WM8786 does not require a specific phase relationship between MLCK and LRCLK. If the relationship between MCLK and LRCLK changes by more than +/-8 BCLKs in a 64 BCLK frame, the WM8786 will attempt to re-synchronise. During re-synchronisation, data samples may be dropped or duplicated.

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

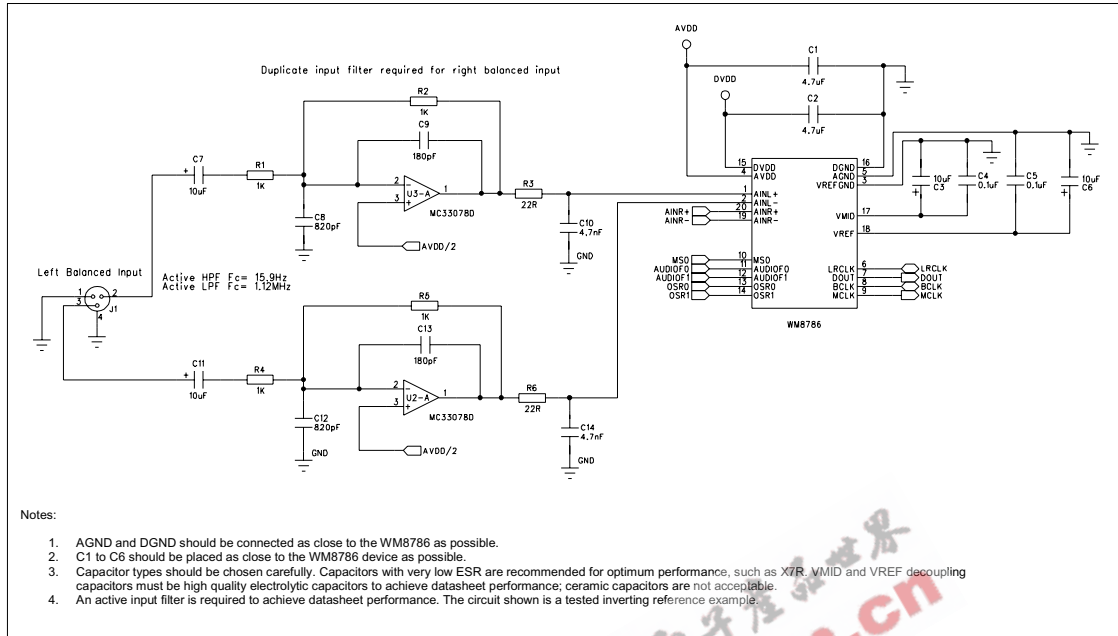
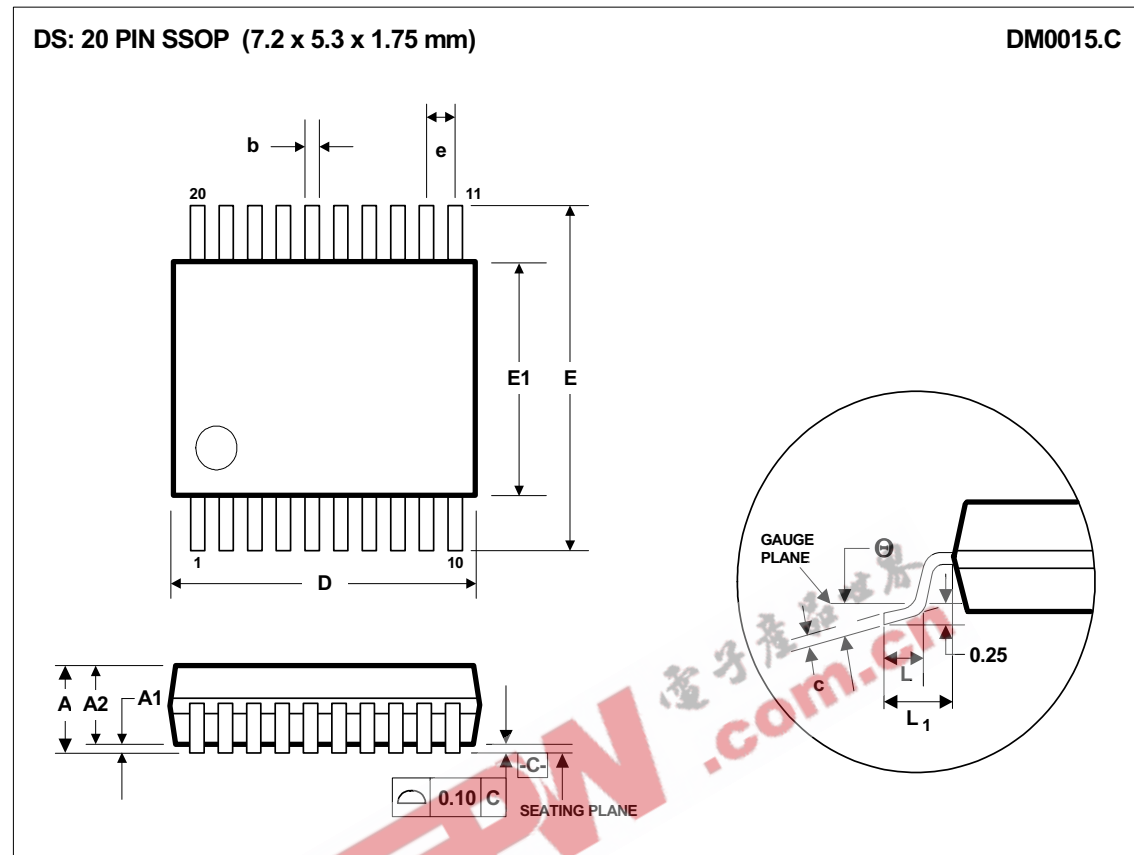


Figure 21 External Component Diagram

## PACKAGE DIMENSIONS



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	----	----	2.0
A <sub>1</sub>	0.05	----	----
A <sub>2</sub>	1.65	1.75	1.85
b	0.22	0.30	0.38
c	0.09	----	0.25
D	6.90	7.20	7.50
e	0.65 BSC		
E	7.40	7.80	8.20
E <sub>1</sub>	5.00	5.30	5.60
L	0.55	0.75	0.95
L <sub>1</sub>	1.25 REF		
θ	0°	4°	8°
REF:	JEDEC.95, MO-150		

## NOTES:

- A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.  
 B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.  
 C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.  
 D. MEETS JEDEC.95 MO-150, VARIATION = AE. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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