



512Kx8 MONOLITHIC SRAM

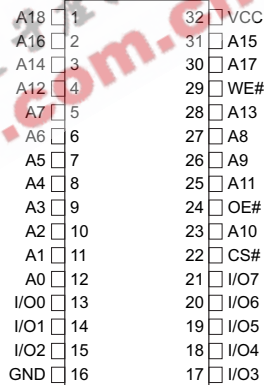
FEATURES

- Access Times 70, 85, 100, 120ns
- MIL-STD-883 Compliant Devices Available
- Low Voltage Operation
- Evolutionary, Corner Power/Ground Pinout JEDEC Approved
 - 32 pin Ceramic DIP (Package 300)
 - 32 lead Ceramic SOJ (Package 101)
- Commercial, Industrial and Military Temperature Ranges
- Low Power CMOS
- Low Voltage Operation
 - 3.3V ± 10% Power Supply
- Low Power Data Retention
- TTL Compatible Inputs and Outputs

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

EVOLUTIONARY PINOUT

32 DIP
32 CSOJ (DE)
TOP VIEW



PIN DESCRIPTION

| | |
|-----------------|--------------------|
| A0-18 | Address Inputs |
| I/O0-7 | Data Input/Output |
| CS# | Chip Select |
| OE# | Output Enable |
| WE# | Write Enable |
| V _{CC} | +3.3V Power Supply |
| GND | Ground |



ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min | Max | Unit |
|--------------------------------|------------------|------|----------------------|------|
| Operating Temperature | T _A | -55 | +125 | °C |
| Storage Temperature | T _{STG} | -65 | +150 | °C |
| Signal Voltage Relative to GND | V _G | -0.5 | V _{CC} +0.5 | V |
| Junction Temperature | T _J | | 150 | °C |
| Supply Voltage | V _{CC} | -0.5 | 7.0 | V |

TRUTH TABLE

| CS# | OE# | WE# | Mode | Data I/O | Power |
|-----|-----|-----|-------------|----------|---------|
| H | X | X | Standby | High Z | Standby |
| L | L | H | Read | Data Out | Active |
| L | X | L | Write | Data In | Active |
| L | H | H | Out Disable | High Z | Active |

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|------------------------|-----------------|------|-----------------------|------|
| Supply Voltage | V _{CC} | 3.0 | 3.6 | V |
| Input High Voltage | V _{IH} | 2.2 | V _{CC} + 0.3 | V |
| Input Low Voltage | V _{IL} | -0.3 | +0.8 | V |
| Operating Temp. (Mil.) | T _A | -55 | +125 | °C |

CAPACITANCE

T_A = +25°C

| Parameter | Symbol | Condition | Max | Unit |
|--------------------|------------------|-----------------------------------|-----|------|
| Input capacitance | C _{IN} | V _{IN} = 0V, f = 1.0MHz | 12 | pF |
| Output capacitance | C _{OUT} | V _{OUT} = 0V, f = 1.0MHz | 12 | pF |

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, -55°C ≤ T_A ≤ +125°C

| Parameter | Symbol | Conditions | Min | Max | Units |
|--------------------------|-----------------|---|-----|-----|-------|
| Input Leakage Current | I _{LI} | V _{CC} = 3.6, V _{IN} = GND to V _{CC} | | 10 | μA |
| Output Leakage Current | I _{LO} | CS# = V _{IH} , OE# = V _{IH} , V _{OUT} = GND to V _{CC} | | 10 | μA |
| Operating Supply Current | I _{CC} | CS# = V _{IL} , OE# = V _{IH} , f = 5MHz, V _{CC} = 3.6 | | 25 | mA |
| Standby Current | I _{SB} | CS# = V _{IH} , OE# = V _{IH} , f = 5MHz, V _{CC} = 3.6 | | 400 | μA |
| Output Low Voltage | V _{OL} | I _{OL} = 2.1mA, V _{CC} = 3.0 | | 0.4 | V |
| Output High Voltage | V _{OH} | I _{OH} = -1.0mA, V _{CC} = 3.0 | 2.4 | | V |

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V



AC CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, -55°C ≤ T_A ≤ +125°C

| Parameter | Symbol | -70 | | -85 | | -100 | | -120 | | Units |
|------------------------------------|-------------------------------|-----|-----|-----|-----|------|-----|------|-----|-------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | t _{RC} | 70 | | 85 | | 100 | | 120 | | ns |
| Address Access Time | t _{AA} | | 70 | | 85 | | 100 | | 120 | ns |
| Output Hold from Address Change | t _{OH} | 5 | | 5 | | 5 | | 5 | | ns |
| Chip Select Access Time | t _{ACS} | | 70 | | 85 | | 100 | | 120 | ns |
| Output Enable to Output Valid | t _{OE} | | 35 | | 40 | | 50 | | 60 | ns |
| Chip Select to Output in Low Z | t _{CLZ} ¹ | 10 | | 10 | | 10 | | 10 | | ns |
| Output Enable to Output in Low Z | t _{OLZ} ¹ | 5 | | 5 | | 5 | | 5 | | ns |
| Chip Disable to Output in High Z | t _{CHZ} ¹ | | 25 | | 25 | | 35 | | 35 | ns |
| Output Disable to Output in High Z | t _{OHZ} ¹ | | 25 | | 25 | | 35 | | 35 | ns |

1. This parameter is guaranteed by design but not tested.

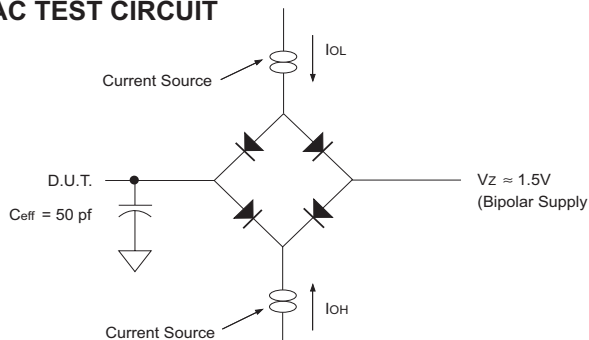
AC CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, -55°C ≤ T_A ≤ +125°C

| Parameter | Symbol | -70 | | -85 | | -100 | | -120 | | Units |
|----------------------------------|-------------------------------|-----|-----|-----|-----|------|-----|------|-----|-------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | t _{WC} | 70 | | 85 | | 100 | | 120 | | ns |
| Chip Select to End of Write | t _{CW} | 60 | | 75 | | 80 | | 100 | | ns |
| Address Valid to End of Write | t _{AW} | 60 | | 75 | | 80 | | 100 | | ns |
| Data Valid to End of Write | t _{DW} | 30 | | 35 | | 40 | | 40 | | ns |
| Write Pulse Width | t _{WP} | 50 | | 50 | | 60 | | 60 | | ns |
| Address Setup Time | t _{AS} | 0 | | 0 | | 0 | | 0 | | ns |
| Address Hold Time | t _{AH} | 5 | | 5 | | 5 | | 5 | | ns |
| Output Active from End of Write | t _{OW} ¹ | 5 | | 5 | | 5 | | 5 | | ns |
| Write Enable to Output in High Z | t _{WHZ} ¹ | | 25 | | 25 | | 35 | | 35 | ns |
| Data Hold from Write Time | t _{DH} | 0 | | 0 | | 0 | | 0 | | ns |

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AC TEST CIRCUIT



AC TEST CONDITIONS

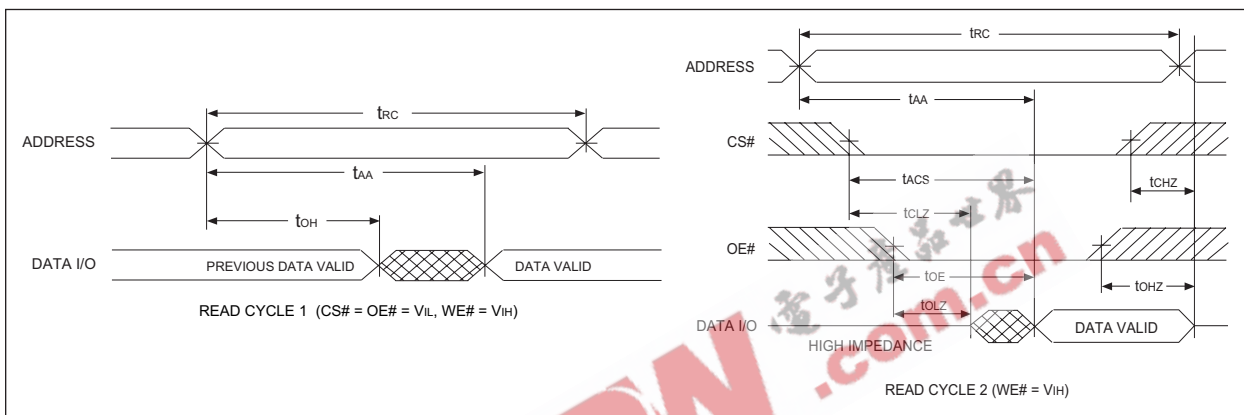
| Parameter | Typ | Unit |
|----------------------------------|--|------|
| Input Pulse Levels | V _{IL} = 0, V _{IH} = 3.0 | V |
| Input Rise and Fall | 5 | ns |
| Input and Output Reference Level | 1.5 | V |
| Output Timing Reference Level | 1.5 | V |

NOTES:

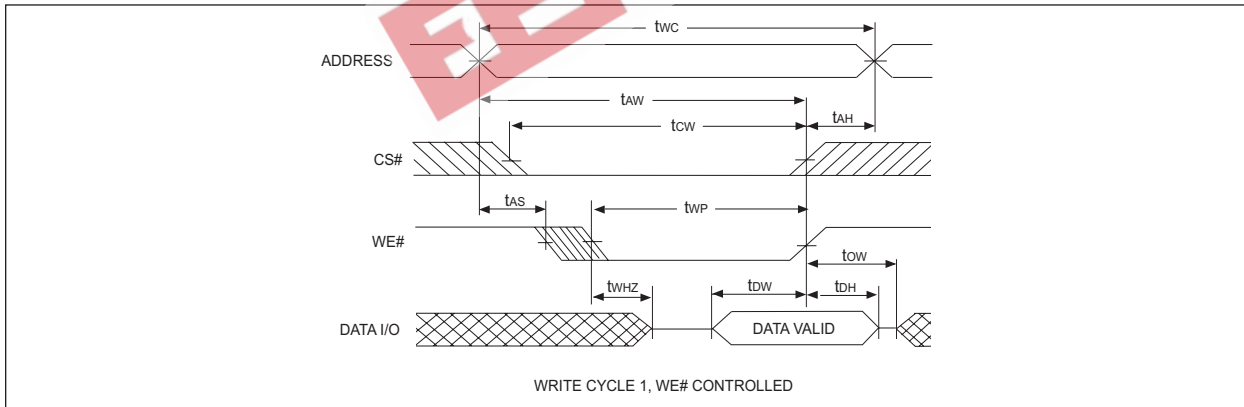
V_z is programmable from -2V to +7V.
 I_{oL} & I_{oH} programmable from 0 to 16mA.
 Tester Impedance Z₀ = 75 Ω.
 V_z is typically the midpoint of V_{OH} and V_{OL}.
 I_{oL} & I_{oH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.



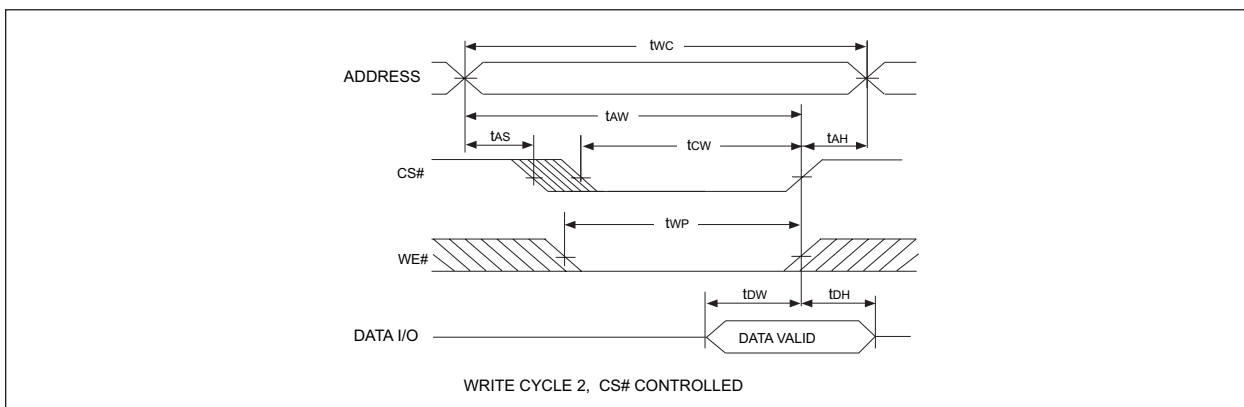
TIMING WAVEFORM - READ CYCLE



WRITE CYCLE - WE# CONTROLLED

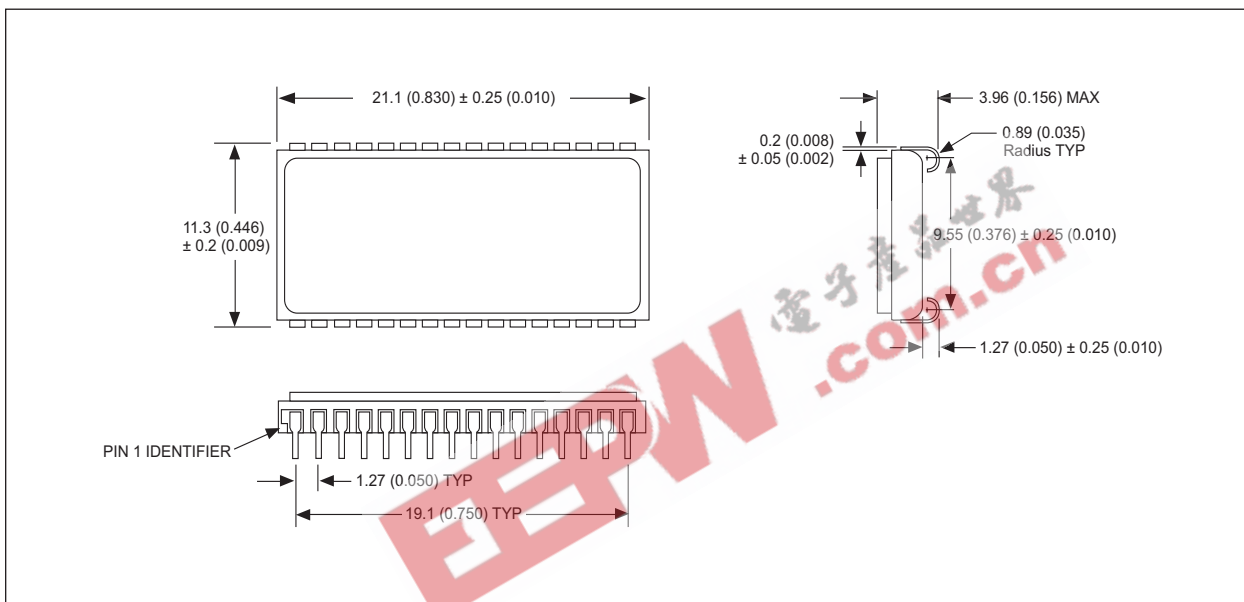


WRITE CYCLE - CS# CONTROLLED



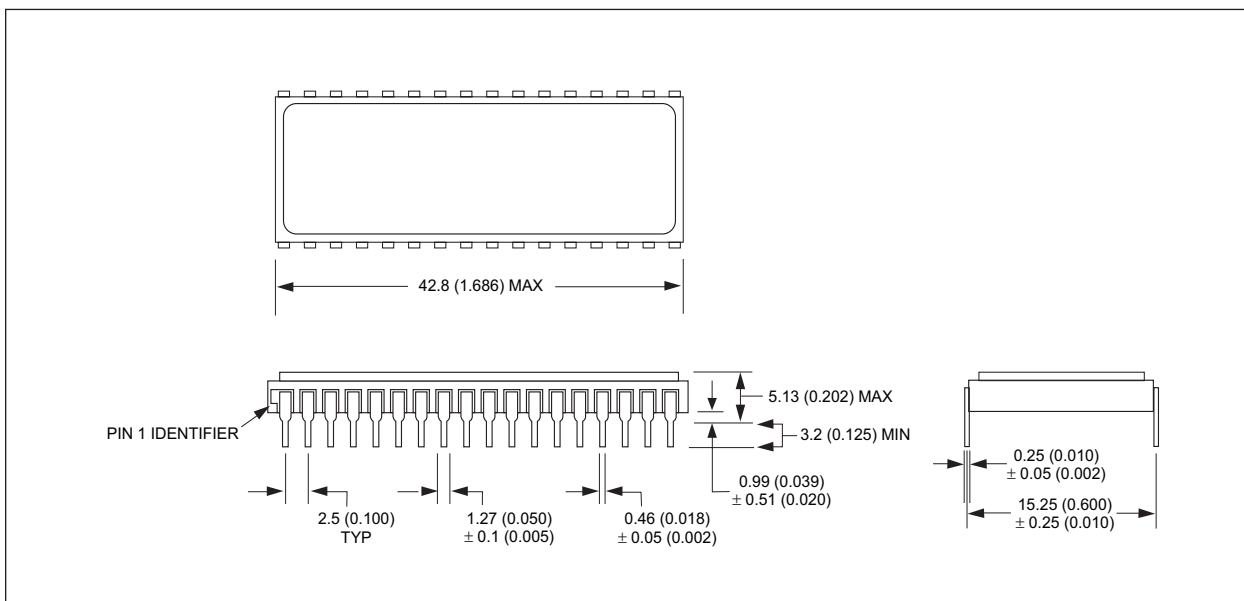


PACKAGE 101: 32 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



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ORDERING INFORMATION

W M S 512K 8 V L - XXX X X X X

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

SPECIAL PROCESSING:

- E = Epitaxial Layer

DEVICE GRADE:

- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE:

- C = 32 Pin Ceramic 0.600" DIP (Package 300)
- DE = 32 Lead Ceramic SOJ (Package 101) Evolutionary

ACCESS TIME (ns)

IMPROVEMENT MARK

- L = Low Power Data Retention

Low Voltage Supply 3.3V ± 10%

ORGANIZATION, 512K x 8

SRAM

MONOLITHIC

WHITE ELECTRONIC DESIGNS CORP.

