



128Kx8 MONOLITHIC FLASH, SMD 5962-96690

FEATURES

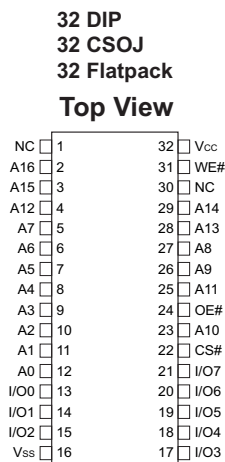
- Access Times of 50*, 60, 70, 90, 120, 150ns
- Packaging
 - 32 lead, Hermetic Ceramic, 0.400" SOJ (Package 101)
 - 32 pin, Hermetic Ceramic, 0.600" DIP (Package 300)
 - 32 lead, Flatpack (Package 220)
 - 32 lead, Formed Flatpack (Package 221)
 - 32 pin, Rectangular Ceramic Leadless Chip Carrier (Package 601)
- 100,000 Erase/Program Cycles Minimum
- Sector Erase Architecture
 - 8 equal size sectors of 16KBytes each
 - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 128Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Programming. 5V ± 10% Supply.
- Low Power CMOS
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Page Program Operation and Internal Program Control Time.

This product is subject to change without notice.

Note: For programming information refer to Flash Programming 1M5 Application Note.

* The access time of 50ns is available in Industrial and Commercial temperature ranges only.

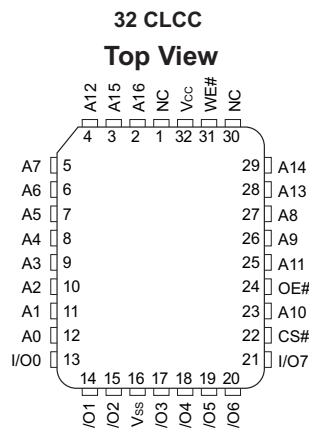
Pin Configuration For WMF128K8-XXX5



Pin Description

| | |
|--------|-------------------|
| A0-16 | Address Inputs |
| I/O0-7 | Data Input/Output |
| CS# | Chip Select |
| OE# | Output Enable |
| WE# | Write Enable |
| Vcc | +5.0V Power |
| Vss | Ground |

Pin Configuration For WMF128K8-XCLX5





ABSOLUTE MAXIMUM RATINGS (1)

| Parameter | | Unit |
|--|---------------|--------|
| Operating Temperature | -55 to +125 | °C |
| Supply Voltage (V _{CC}) | -2.0 to +7.0 | V |
| Signal Voltage Range (any pin except A9) (2) | -2.0 to +7.0 | V |
| Storage Temperature Range | -65 to +150 | °C |
| Lead Temperature (soldering, 10 seconds) | +300 | °C |
| Data Retention Mil Temp | 10 | years |
| Endurance (write/erase cycles) (Mil Temp) | 10,000 min | cycles |
| A9 Voltage for sector protect (V _{ID}) (3) | -2.0 to +14.0 | V |

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|-------------------------------|-----------------|------|-----------------------|------|
| Supply Voltage | V _{CC} | 4.5 | 5.5 | V |
| Input High Voltage | V _{IH} | 2.0 | V _{CC} + 0.5 | V |
| Input Low Voltage | V _{IL} | -0.5 | +0.8 | V |
| Operating Temp. (Mil.) | T _A | -55 | +125 | °C |
| Operating Temp. (Ind.) | T _A | -40 | +85 | °C |
| A9 Voltage for Sector Protect | V _{ID} | 11.5 | 12.5 | V |

NOTES:

- Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot V_{SS} to -2.0 V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods of up to 20ns.
- Minimum DC input voltage on A9 pin is -0.5V. During voltage transitions, A9 may overshoot V_{SS} to -2V for periods of up to 20ns. Maximum DC input voltage on A9 is +13.5V which may overshoot to 14.0 V for periods up to 20ns.

CAPACITANCE

T_A = +25°C

| Parameter | Symbol | Conditions | Max | Unit |
|---------------------------|-----------------|------------------------------------|-----|------|
| Address Input capacitance | C _{AD} | V _{IO} = 0 V, f = 1.0 MHz | 15 | pF |
| Output Enable capacitance | C _{OE} | V _{IN} = 0 V, f = 1.0 MHz | 15 | pF |
| Write Enable capacitance | C _{WE} | V _{IN} = 0 V, f = 1.0 MHz | 15 | pF |
| Chip Select capacitance | C _{CS} | V _{IN} = 0 V, f = 1.0 MHz | 15 | pF |
| Data I/O capacitance | C _{IO} | V _{IO} = 0 V, f = 1.0 MHz | 15 | pF |

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS — CMOS COMPATIBLE

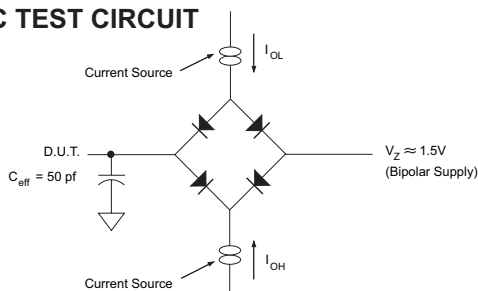
V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

| Parameter | Symbol | Conditions | Min | Max | Unit |
|---|------------------|---|------------------------|------|------|
| Input Leakage Current | I _{LI} | V _{CC} = 5.5, V _{IN} = GND to V _{CC} | | 10 | µA |
| Output Leakage Current | I _{LO} | V _{CC} = 5.5, V _{IN} = GND to V _{CC} | | 10 | µA |
| V _{CC} Active Current for Read (1) | I _{CC1} | CS# = V _{IL} , OE# = V _{IH} | | 35 | mA |
| V _{CC} Active Current for Program or Erase (2) | I _{CC2} | CS# = V _{IL} , OE# = V _{IH} | | 50 | mA |
| V _{CC} Standby Current | I _{CC3} | V _{CC} = 5.5, CS# = V _{IH} , f = 5MHz | | 1.6 | mA |
| Output Low Voltage | V _{OL} | I _{OL} = 8.0 mA, V _{CC} = 4.5 | | 0.45 | V |
| Output High Voltage | V _{OH1} | I _{OH} = -2.5 mA, V _{CC} = 4.5 | 0.85 x V _{CC} | | V |
| Output High Voltage | V _{OH2} | I _{OH} = -100 µA, V _{CC} = 4.5 | V _{CC} - 0.4 | | V |
| Low V _{CC} Lock-Out Voltage | V _{LKO} | | 3.2 | | V |

NOTES:

- The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with OE# at V_{IH}.
- I_{CC} active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

AC TEST CIRCUIT



AC TEST CONDITIONS

| Parameter | Typ | Unit |
|----------------------------------|--|------|
| Input Pulse Levels | V _{IL} = 0, V _{IH} = 3.0 | V |
| Input Rise and Fall | 5 | ns |
| Input and Output Reference Level | 1.5 | V |
| Output Timing Reference Level | 1.5 | V |

Notes:
 V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance Z₀ = 75 Ω.
 V_Z is typically the midpoint of V_{OH} and V_{OL}.
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, WE# CONTROLLED

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

| Parameter | Symbol | | -50 | | -60 | | -70 | | -90 | | -120 | | -150 | | Unit |
|--|--------------------|------------------|-----|------|-----|------|-----|------|-----|------|------|------|------|------|------|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | t _{AVAV} | t _{WC} | 50 | | 60 | | 70 | | 90 | | 120 | | 150 | | ns |
| Chip Select Setup Time | t _{ELWL} | t _{CS} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Write Enable Pulse Width | t _{WLWH} | t _{WP} | 25 | | 30 | | 35 | | 45 | | 50 | | 50 | | ns |
| Address Setup Time | t _{AVWH} | t _{AS} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Data Setup Time | t _{DVWH} | t _{DS} | 25 | | 30 | | 30 | | 45 | | 50 | | 50 | | ns |
| Data Hold Time | t _{WDHX} | t _{DH} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Address Hold Time | t _{WHAX} | t _{AH} | 40 | | 45 | | 45 | | 45 | | 50 | | 50 | | ns |
| Chip Select Hold Time | t _{WHEH} | t _{CH} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Write Enable Pulse Width High | t _{WHWL} | t _{WPH} | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | ns |
| Duration of Byte Programming Operation (min) | t _{WHWH1} | | 14 | | 14 | | 14 | | 14 | | 14 | | 14 | | μs |
| Sector Erase Time | t _{WHWH2} | | 2.2 | 60 | 2.2 | 60 | 2.2 | 60 | 2.2 | 60 | 2.2 | 60 | 2.2 | 60 | sec |
| Read Recovery Time before Write | t _{GHWL} | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ms |
| V _{CC} Set-up Time | | t _{VCS} | 50 | | 50 | | 50 | | 50 | | 50 | | 50 | | μs |
| Chip Programming Time | | | | 12.5 | | 12.5 | | 12.5 | | 12.5 | | 12.5 | | 12.5 | sec |
| Output Enable Setup Time | | t _{OES} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Output Enable Hold Time (1) | | t _{OEH} | 10 | | 10 | | 10 | | 10 | | 10 | | 10 | | ns |

NOTES:

1. For Toggle and Data# Polling.

AC CHARACTERISTICS – READ ONLY OPERATIONS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

| Parameter | Symbol | | -50 | | -60 | | -70 | | -90 | | -120 | | -150 | | Unit |
|---|-------------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|------|-----|------|-----|------|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | t _{AVAV} | t _{RC} | 50 | | 60 | | 70 | | 90 | | 120 | | 150 | | ns |
| Address Access Time | t _{AVQV} | t _{ACC} | | 50 | | 60 | | 70 | | 90 | | 120 | | 150 | ns |
| Chip Select Access Time | t _{ELQV} | t _{CE} | | 50 | | 60 | | 70 | | 90 | | 120 | | 150 | ns |
| OE# to Output Valid | t _{GLQV} | t _{OE} | | 25 | | 30 | | 35 | | 40 | | 50 | | 55 | ns |
| Chip Select to Output High Z (1) | t _{EHQZ} | t _{DF} | | 20 | | 20 | | 20 | | 25 | | 30 | | 35 | ns |
| OE# High to Output High Z (1) | t _{GHQZ} | t _{DF} | | 20 | | 20 | | 20 | | 25 | | 30 | | 35 | ns |
| Output Hold from Address, CS# or OE# Change, whichever is First | t _{AXQX} | t _{OH} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |

NOTES:

1. Guaranteed by design, but not tested



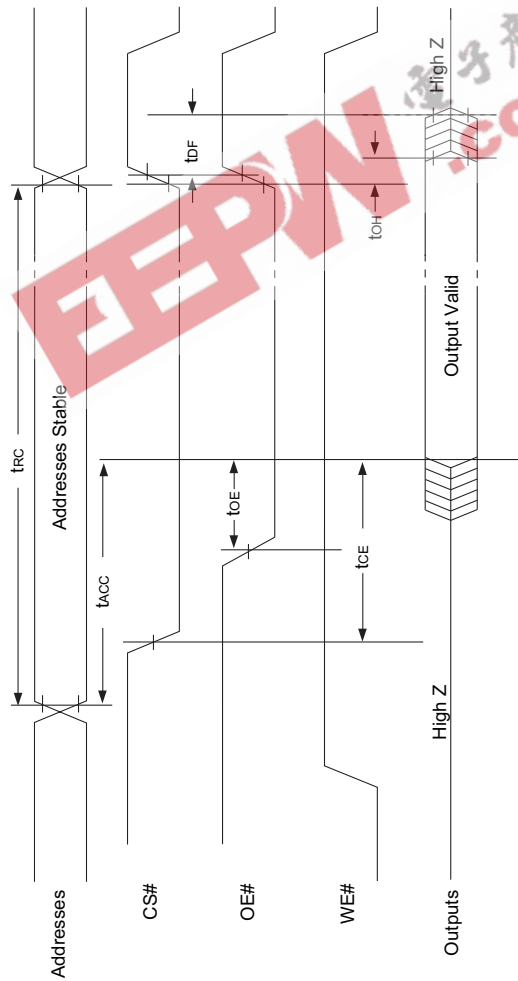
AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, CS# CONTROLLED

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

| Parameter | Symbol | | -50 | | -60 | | -70 | | -90 | | -120 | | -150 | | Unit |
|-----------------------------------|--------------------|------------------|-----|------|-----|------|-----|------|-----|------|------|------|------|------|------|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | t _{AVAV} | t _{WC} | 50 | | 60 | | 70 | | 90 | | 120 | | 150 | | ns |
| WE# Setup Time | t _{WLEL} | t _{WS} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| CS# Pulse Width | t _{LEH} | t _{CP} | 25 | | 30 | | 35 | | 45 | | 50 | | 50 | | ns |
| Address Setup Time | t _{AVEL} | t _{AS} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Data Setup Time | t _{DVEH} | t _{DS} | 25 | | 30 | | 30 | | 45 | | 50 | | 50 | | ns |
| Data Hold Time | t _{EHDX} | t _{DH} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Address Hold Time | t _{ELAX} | t _{AH} | 40 | | 45 | | 45 | | 45 | | 50 | | 50 | | ns |
| WE# Hold from WE# High | t _{EHWH} | t _{WH} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| CS# Pulse Width High | t _{HEL} | t _{CPH} | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | ns |
| Duration of Programming Operation | t _{WHWH1} | | 14 | | 14 | | 14 | | 14 | | 14 | | 14 | | μs |
| Duration of Erase Operation | t _{WHWH2} | | 2.2 | 60 | 2.2 | 60 | 2.2 | 60 | 2.2 | 60 | 2.2 | 60 | 2.2 | 60 | sec |
| Read Recovery before Write | t _{GHEL} | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Chip Programming Time | | | | 12.5 | | 12.5 | | 12.5 | | 12.5 | | 12.5 | | 12.5 | sec |

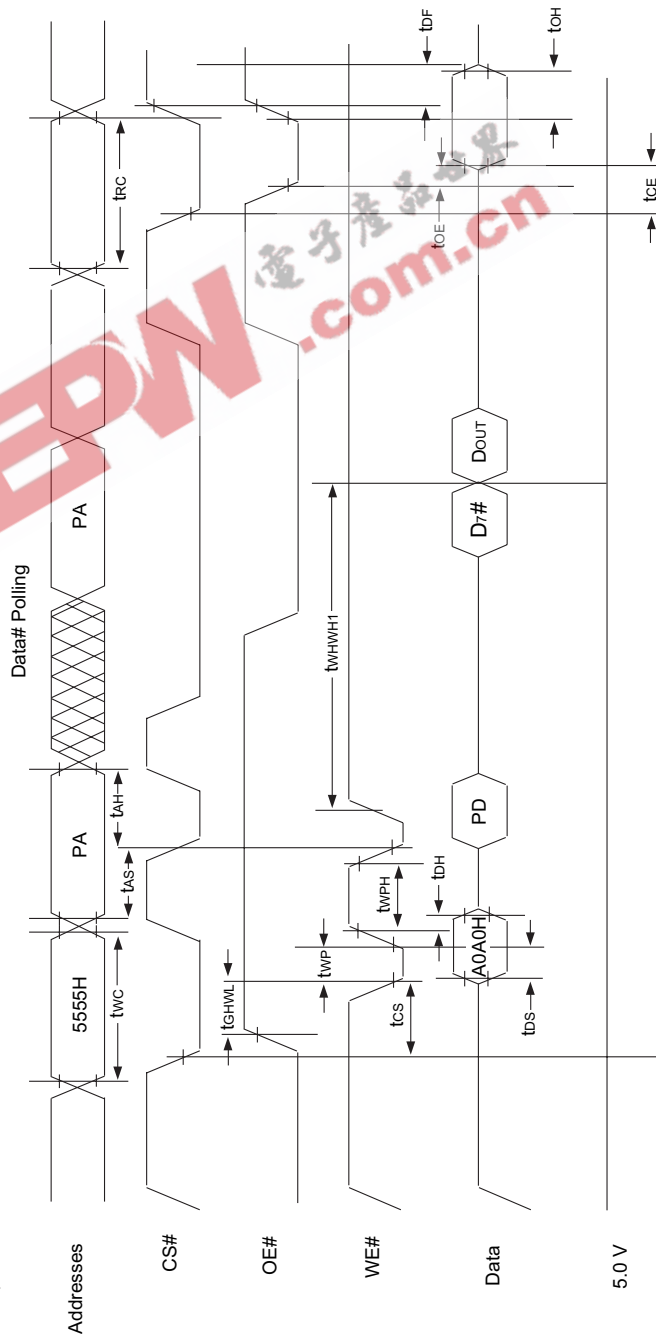


AC WAVEFORMS FOR READ OPERATIONS





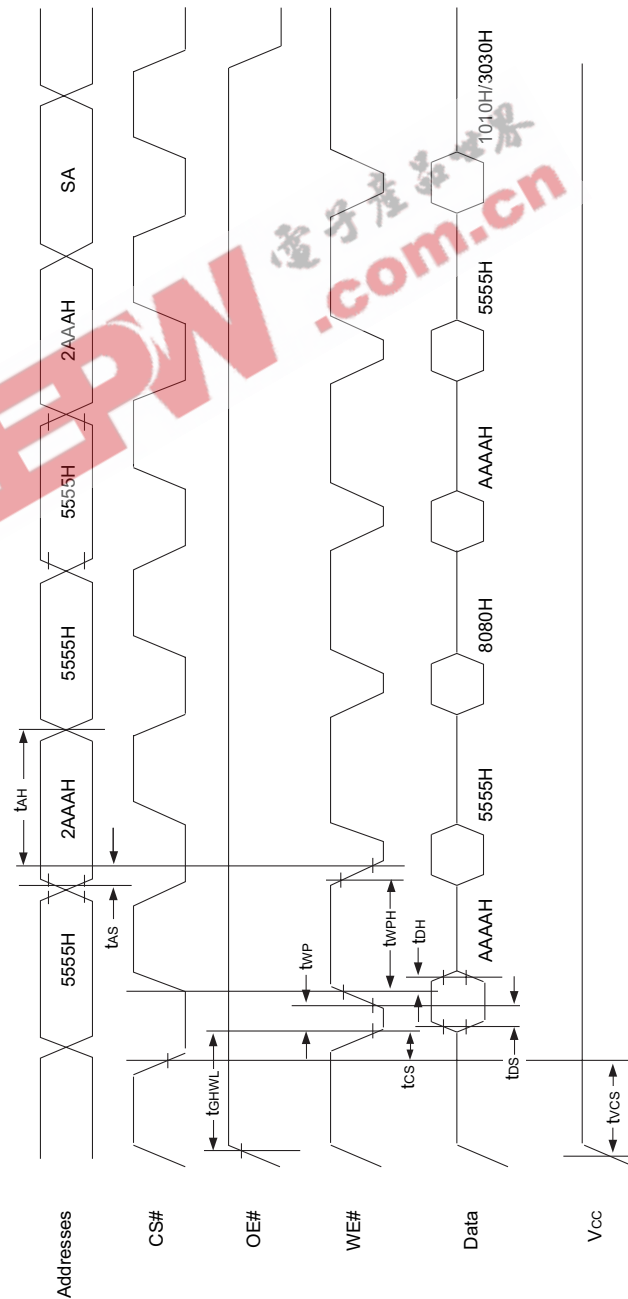
WRITE/ERASE/PROGRAM OPERATION, WE# CONTROLLED



- NOTES:
1. PA is the address of the memory location to be programmed.
 2. PD is the data to be programmed at byte address.
 3. D7# is the output of the complement of the data written to each chip.
 4. DOUT is the output of the data written to the device.
 5. Figure indicates last two bus cycles of four bus cycle sequence.



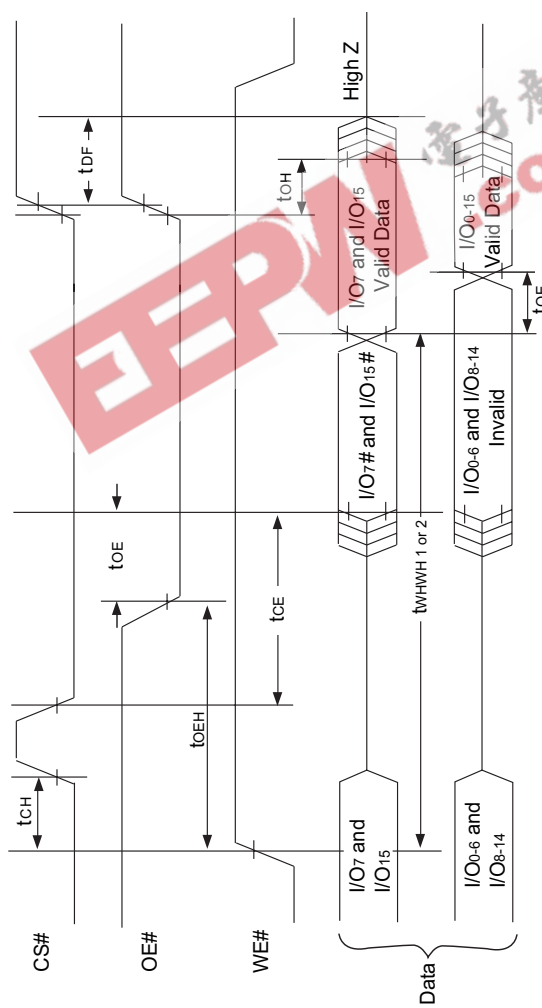
AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



NOTE:
1. SA is the sector address for Sector Erase.

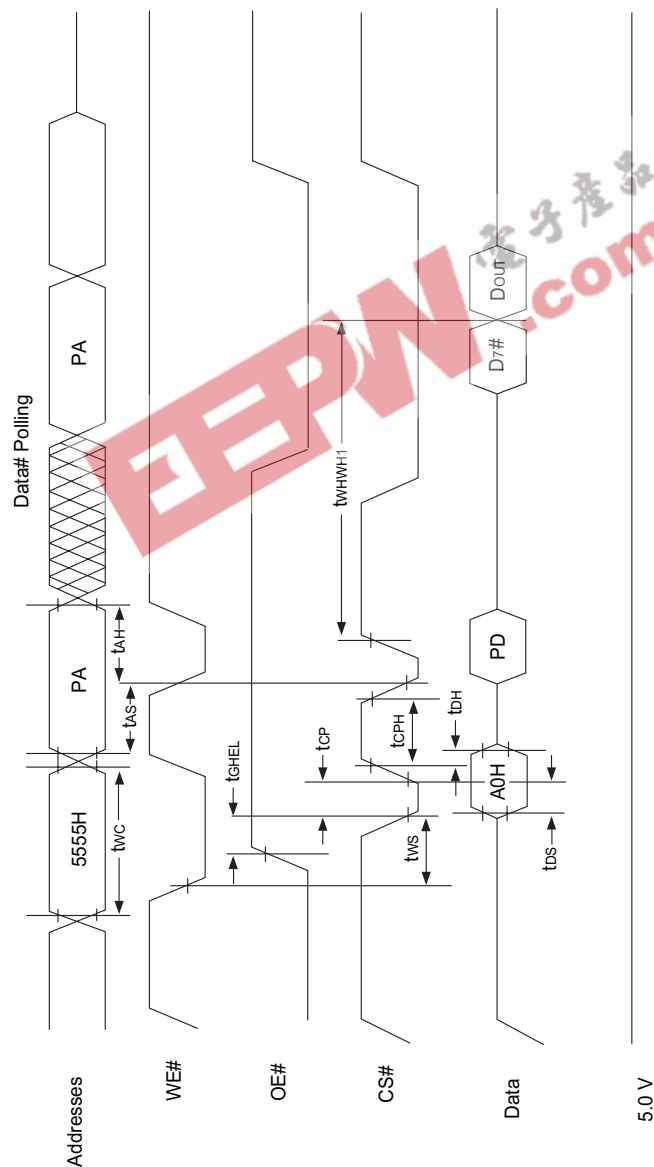


AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS





ALTERNATE CS# CONTROLLED PROGRAMMING OPERATION TIMINGS

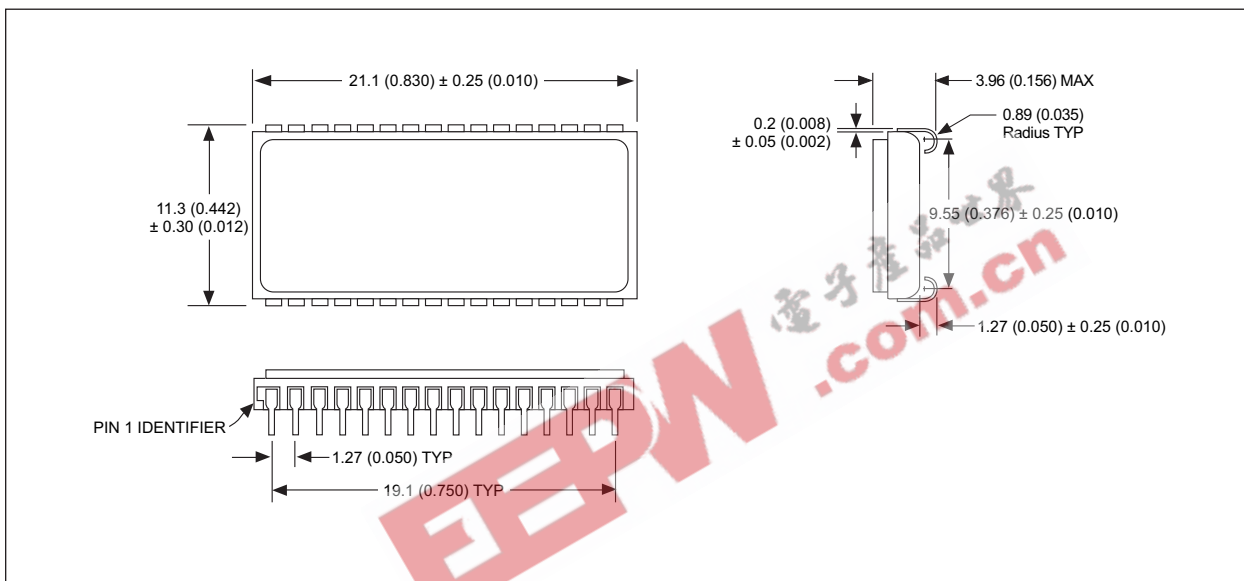


NOTES:

1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to each chip.
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

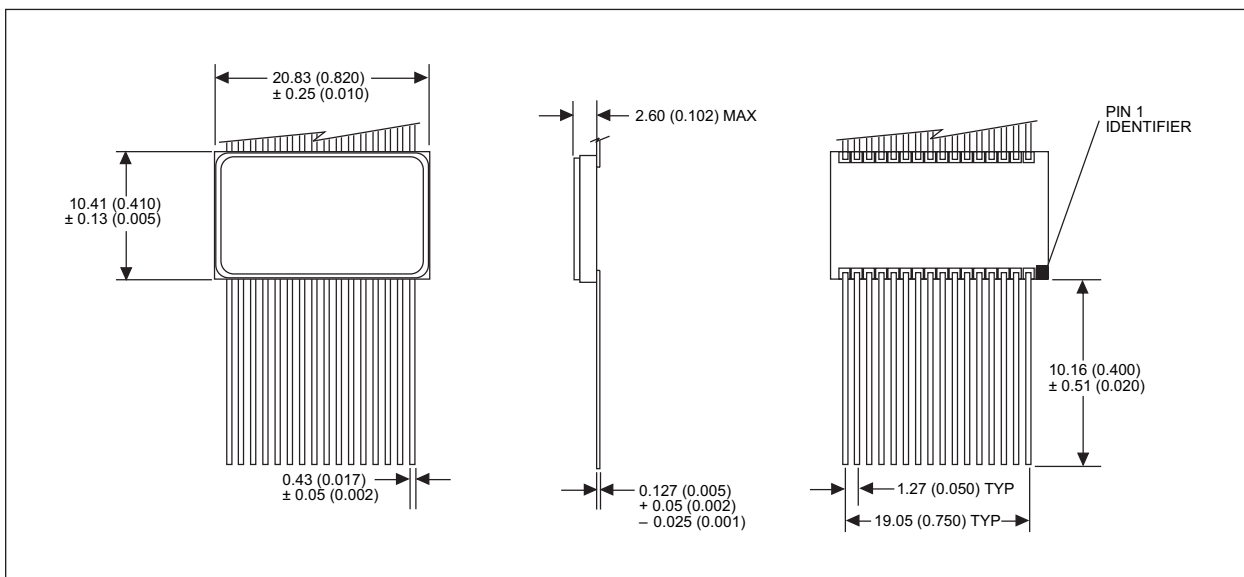


PACKAGE 101: 32 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

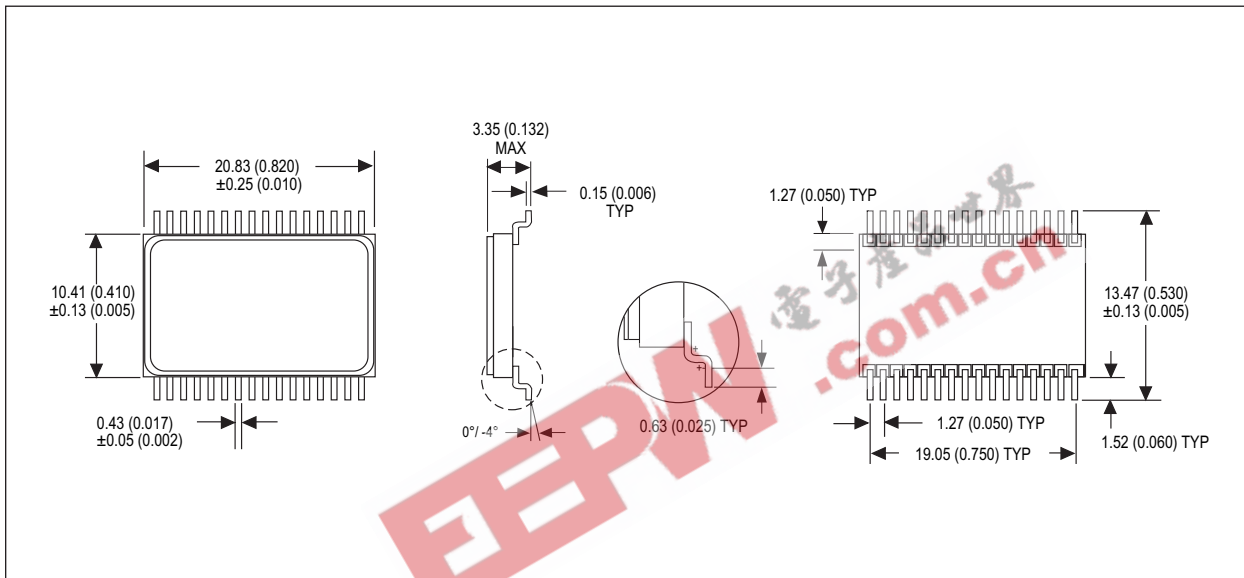
PACKAGE 220: 32 LEAD, CERAMIC FLATPACK



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

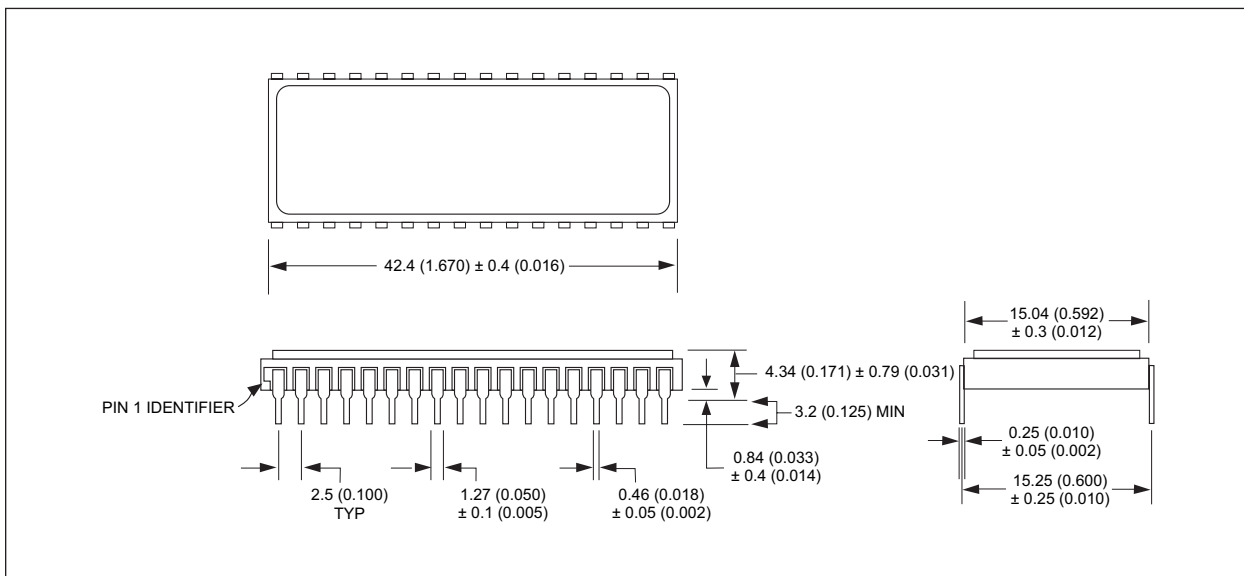


PACKAGE 221: 32 LEAD, FORMED CERAMIC FLATPACK



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

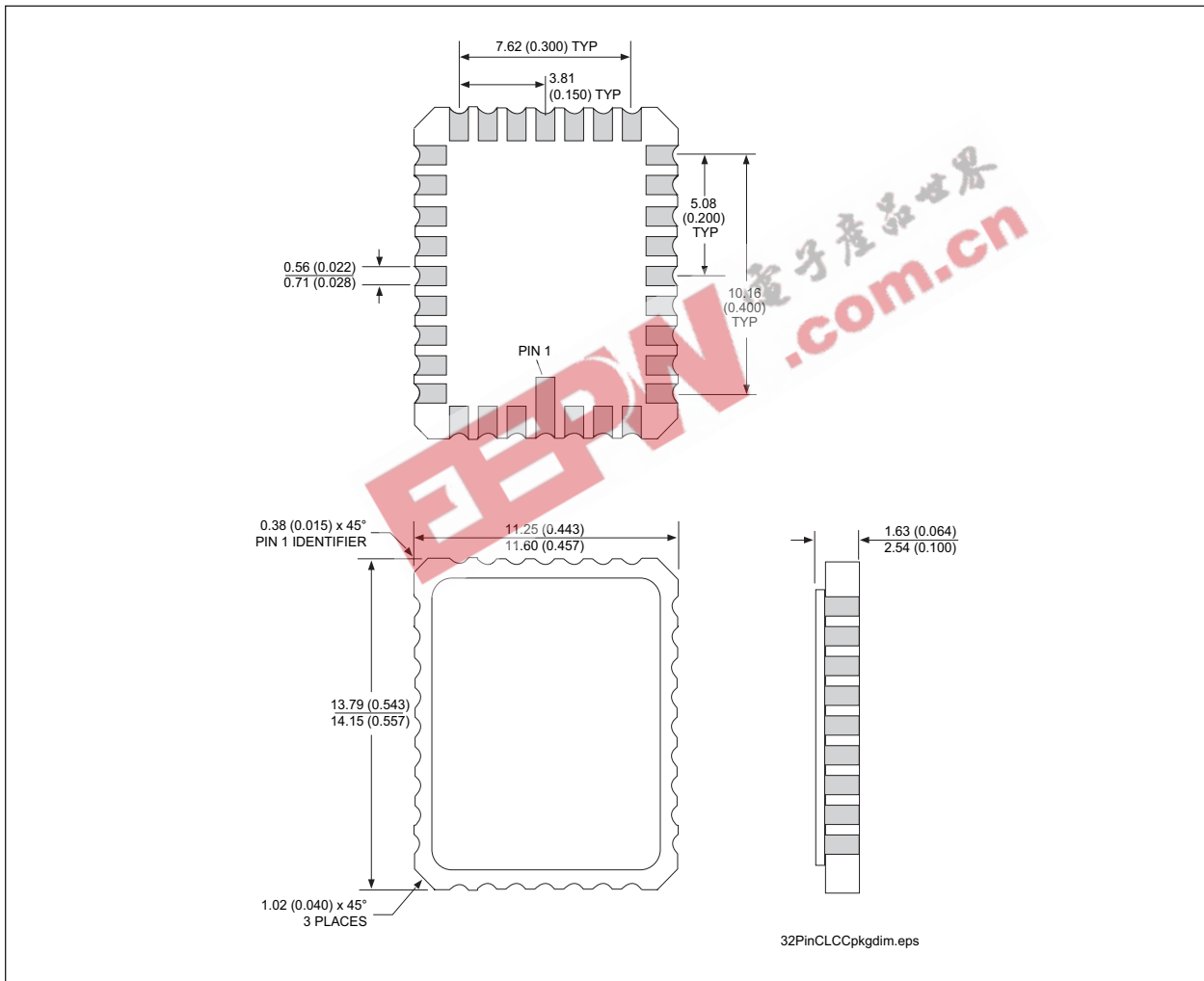
PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 601: 32 PIN, RECTANGULAR CERAMIC LEADLESS CHIP CARRIER



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

W M F 128K8 -XXX X X 5 X

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

V_{PP} PROGRAMMING VOLTAGE

- 5 = 5V

DEVICE GRADE:

- Q = MIL-STD-883 Compliant
- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE TYPE:

- DE = 32 Lead Ceramic SOJ (Package 101)
- C = 32 Pin Ceramic DIP (Package 300)
- FE = 32 Lead Ceramic Flatpack (Package 220)
- FF = 32 Lead Formed Ceramic Flatpack (Package 221)
- CL = 32 Pin rectangular Ceramic Leadless Chip Carrier (Package 601)

ACCESS TIME (ns)

ORGANIZATION, 128K x 8

Flash

MONOLITHIC

WHITE ELECTRONIC DESIGNS CORP.



| DEVICE TYPE | SECTOR SIZE | SPEED | PACKAGE | SMD NO. |
|---------------------------|-------------|-------|------------------------------|------------------|
| 128K x 8 Flash Monolithic | 16KByte | 150ns | 32 pin DIP (C) | 5962-96690 01HXX |
| 128K x 8 Flash Monolithic | 16KByte | 120ns | 32 pin DIP (C) | 5962-96690 02HXX |
| 128K x 8 Flash Monolithic | 16KByte | 90ns | 32 pin DIP (C) | 5962-96690 03HXX |
| 128K x 8 Flash Monolithic | 16KByte | 70ns | 32 pin DIP (C) | 5962-96690 04HXX |
| 128K x 8 Flash Monolithic | 16KByte | 60ns | 32 pin DIP (C) | 5962-96690 05HXX |
| 128K x 8 Flash Monolithic | 16KByte | 150ns | 32 lead SOJ (DE) | 5962-96690 01HXX |
| 128K x 8 Flash Monolithic | 16KByte | 120ns | 32 lead SOJ (DE) | 5962-96690 02HXX |
| 128K x 8 Flash Monolithic | 16KByte | 90ns | 32 lead SOJ (DE) | 5962-96690 03HXX |
| 128K x 8 Flash Monolithic | 16KByte | 70ns | 32 lead SOJ (DE) | 5962-96690 04HXX |
| 128K x 8 Flash Monolithic | 16KByte | 60ns | 32 lead SOJ (DE) | 5962-96690 05HXX |
| 128K x 8 Flash Monolithic | 16KByte | 150ns | 32 lead Flatpack (FE) | 5962-96690 01HTX |
| 128K x 8 Flash Monolithic | 16KByte | 120ns | 32 lead Flatpack (FE) | 5962-96690 02HTX |
| 128K x 8 Flash Monolithic | 16KByte | 90ns | 32 lead Flatpack (FE) | 5962-96690 03HTX |
| 128K x 8 Flash Monolithic | 16KByte | 70ns | 32 lead Flatpack (FE) | 5962-96690 04HTX |
| 128K x 8 Flash Monolithic | 16KByte | 60ns | 32 lead Flatpack (FE) | 5962-96690 05HTX |
| 128K x 8 Flash Monolithic | 16KByte | 150ns | 32 lead Formed Flatpack (FF) | 5962-96690 01HUX |
| 128K x 8 Flash Monolithic | 16KByte | 120ns | 32 lead Formed Flatpack (FF) | 5962-96690 02HUX |
| 128K x 8 Flash Monolithic | 16KByte | 90ns | 32 lead Formed Flatpack (FF) | 5962-96690 03HUX |
| 128K x 8 Flash Monolithic | 16KByte | 70ns | 32 lead Formed Flatpack (FF) | 5962-96690 04HUX |
| 128K x 8 Flash Monolithic | 16KByte | 60ns | 32 lead Formed Flatpack (FF) | 5962-96690 05HUX |