512Kx8 MONOLITHIC SRAM

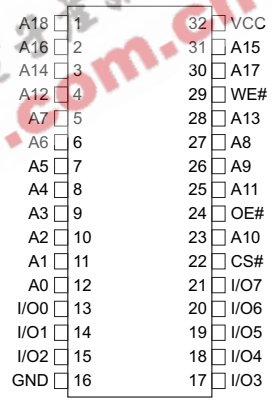
FEATURES

- Access Times 70, 85, 100, 120ns
- MIL-STD-883 Compliant Devices Available
- Low Voltage Operation
- Evolutionary, Corner Power/Ground Pinout JEDEC Approved
  - 32 pin Ceramic DIP (Package 300)
  - 32 lead Ceramic SOJ (Package 101)
- Commercial, Industrial and Military Temperature Ranges
- Low Power CMOS
- Low Voltage Operation
  - 3.3V ± 10% Power Supply
- Low Power Data Retention
- TTL Compatible Inputs and Outputs

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

EVOLUTIONARY PINOUT

32 DIP
32 CSOJ (DE)
TOP VIEW



PIN DESCRIPTION

A0-18	Address Inputs
I/O0-7	Data Input/Output
CS#	Chip Select
OE#	Output Enable
WE#	Write Enable
V_{CC}	+3.3V Power Supply
GND	Ground

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	V_{CC}+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

TRUTH TABLE

CS#	OE#	WE#	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V, f = 1.0MHz	12	pF
Output capacitance	C_{OUT}	V_{OUT} = 0V, f = 1.0MHz	12	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 3.6, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	CS# = V_{IH}, OE# = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current	I_{CC}	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz, V_{CC} = 3.6		25	mA
Standby Current	I_{SB}	CS# = V_{IH}, OE# = V_{IH}, f = 5MHz, V_{CC} = 3.6		400	µA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA, V_{CC} = 3.0		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA, V_{CC} = 3.0	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

AC CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter Read Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		120		ns
Address Access Time	t_{AA}		70		85		100		120	ns
Output Hold from Address Change	t_{OH}	5		5		5		5		ns
Chip Select Access Time	t_{ACS}		70		85		100		120	ns
Output Enable to Output Valid	t_{OE}		35		40		50		60	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	10		10		10		10		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	5		5		5		5		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		25		25		35		35	ns
Output Disable to Output in High Z	t_{OHZ}[1]		25		25		35		35	ns

1. This parameter is guaranteed by design but not tested.

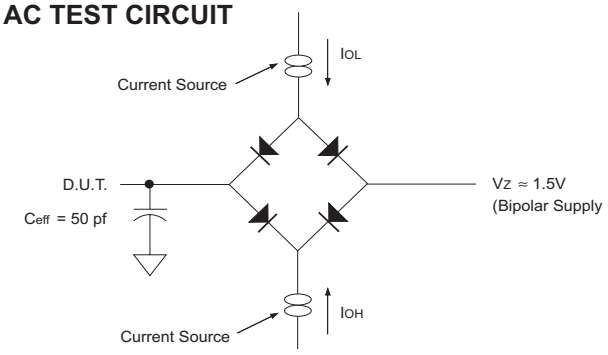
AC CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter Write Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		120		ns
Chip Select to End of Write	t_{CW}	60		75		80		100		ns
Address Valid to End of Write	t_{AW}	60		75		80		100		ns
Data Valid to End of Write	t_{DW}	30		35		40		40		ns
Write Pulse Width	t_{WP}	50		50		60		60		ns
Address Setup Time	t_{AS}	0		0		0		0		ns
Address Hold Time	t_{AH}	5		5		5		5		ns
Output Active from End of Write	t_{OW}[1]	5		5		5		5		ns
Write Enable to Output in High Z	t_{WHZ}[1]		25		25		35		35	ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

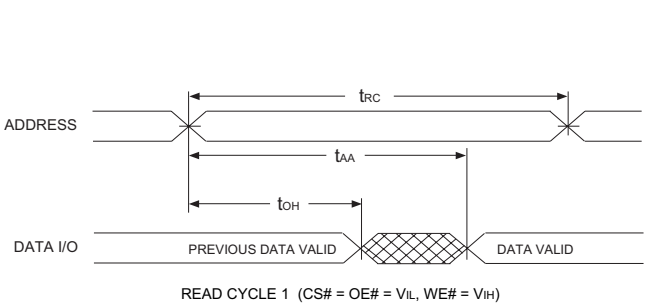


AC TEST CONDITIONS

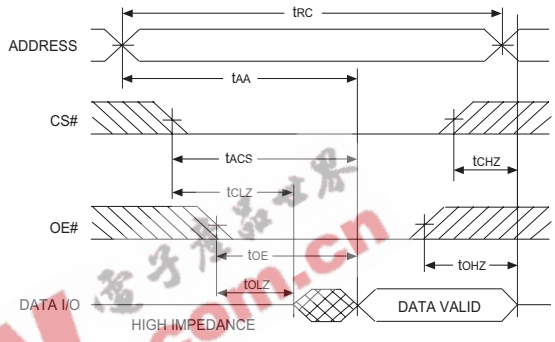
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

TIMING WAVEFORM - READ CYCLE

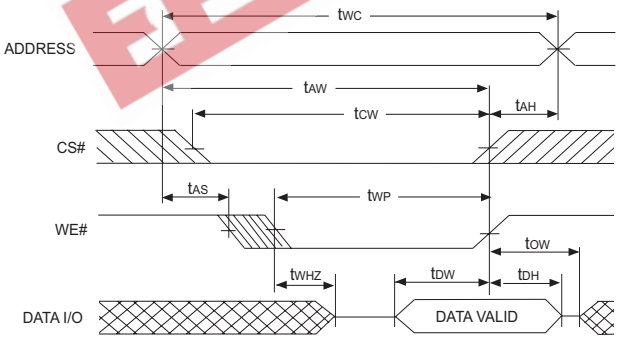


READ CYCLE 1 (CS# = OE# = V_{IL}, WE# = V_{IH})



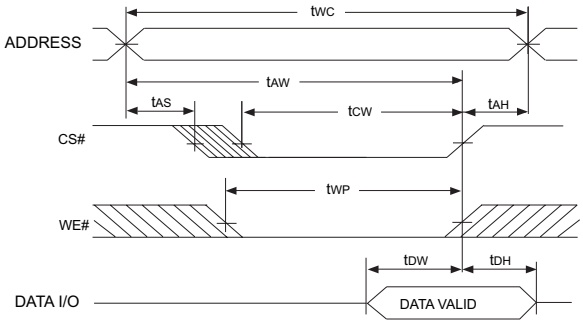
READ CYCLE 2 (WE# = V_{IH})

WRITE CYCLE - WE# CONTROLLED



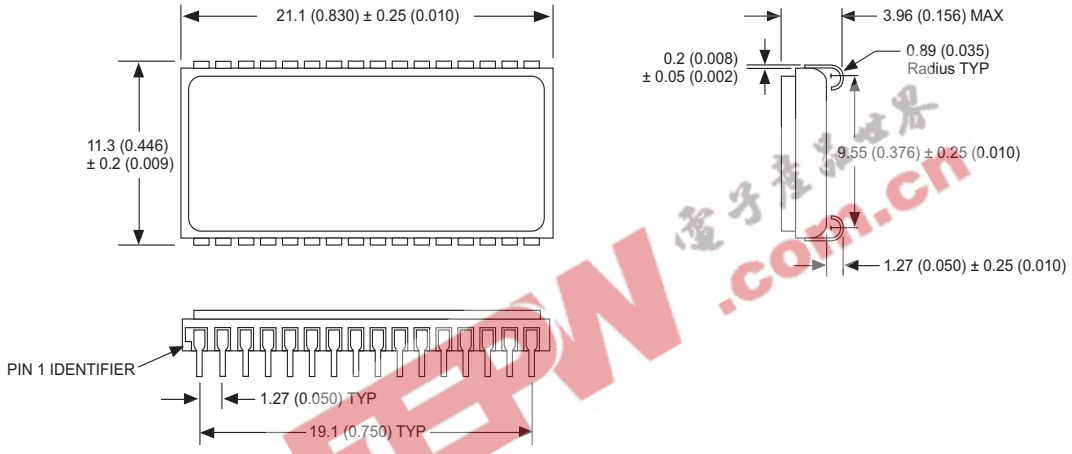
WRITE CYCLE 1, WE# CONTROLLED

WRITE CYCLE - CS# CONTROLLED



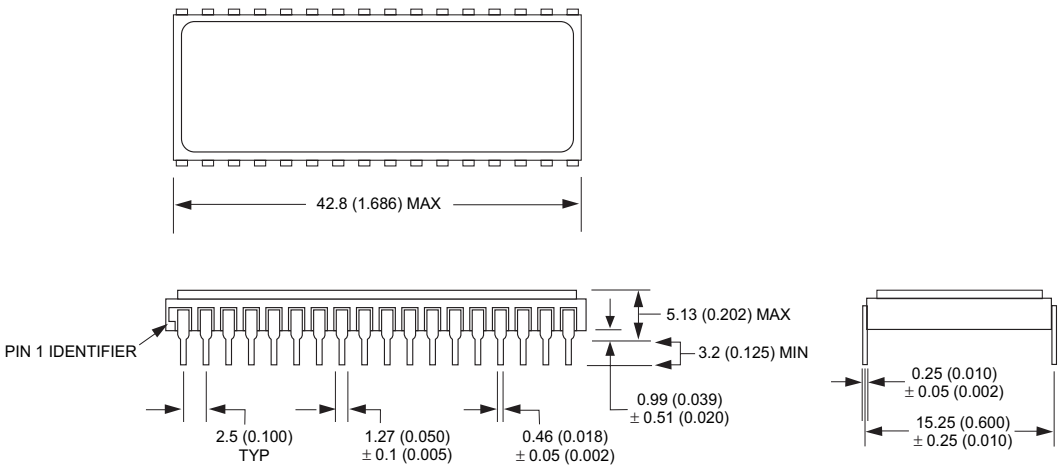
WRITE CYCLE 2, CS# CONTROLLED

PACKAGE 101: 32 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



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ORDERING INFORMATION