



## 256Kx16 MONOLITHIC SRAM, SMD 5962-96902

### FEATURES

- Access Times 17, 20, 25, 35ns
- MIL-STD-883 Compliant Devices Available
- Packaging
  - 44 pin Ceramic SOJ (Package 102)
  - 44 lead Ceramic Flatpack (Package 225)
  - 44 lead Formed Ceramic Flatpack
- Organized as 256Kx16
- Data Byte Control:
  - Lower Byte (LB#) = I/O<sub>1-8</sub>
  - Upper Byte (UB#) = I/O<sub>9-16</sub>
- 2V Minimum Data Retention for battery back up operation (WMS256K16L-XXX Low Power Version Only)
- Commercial, Industrial and Military Temperature Range
- 5V Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs

### PIN CONFIGURATION FOR WMS256K16-XXX



### PIN DESCRIPTION

A0-17	Address Inputs
LB#	Lower-Byte Control (I/O <sub>1-8</sub> )
UB#	Upper-Byte Control (I/O <sub>9-16</sub> )
I/O <sub>1-16</sub>	Data Input/Output
CS#	Chip Select
OE#	Output Enable
WE#	Write Enable
Vcc	+5.0V Power
GND	Ground
NC	No Connection



**TRUTH TABLE**

CS#	WE#	OE#	LB#	UB#	Mode	Data I/O		Power
						I/O <sub>1-8</sub>	I/O <sub>9-16</sub>	
H	X	X	X	X	Not Select	High Z	High Z	Standby
L	H	H	X	X	Output Disable	High Z	High Z	Active
L	X	X	H	H				
L	H	L	L	H	Read	Data Out	High Z	Active
			H	L		High Z	Data Out	
			L	L		Data Out	Data Out	
L	L	X	L	H	Write	Data In	High Z	Active
			H	L		High Z	Data In	
			L	L		Data In	Data In	

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	VG	-0.5	V <sub>CC</sub> +0.5	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	7.0	V

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	+0.8	V
Operating Temp. (Mil.)	T <sub>A</sub>	-55	+125	°C

**CAPACITANCE**

T<sub>A</sub> = +25°C

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V, f = 1.0MHz	20	pF
Output capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> = 0V, f = 1.0MHz	20	pF

This parameter is guaranteed by design but not tested.

**DC CHARACTERISTICS**

V<sub>CC</sub> = 5.0V, GND = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10	μA
Output Leakage Current	I <sub>LO</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10	μA
Operating Supply Current	I <sub>CC</sub>	CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		275	mA
Standby Current	I <sub>SB</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		17	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 6mA, V <sub>CC</sub> = 4.5		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA, V <sub>CC</sub> = 4.5	2.4		V

NOTE: DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V

**LOW POWER DATA RETENTION CHARACTERISTICS (WMS256K16L-XXX ONLY)**

-55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Supply Voltage	V <sub>DR</sub>	CS# ≥ V <sub>CC</sub> - 0.2V	2.0		5.5	V
Data Retention Current	I <sub>CCDR</sub> <sup>1</sup>	V <sub>CC</sub> = 3V		1.0	8.0	mA



**AC CHARACTERISTICS**

$V_{CC} = 5.0V, GND = 0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol	-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle										
Read Cycle Time	$t_{RC}$	17		20		25		35		ns
Address Access Time	$t_{AA}$		17		20		25		35	ns
Output Hold from Address Change	$t_{OH}$	0		0		0		0		ns
Chip Select Access Time	$t_{ACS}$		17		20		25		35	ns
Output Enable to Output Valid	$t_{OE}$		10		12		15		20	ns
Chip Select to Output in Low Z	$t_{CLZ}^1$	2		5		5		5		ns
Output Enable to Output in Low Z	$t_{OLZ}^1$	0		0		0		0		ns
Chip Disable to Output in High Z	$t_{CHZ}^1$		9		10		12		15	ns
Output Disable to Output in High Z	$t_{OHZ}^1$		9		10		12		15	ns
LB#, UB# Access Time	$t_{BA}$		10		12		14		17	ns
LB#, UB# Enable to Low Z Output	$t_{BLZ}^1$	0		0		0		0		ns
LB#, UB# Disable to High Z Output	$t_{BHZ}^1$		9		10		12		15	ns

1. This parameter is guaranteed by design but not tested.

**AC CHARACTERISTICS**

$V_{CC} = 5.0V, GND = 0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol	-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle										
Write Cycle Time	$t_{WC}$	17		20		25		35		ns
Chip Select to End of Write	$t_{CW}$	14		17		20		25		ns
Address Valid to End of Write	$t_{AW}$	14		17		20		25		ns
Data Valid to End of Write	$t_{DW}$	10		12		15		20		ns
Write Pulse Width	$t_{WP}$	14		17		20		25		ns
Address Setup Time	$t_{AS}$	0		0		0		0		ns
Address Hold Time	$t_{AH}$	2		2		2		2		ns
Output Active from End of Write	$t_{OW}^1$	0		0		0		0		ns
Write Enable to Output in High Z	$t_{WHZ}^1$		9		10		10		15	ns
Data Hold Time	$t_{DH}$	0		0		0		0		ns
LB#, UB# Valid to End of Write	$t_{BW}$	14		17		20		25		ns

1. This parameter is guaranteed by design but not tested.

**AC TEST CIRCUIT**



**AC TEST CONDITIONS**

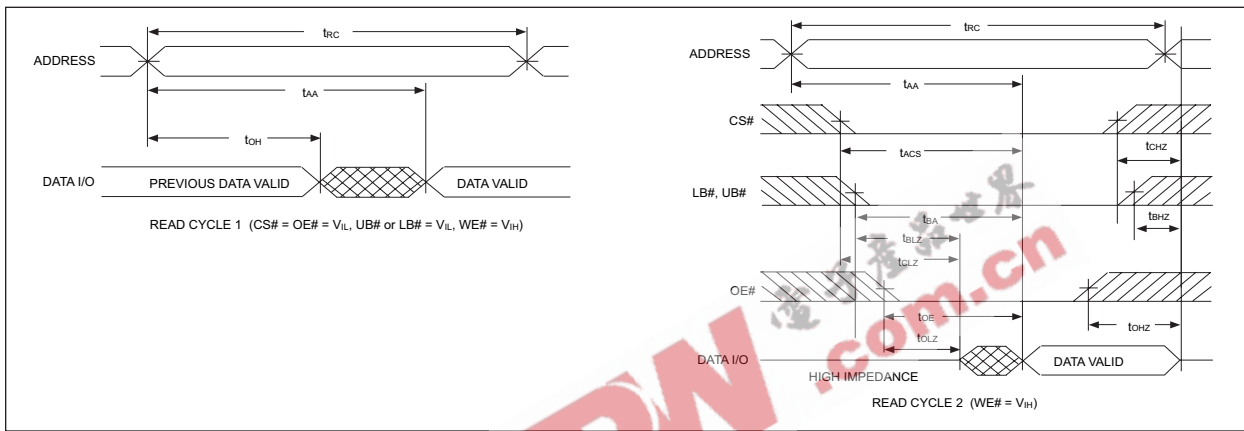
Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:

- $V_Z$  is programmable from -2V to +7V.
- $I_{OL}$  &  $I_{OH}$  programmable from 0 to 16mA.
- Tester Impedance  $Z_0 = 75 \Omega$ .
- $V_Z$  is typically the midpoint of  $V_{OH}$  and  $V_{OL}$ .
- $I_{OL}$  &  $I_{OH}$  are adjusted to simulate a typical resistive load circuit.
- ATE tester includes jig capacitance.



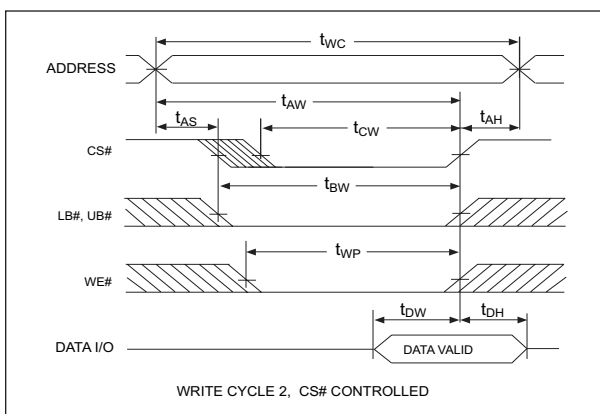
TIMING WAVEFORM - READ CYCLE



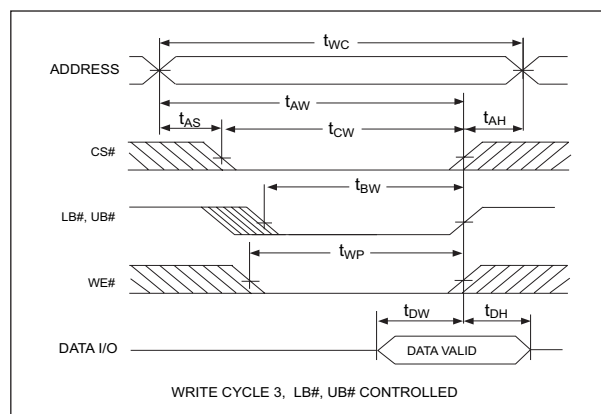
WRITE CYCLE - WE# CONTROLLED



WRITE CYCLE - CS# CONTROLLED



WRITE CYCLE - LB#, UB# CONTROLLED





PACKAGE 102: 44 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 225: 44 LEAD, CERAMIC FLAT PACK



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



**PACKAGE 211: 44 LEAD FORMED, CERAMIC FLAT PACK**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

**ORDERING INFORMATION**

**W M S 256K16 X - XXX X X X**

**LEAD FINISH:**

- Blank = Gold plated leads
- A = Solder dip leads

**DEVICE GRADE:**

- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

**PACKAGE:**

- DL = 44 Lead Ceramic SOJ (Package 102)
- FL = 44 Lead Ceramic Flatpack (Package 225)
- FG = 44 Lead Formed Ceramic Flatpack

**ACCESS TIME (ns)**

**IMPROVEMENT MARK:**

- Blank = Standard Power
- L = Low Power Data Retention

**ORGANIZATION, 256K x 16**

**SRAM**

**MONOLITHIC**

**WHITE ELECTRONIC DESIGNS CORP.**



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
256K x 16 SRAM Monolithic	35ns	44 lead SOJ (DL)	5962-96902 01HMX
256K x 16 SRAM Monolithic	25ns	44 lead SOJ (DL)	5962-96902 02HMX
256K x 16 SRAM Monolithic	20ns	44 lead SOJ (DL)	5962-96902 03HMX
256K x 16 SRAM Monolithic	17ns	44 lead SOJ (DL)	5962-96902 04HMX
256K x 16 SRAM Monolithic	35ns	44 lead Flatpack (FL)	5962-96902 01HNX
256K x 16 SRAM Monolithic	25ns	44 lead Flatpack (FL)	5962-96902 02HNX
256K x 16 SRAM Monolithic	20ns	44 lead Flatpack (FL)	5962-96902 03HNX
256K x 16 SRAM Monolithic	17ns	44 lead Flatpack (FL)	5962-96902 04HNX
256K x 16 SRAM Monolithic	35ns	44 lead Formed Flatpack (FG)	5962-96902 01HTX
256K x 16 SRAM Monolithic	25ns	44 lead Formed Flatpack (FG)	5962-96902 02HTX
256K x 16 SRAM Monolithic	20ns	44 lead Formed Flatpack (FG)	5962-96902 03HTX
256K x 16 SRAM Monolithic	17ns	44 lead Formed Flatpack (FG)	5962-96902 04HTX