



# 512Kx8 MONOLITHIC SRAM, SMD 5962-95613

## FEATURES

- Access Times 15, 17, 20, 25, 35, 45, 55ns
- MIL-STD-883 Compliant Devices Available
- Revolutionary, Center Power/Ground Pinout JEDEC Approved
  - 36 lead Ceramic SOJ (Package 100)
  - 36 lead Ceramic Flat Pack (Package 226)
- Evolutionary, Corner Power/Ground Pinout JEDEC Approved
  - 32 pin Ceramic DIP (Package 300)
  - 32 lead Ceramic SOJ (Package 101)
  - 32 lead Ceramic Flat Pack (Package 220)
  - 32 lead Ceramic Flat Pack (Package 142)
- 32 pin, Rectangular Ceramic Leadless Chip Carrier (Package 601)
- Commercial, Industrial and Military Temperature Range
- 5 Volt Power Supply
- Low Power CMOS
- Low Power Data Retention for Battery Back-up Operation
- TTL Compatible Inputs and Outputs

### REVOLUTIONARY PINOUT

36 FLAT PACK  
36 CSOJ

#### TOP VIEW



### EVOLUTIONARY PINOUT

32 DIP  
32 CSOJ (DE)  
32 FLAT PACK (FE)\*  
32 FLAT PACK (FD)

#### TOP VIEW



32 CLCC

#### TOP VIEW



### PIN DESCRIPTION

|        |                   |
|--------|-------------------|
| A0-18  | Address Inputs    |
| I/O0-7 | Data Input/Output |
| CS     | Chip Select       |
| OE     | Output Enable     |
| WE     | Write Enable      |
| Vcc    | +5.0V Power       |
| GND    | Ground            |

\*Package not recommended for new designs, "FD" recommended for new designs.



## ABSOLUTE MAXIMUM RATINGS

| Parameter                      | Symbol           | Min  | Max                  | Unit |
|--------------------------------|------------------|------|----------------------|------|
| Operating Temperature          | T <sub>A</sub>   | -55  | +125                 | °C   |
| Storage Temperature            | T <sub>STG</sub> | -65  | +150                 | °C   |
| Signal Voltage Relative to GND | V <sub>G</sub>   | -0.5 | V <sub>CC</sub> +0.5 | V    |
| Junction Temperature           | T <sub>J</sub>   |      | 150                  | °C   |
| Supply Voltage                 | V <sub>CC</sub>  | -0.5 | 7.0                  | V    |

## TRUTH TABLE

| CS | OE | WE | Mode        | Data I/O | Power   |
|----|----|----|-------------|----------|---------|
| H  | X  | X  | Standby     | High Z   | Standby |
| L  | L  | H  | Read        | Data Out | Active  |
| L  | X  | L  | Write       | Data In  | Active  |
| L  | H  | H  | Out Disable | High Z   | Active  |

## RECOMMENDED OPERATING CONDITIONS

| Parameter              | Symbol          | Min  | Max                   | Unit |
|------------------------|-----------------|------|-----------------------|------|
| Supply Voltage         | V <sub>CC</sub> | 4.5  | 5.5                   | V    |
| Input High Voltage     | V <sub>IH</sub> | 2.2  | V <sub>CC</sub> + 0.3 | V    |
| Input Low Voltage      | V <sub>IL</sub> | -0.3 | +0.8                  | V    |
| Operating Temp. (Mil.) | T <sub>A</sub>  | -55  | +125                  | °C   |

## CAPACITANCE

(T<sub>A</sub> = +25°C)

| Parameter          | Symbol           | Condition                         | Package                                     | Speed (ns)           | Max      | Unit     |
|--------------------|------------------|-----------------------------------|---|----------------------|----------|----------|
| Input capacitance  | C <sub>IN</sub>  | V <sub>IN</sub> = 0V, f = 1.0MHz  | 32 Pin CSOJ, DIP,<br>Flat Pack Evolutionary | 15 to 55             | 20       | pF       |
|                    |                  |                                   | 32 Pin CLCC                                 | 15 to 55             | 15       | pF       |
|                    |                  |                                   | 36 Pin CSOJ & Flat Pack<br>Revolutionary    | 15 to 35<br>45 to 55 | 12<br>20 | pF<br>pF |
| Output capacitance | C <sub>OUT</sub> | V <sub>OUT</sub> = 0V, f = 1.0MHz | 32 Pin CSOJ, DIP,<br>Flat Pack Evolutionary | 15 to 55             | 20       | pF       |
|                    |                  |                                   | 36 Pin CSOJ & Flat Pack<br>Revolutionary    | 15 to 35             | 12       | pF       |
|                    |                  |                                   |   | 45 to 55             | 20       | pF       |

This parameter is guaranteed by design but not tested.

## DC CHARACTERISTICS

(V<sub>CC</sub> = 5.0V, GND = 0V, T<sub>A</sub> = -55°C to +125°C)

| Parameter                 | Sym             | Conditions   | Min | Max | Units |
|---------------------------|-----------------|--|-----|-----|-------|
| Input Leakage Current     | I <sub>LI</sub> | V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>  |     | 10  | μA    |
| Output Leakage Current    | I <sub>LO</sub> | CS = V <sub>IH</sub> , OE = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>                  |     | 10  | μA    |
| Operating Supply Current* | I <sub>CC</sub> | CS = V <sub>IL</sub> , OE = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5                            |     | 160 | mA    |
| Standby Current           | I <sub>SB</sub> | CS = V <sub>IH</sub> , OE = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5                            |     | 15  | mA    |
| Output Low Voltage        | V <sub>OL</sub> | I <sub>OL</sub> = 8mA for 17 - 35ns,<br>I <sub>OL</sub> = 2.1mA for 45 - 55ns, V <sub>CC</sub> = 4.5     |     | 0.4 | V     |
| Output High Voltage       | V <sub>OH</sub> | I <sub>OH</sub> = -4.0mA for 17 - 35ns,<br>I <sub>OH</sub> = -1.0mA for 45 - 55ns, V <sub>CC</sub> = 4.5 | 2.4 |     | V     |

NOTE: DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V

\* Not 100% duty cycle

## DATA RETENTION CHARACTERISTICS FOR LOW POWER "L" VERSION

| Parameter                     | Symbol             | Conditions                  | Units |     |    |
|-------------------------------|--------------------|-----------------------------|-------|-----|----|
|                               |                    |                             | Min   | Max |    |
| Data Retention Supply Voltage | V <sub>DR</sub>    | CS ≥ V <sub>CC</sub> - 0.2V | 2.0   | 5.5 | V  |
| Low Power Data Retention      | I <sub>CCDR1</sub> | V <sub>CC</sub> = 3V        |       | 7   | mA |
| Low Power Data Retention      | I <sub>CCDR2</sub> | V <sub>CC</sub> = 2V        |       | 2   | mA |



## AC CHARACTERISTICS

(V<sub>CC</sub> = 5.0V, GND = 0V, T<sub>A</sub> = -55°C to +125°C)

| Parameter                          | Symbol                        | -15 |     | -17 |     | -20 |     | -25 |     | -35 |     | -45 |     | -55 |     | Units |
|------------------------------------|-------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-------|
|                                    |                               | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |       |
| Read Cycle Time                    | t <sub>RC</sub>               | 15  |     | 17  |     | 20  |     | 25  |     | 35  |     | 45  |     | 55  |     | ns    |
| Address Access Time                | t <sub>AA</sub>               |     | 15  |     | 17  |     | 20  |     | 25  |     | 35  |     | 45  |     | 55  | ns    |
| Output Hold from Address Change    | t <sub>OH</sub>               | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | ns    |
| Chip Select Access Time            | t <sub>ACS</sub>              |     | 15  |     | 17  |     | 20  |     | 25  |     | 35  |     | 45  |     | 55  | ns    |
| Output Enable to Output Valid      | t <sub>OE</sub>               |     | 8   |     | 9   |     | 10  |     | 12  |     | 25  |     | 25  |     | 25  | ns    |
| Chip Select to Output in Low Z     | t <sub>CLZ</sub> <sup>1</sup> | 2   |     | 2   |     | 2   |     | 2   |     | 4   |     | 4   |     | 4   |     | ns    |
| Output Enable to Output in Low Z   | t <sub>OLZ</sub> <sup>1</sup> | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | ns    |
| Chip Disable to Output in High Z   | t <sub>CHZ</sub> <sup>1</sup> |     | 8   |     | 9   |     | 10  |     | 12  |     | 15  |     | 20  |     | 20  | ns    |
| Output Disable to Output in High Z | t <sub>OHZ</sub> <sup>1</sup> |     | 8   |     | 9   |     | 10  |     | 12  |     | 15  |     | 20  |     | 20  | ns    |

1. This parameter is guaranteed by design but not tested.

## AC CHARACTERISTICS

(V<sub>CC</sub> = 5.0V, GND = 0V, T<sub>A</sub> = -55°C to +125°C)

| Parameter                        | Symbol                        | -15 |     | -17 |     | -20 |     | -25 |     | -35 |     | -45 |     | -55 |     | Units |
|----------------------------------|-------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-------|
|                                  |                               | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |       |
| Write Cycle Time                 | t <sub>WC</sub>               | 15  |     | 17  |     | 20  |     | 25  |     | 35  |     | 45  |     | 55  |     | ns    |
| Chip Select to End of Write      | t <sub>CW</sub>               | 13  |     | 14  |     | 14  |     | 15  |     | 25  |     | 35  |     | 50  |     | ns    |
| Address Valid to End of Write    | t <sub>AW</sub>               | 13  |     | 14  |     | 14  |     | 15  |     | 25  |     | 35  |     | 50  |     | ns    |
| Data Valid to End of Write       | t <sub>DW</sub>               | 8   |     | 9   |     | 10  |     | 10  |     | 20  |     | 25  |     | 25  |     | ns    |
| Write Pulse Width                | t <sub>WP</sub>               | 13  |     | 14  |     | 14  |     | 15  |     | 25  |     | 35  |     | 40  |     | ns    |
| Address Setup Time               | t <sub>AS</sub>               | 2   |     | 2   |     | 2   |     | 2   |     | 2   |     | 2   |     | 2   |     | ns    |
| Address Hold Time                | t <sub>AH</sub>               | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | 5   |     | 5   |     | ns    |
| Output Active from End of Write  | t <sub>OW</sub> <sup>1</sup>  | 2   |     | 2   |     | 3   |     | 4   |     | 4   |     | 5   |     | 5   |     | ns    |
| Write Enable to Output in High Z | t <sub>WHZ</sub> <sup>1</sup> |     | 8   |     | 9   |     | 9   |     | 10  |     | 15  |     | 20  |     | 25  | ns    |
| Data Hold Time                   | t <sub>DH</sub>               | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | 0   |     | ns    |

1. This parameter is guaranteed by design but not tested.

### AC TEST CIRCUIT



### AC TEST CONDITIONS

| Parameter                        | Typ  | Unit |
|----------------------------------|--|------|
| Input Pulse Levels               | V <sub>IL</sub> = 0, V <sub>IH</sub> = 3.0 | V    |
| Input Rise and Fall              | 5  | ns   |
| Input and Output Reference Level | 1.5  | V    |
| Output Timing Reference Level    | 1.5  | V    |

#### NOTES:

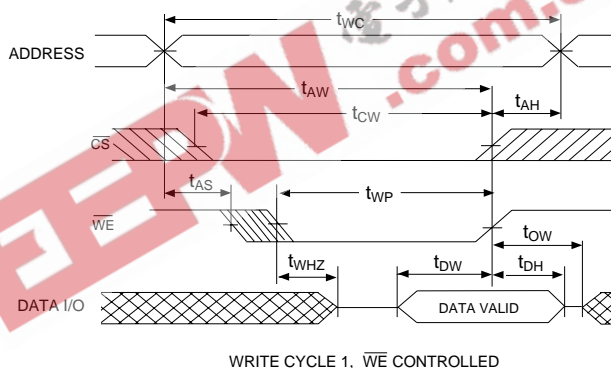
V<sub>Z</sub> is programmable from -2V to +7V.  
 I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.  
 Tester Impedance Z<sub>0</sub> = 75 Ω.  
 V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.  
 I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.  
 ATE tester includes jig capacitance.



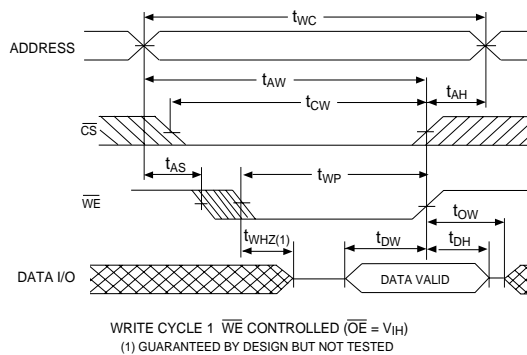
### TIMING WAVEFORM - READ CYCLE



### WRITE CYCLE - $\overline{WE}$ CONTROLLED



### WRITE CYCLE - $\overline{CS}$ CONTROLLED



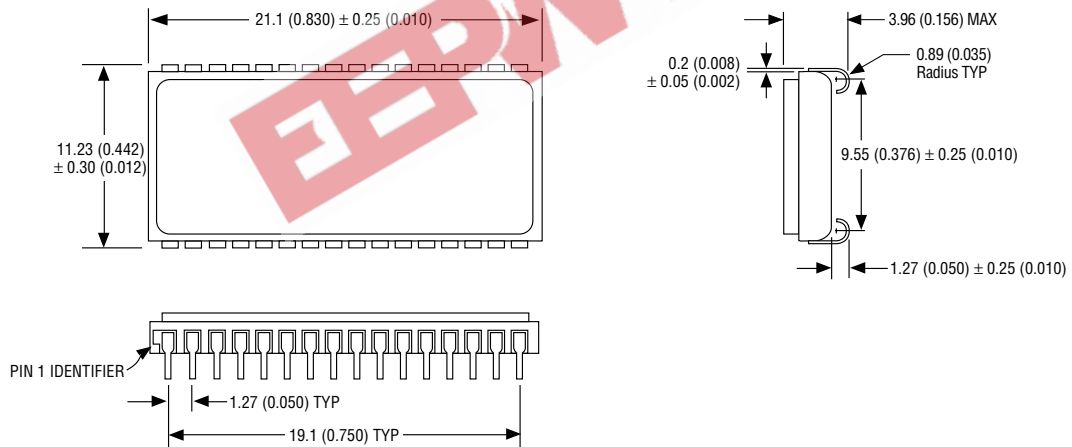


**PACKAGE 100: 36 LEAD, CERAMIC SOJ**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

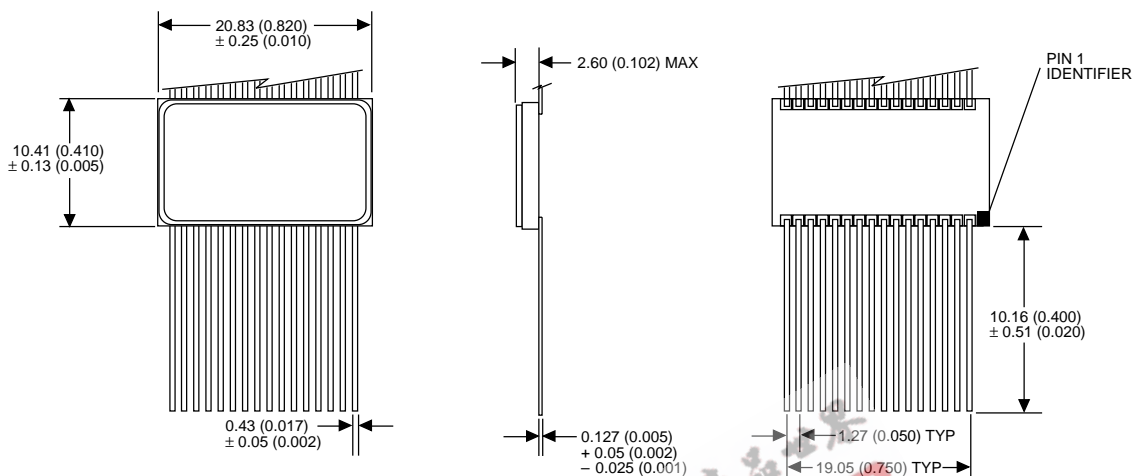
**PACKAGE 101: 32 LEAD, CERAMIC SOJ**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

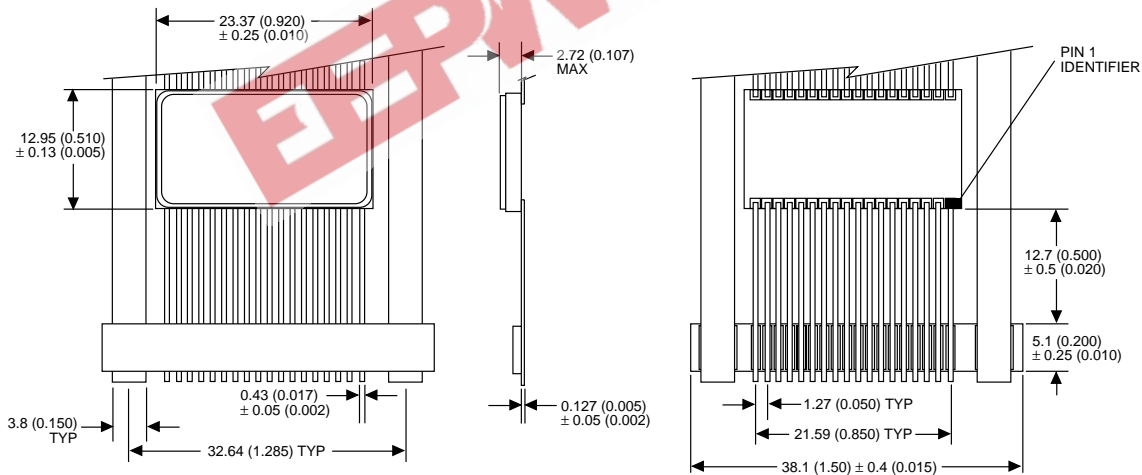


**PACKAGE 220: 32 LEAD, CERAMIC FLAT PACK**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

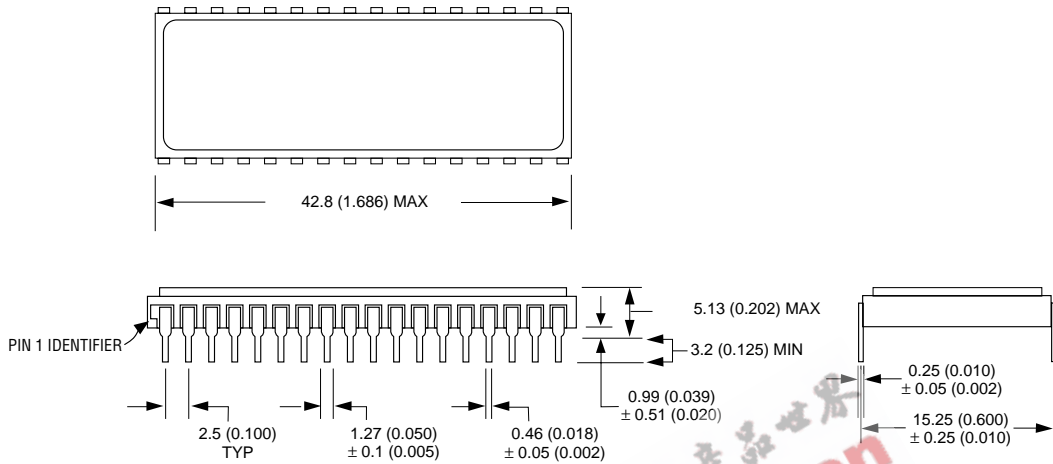
**PACKAGE 226: 36 LEAD, CERAMIC FLAT PACK**



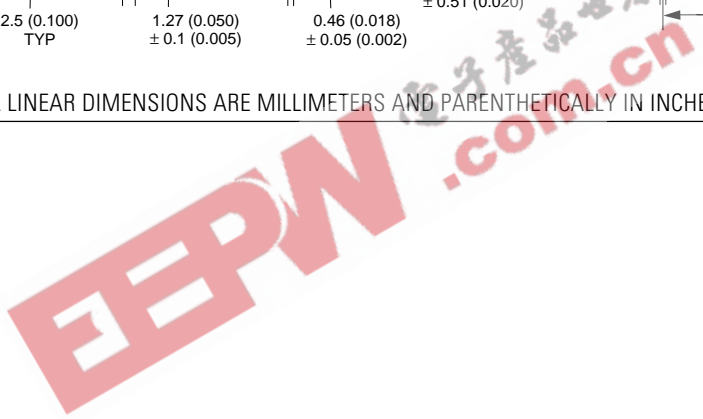
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



**PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES





**PACKAGE 601: 32 PIN, RECTANGULAR CERAMIC LEADLESS CHIP CARRIER**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES





ORDERING INFORMATION

W M S 512K 8 X - XXX X X X

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:

- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE:

- C = 32 Pin Ceramic 0.600" DIP (Package 300)
- CL = 32 Pin Rectangular Ceramic Leadless Chip Carrier (Package 601)
- DE = 32 Lead Ceramic SOJ (Package 101) Evolutionary
- DJ = 36 Lead Ceramic SOJ (Package 100)
- F = 36 Lead Ceramic Flat Pack (Package 226)
- FE = 32 Lead Ceramic Flat Pack (Package 220)

ACCESS TIME (ns)

IMPROVEMENT MARK:

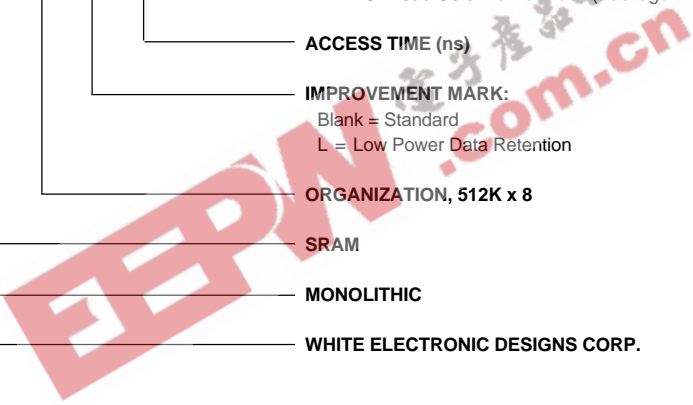
- Blank = Standard
- L = Low Power Data Retention

ORGANIZATION, 512K x 8

SRAM

MONOLITHIC

WHITE ELECTRONIC DESIGNS CORP.





| DEVICE TYPE              | SPEED | PACKAGE               | SMD NO.          |
|--------------------------|-------|-----------------------|------------------|
| 512K x 8 SRAM Monolithic | 55ns  | 32 pin DIP (C)        | 5962-95613 05HYX |
| 512K x 8 SRAM Monolithic | 45ns  | 32 pin DIP (C)        | 5962-95613 06HYX |
| 512K x 8 SRAM Monolithic | 35ns  | 32 pin DIP (C)        | 5962-95613 07HYX |
| 512K x 8 SRAM Monolithic | 25ns  | 32 pin DIP (C)        | 5962-95613 08HYX |
| 512K x 8 SRAM Monolithic | 20ns  | 32 pin DIP (C)        | 5962-95613 09HYX |
| 512K x 8 SRAM Monolithic | 17ns  | 32 pin DIP (C)        | 5962-95613 10HYX |
| 512K x 8 SRAM Monolithic | 15ns  | 32 pin DIP (C)        | 5962-95613 14HYX |
| 512K x 8 SRAM Monolithic | 55ns  | 32 lead SOJ Evol (DE) | 5962-95613 05HTX |
| 512K x 8 SRAM Monolithic | 45ns  | 32 lead SOJ Evol (DE) | 5962-95613 06HTX |
| 512K x 8 SRAM Monolithic | 35ns  | 32 lead SOJ Evol (DE) | 5962-95613 07HTX |
| 512K x 8 SRAM Monolithic | 25ns  | 32 lead SOJ Evol (DE) | 5962-95613 08HTX |
| 512K x 8 SRAM Monolithic | 20ns  | 32 lead SOJ Evol (DE) | 5962-95613 09HTX |
| 512K x 8 SRAM Monolithic | 17ns  | 32 lead SOJ Evol (DE) | 5962-95613 10HTX |
| 512K x 8 SRAM Monolithic | 15ns  | 32 lead SOJ Evol (DE) | 5962-95613 14HTX |
| 512K x 8 SRAM Monolithic | 55ns  | 36 lead SOJ (DJ)      | 5962-95613 05HZX |
| 512K x 8 SRAM Monolithic | 45ns  | 36 lead SOJ (DJ)      | 5962-95613 06HZX |
| 512K x 8 SRAM Monolithic | 35ns  | 36 lead SOJ (DJ)      | 5962-95613 07HZX |
| 512K x 8 SRAM Monolithic | 25ns  | 36 lead SOJ (DJ)      | 5962-95613 08HZX |
| 512K x 8 SRAM Monolithic | 20ns  | 36 lead SOJ (DJ)      | 5962-95613 09HZX |
| 512K x 8 SRAM Monolithic | 17ns  | 36 lead SOJ (DJ)      | 5962-95613 10HZX |
| 512K x 8 SRAM Monolithic | 15ns  | 36 lead SOJ (DJ)      | 5962-95613 14HZX |
| 512K x 8 SRAM Monolithic | 55ns  | 36 lead Flatpack (F)  | 5962-95613 05HXX |
| 512K x 8 SRAM Monolithic | 45ns  | 36 lead Flatpack (F)  | 5962-95613 06HXX |
| 512K x 8 SRAM Monolithic | 35ns  | 36 lead Flatpack (F)  | 5962-95613 07HXX |
| 512K x 8 SRAM Monolithic | 25ns  | 36 lead Flatpack (F)  | 5962-95613 08HXX |
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