WM9709

AC-link Interface Audio DAC

DESCRIPTION

The WM9709 is a low cost, high-quality stereo audio DAC. It utilises the Intel specified AC-link audio interface protocol, allowing a pair of audio output channels to be added to any AC link compliant controller device at minimal board area and external component cost.

The WM9709 device supports 48ks/s sample rates when operated at the normal AC link rate. The WM9709 supports a revision 1.03 AC '97 AC-link interface, the device acting as a master in normal operation.

The ID pin can be used to select which data slots on the AC-link are to be used as input to the DAC. This allows 3 x WM9709 to be used with a single controller that supports 6 channel sound, to output surround sound audio signals. When supporting surround, centre or LFE channels, the WM9709 behaves as a slave device.

The WM9709 device is footprint compatible with the WM9708 codec, allowing simple swapping between DAC and full codec features on the same board. The WM9709 is packaged in a 20-pin SSOP.

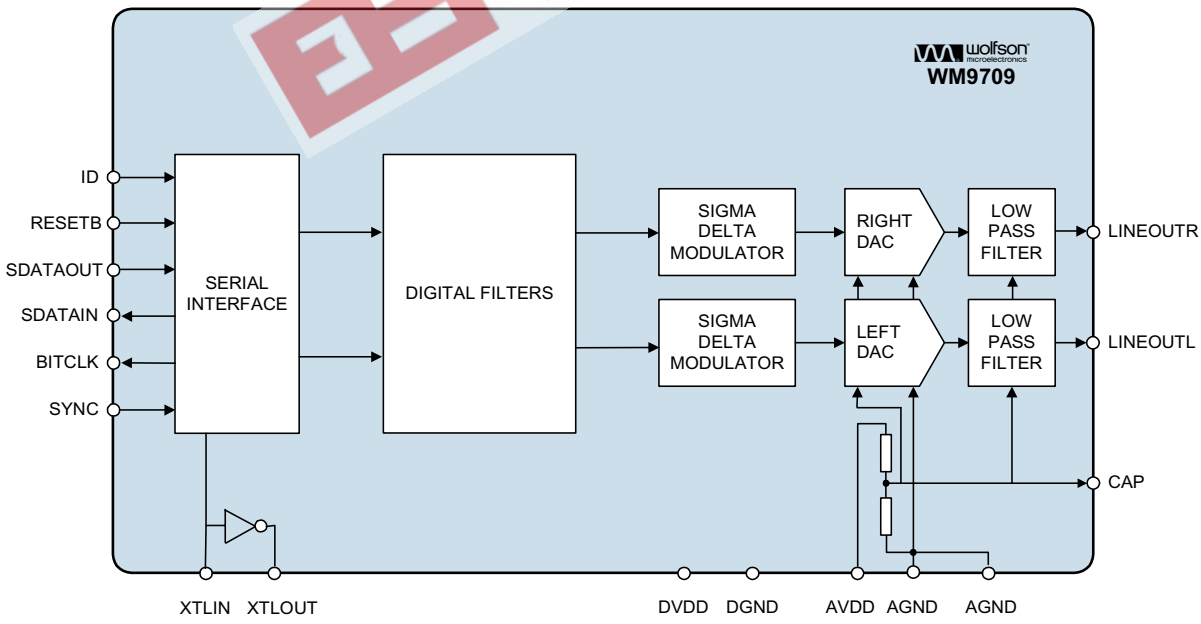
FEATURES

- 20-Bit Stereo DAC
- Audio Performance
  - 102dB SNR ('A' weighted at 48kHz)
  - -95dB THD
- Revision 1.03 or higher AC'97 AC-link interface support.
- 3.3V or mixed 3V digital, 5V analogue operation
- 20-Pin SSOP Package
- Minimal external component cost
- Support for surround and centre/LFE channels

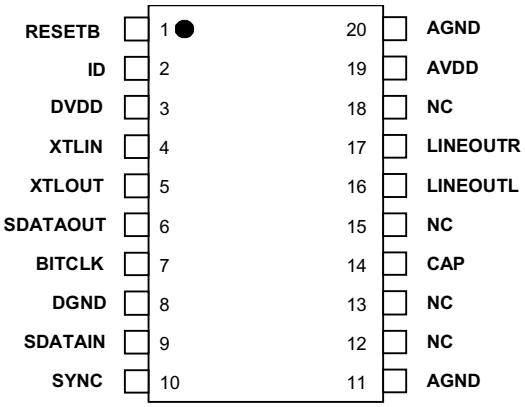
APPLICATIONS

- Notebook PC
- PC sound cards
- Motherboards
- Custom sound applications

BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM9709CDS	0° to 70°C	20-pin SSOP
WM9709CDS/R	0° to 70°C	20-pin SSOP Tape and Reel 330mm Reel 16mm wide tape 2000 units/reel

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	RESETB	Digital input	NOT reset input (active low, resets digital circuitry)
2	ID	Digital input	AC link Data slot select. Low = Normal stereo (slots 3,4), High = Surround (slots 7,8), High impedance (Z) = LFE and centre (slots 6,9)
3	DVDD	Supply	Digital positive supply
4	XTLIN	Digital input	Clock crystal connection or clock input (XTAL not used)
5	XTLOUT	Digital output	Clock crystal connection
6	SDATAOUT	Digital input	Serial data input
7	BITCLK	Digital output (master) Or digital input (slave)	Serial interface clock output to AC-link controller if ID pin held low (WM9709 is master). Serial interface clock input from AC-link master if ID pin held either high or high impedance (WM9709 is slave).
8	DGND	Supply	Digital ground supply
9	SDATAIN	Digital output	Serial data output to AC-link controller
10	SYNC	Digital input	Serial interface sync pulse from AC-link controller
11	AGND	Supply	Analogue ground supply, chip substrate
12	NC		No internal connection
13	NC		No internal connection
14	CAP	Analogue input	Reference input/output; internal divider generates midrail
15	NC		No internal connection
16	LINEOUTL	Analogue output	Main analogue output for left channel
17	LINEOUTR	Analogue output	Main analogue output for right channel
18	NC		No internal connection
19	AVDD	Supply	Analogue positive supply
20	AGND	Supply	Analogue ground supply, chip substrate

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+7V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T_A	0°C	+70°C
Storage temperature prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65°C	+150°C
Package body temperature (soldering, 10 seconds)		+240°C
Package body temperature (soldering, 2 minutes)		+183°C

DC ELECTRICAL CHARACTERISTICS

Test Conditions:
AVDD = 5V, AGND = 0V, DVDD = 3.3V, DGND = 0V, T_A = 25°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Ranges						
Digital supply range	DVDD		-10%	3.3	+10%	V
Analogue supply range	AVDD		-10%	3.3 to 5.0	+10%	V
Digital ground	DGND			0		V
Analogue ground	AGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V
Supply Currents						
Analogue supply current		DVDD=3.3V, AVDD = 5V		12.5	20	mA
Analogue supply current		DVDD, AVDD = 3.3V		11		mA
Digital supply current		DVDD, AVDD = 3.3V		5	8	mA
Digital Logic Levels (DVDD = 3.3)						
Input LOW level	V_{IL}		DGND - 0.3		0.25 * DVDD	V
Input HIGH level	V_{IH}		0.75 * DVDD		DVDD + 0.3	V
Output LOW	V_{OL}	ILOAD = 1mA			0.1 * DVDD	V
Output HIGH	V_{OH}	ILOAD = 1mA	0.9 * DVDD			V

AC ELECTRICAL CHARACTERISTICS

Test Conditions:
AVDD = 5V, AGND = 0V, DVDD = 3.3V, DGND = 0V, T_A = 25°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference Levels						
Reference input/output	CAP		AVDD/2 – 25mV	AVDD/2	AVDD/2 + 25mV	
CAP impedance				5		kΩ
DAC Circuit Specifications (48kHz Sample Rate)						
SNR A-weighted (Note 1,2)		AVDD = 5V	95	102		dB
		AVDD = 3.3V		99		dB
Dynamic Range	DNR	AVDD = 5V	95	102		dB
		AVDD = 3.3V		99		dB
Full scale output voltage into 10kΩ load		AVDD=5V	0.95	1.0	1.05	Vrms
		AVDD=3.3V		0.66		Vrms
THD		0dBfs		-95	-85	dB
Channel Separation			95	102		dB
Channel Matching			-0.35	0	0.35	dB
PSRR		1kHz, 10µF on CAP pin		46		dB
Output offset wrt CAP voltage			-30	0	30	mV
Clock Frequency Range						
Crystal clock				24.576		MHz
BITCLK frequency				12.288		MHz
SYNC frequency				48.0		kHz

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20Hz to 20kHz bandwidth.
2. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. SNR measured with A-weight filter is typically 2dB better than with CCIR2k filter, or 20kHz low pass filter.

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
3. Dynamic range (dB) - DNR is a measure of the ratio between the largest and smallest usable signals. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= 42dB, DNR= 102dB).
4. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.

SERIAL INTERFACE TIMINGS

Test Conditions:
AVDD = 5V, AGND = 0V, DVDD = 3.3V, DGND = 0V, TA = 25°C, unless otherwise stated. All measurements are taken at 10% to 90% VDD, unless otherwise stated.

All the following timing information is guaranteed by design, but not tested in production.

COLD RESET

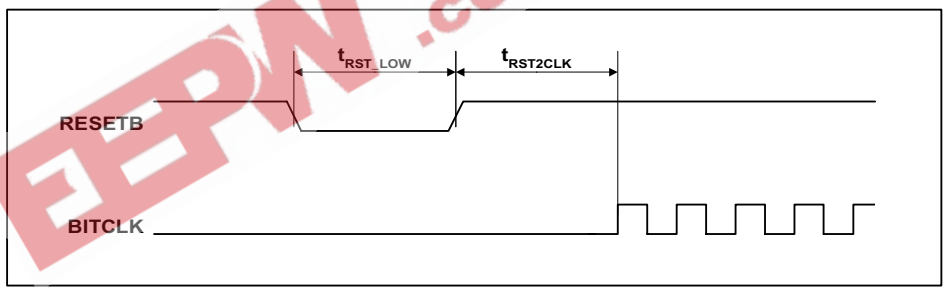


Figure 1 Cold Reset Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
RESETB active low pulse width	t_{RST_LOW}	1.0			µs
RESETB inactive to BITCLK startup delay	$t_{RST2CLK}$	162.8			ns

WARM RESET

Not supported by WM9709

CLOCK SPECIFICATIONS

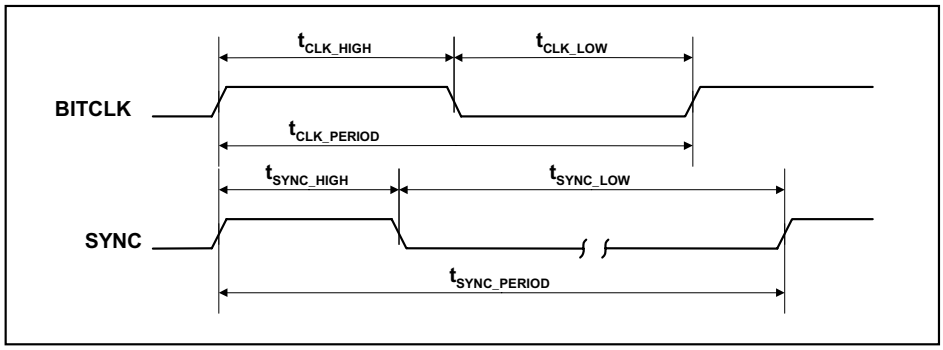


Figure 2 Clock Specifications (50pF External Load)

Note: Worst case duty cycle restricted to 40/60.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BITCLK frequency			12.288		MHz
BITCLK period	t_{CLK_PERIOD}		81.4		ns
BITCLK output jitter				750	ps
BITCLK high pulse width	t_{CLK_HIGH}	32.56	40.7	48.84	ns
BITCLK low pulse width	t_{CLK_LOW}	32.56	40.7	48.84	ns
SYNC frequency			48.0		kHz
SYNC period	t_{SYNC_PERIOD}		20.8		µs
SYNC high pulse width	t_{SYNC_HIGH}		1.3		µs
SYNC low pulse width	t_{SYNC_LOW}		19.5		µs

DATA OUTPUT AND INPUT TIMES

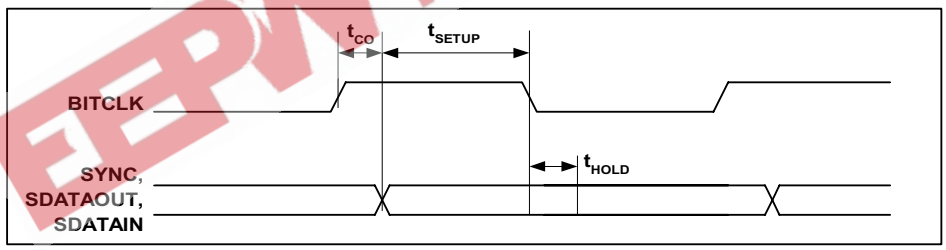


Figure 3 Data Output and Input Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Setup to falling edge of BITCLK	t_{SETUP}	10.0			ns
Hold from falling edge of BITCLK	t_{HOLD}	10.0			ns
Output Valid Delay from rising edge of BITCLK	t_{CO}			15.0	ns

ATE IN CIRCUIT TEST MODE

When the WM9709 is placed in the ATE test mode, its digital AC-link outputs (BITCLK and SDATAIN) are driven to a high impedance state. This allows ATE in circuit testing of the WM9709.

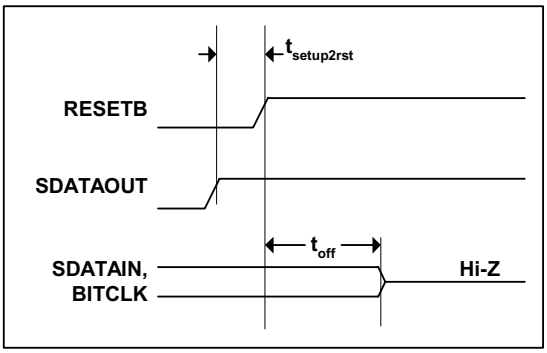


Figure 4 ATE Test Mode Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Setup to trailing edge of RESETB (also applies to SYNC)	$T_{setup2rst}$	15.0	-	-	nS
Rising edge of RESETB to Hi-Z delay	T_{off}	-	-	25.0	nS

Notes:

1. All WM9709 signals are normally low through the trailing edge of RESETB. Bringing SDATAOUT high for the trailing edge of RESETB causes WM9709's AC-link outputs to go high impedance, which is suitable for ATE in circuit testing.
2. A vendor specific internal test mode can be entered by bringing SYNC high for the trailing edge of RESETB. This mode has no effect on WM9709 AC-link output signal levels.
3. Once either of the two test modes have been entered, WM9709 must be issued another RESETB with all AC-link signals low to return to the normal operating mode.

SIGNAL RISE AND FALL TIMES

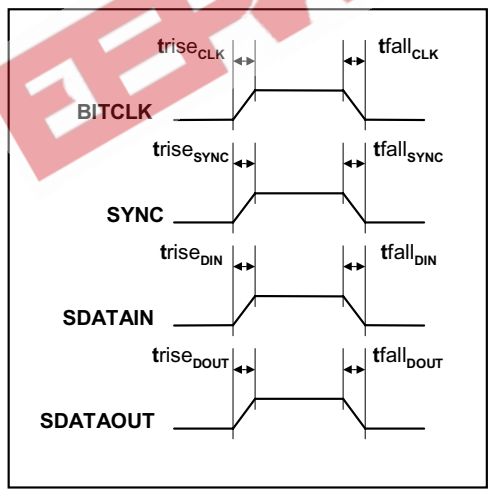


Figure 5 Signal Rise and Fall Times (50pF external load)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BITCLK rise time	$trise_{CLK}$	2		6	ns
BITCLK fall time	$tfall_{CLK}$	2		6	ns
SYNC rise time	$trise_{SYNC}$	2		6	ns
SYNC fall time	$tfall_{SYNC}$	2		6	ns
SDATAIN rise time	$trise_{DIN}$	2		6	ns
SDATAIN fall time	$trise_{DIN}$	2		6	ns
SDATAOUT rise time	$trise_{DOUT}$	2		6	ns
SDATAOUT fall time	$tfall_{DOUT}$	2		6	ns

DIGITAL FILTER RESPONSE

The WM9709 digital filter response is guaranteed by design but is not tested in production.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband		±0.05 dB	0.444fs			dB
Stopband		-3dB		0.487fs		
Passband ripple				±0.05		dB
Stopband Attenuation		f > 0.555fs			-60	dB

TERMINOLOGY

1. Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside the audio band).
2. Pass-Band Ripple - Any variation of the frequency response in the pass-band region.

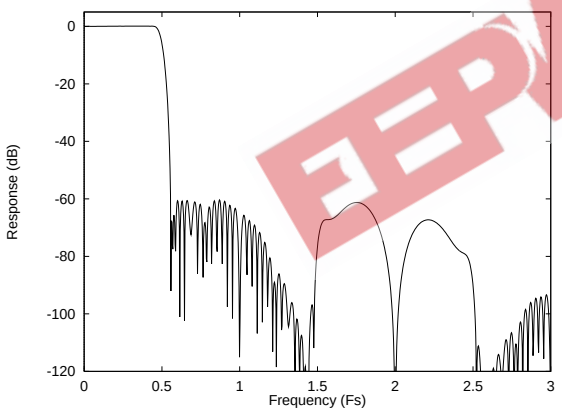


Figure 6 Digital Filter Frequency Response – 48kHz

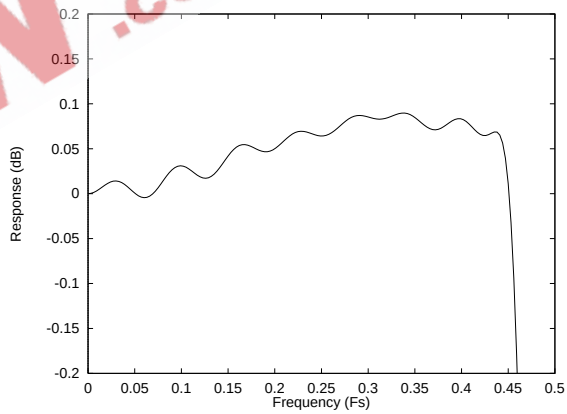


Figure 7 Digital Filter Ripple – 48kHz

DEVICE DESCRIPTION

INTRODUCTION

WM9709 contains a minimal subset of a revision 1.03 AC'97 compliant audio codec.

WM9709 comprises a stereo 20-bit DAC and an Intel revision 1.03 AC-link compatible interface. No internal volume control stages, mute function or power down registers are provided. Vendor ID data may be read back from registers 7C and 7E. The SDATAIN output pin is used for outputting digital signals during manufacturing test, but does not output signals in normal operation.

The DACs on WM9709 are implemented using a multi-bit switched capacitor sigma delta architecture which gives inherently low out of band noise and reduced clock jitter sensitivity.

An internally generated mid-rail reference is provided at pin CAP which is used as the chip reference. This pin should be heavily de-coupled. See Figure 11.

CONTROL AND DATA INTERFACE

A digital interface to control and transfer to and from the WM9709 has been provided. This serial interface is compatible with the Intel revision 1.03 AC-link specification.

The main control interface functions are:

- Transfer of DAC words from AC-link controller.
- Control of test modes.
- Readback of vendor ID.

AC-LINK DIGITAL SERIAL INTERFACE PROTOCOL

WM9709 incorporates a 5 pin digital serial interface that links it to the AC-link controller. The AC-link is a bi-directional, fixed rate, serial PCM digital stream. It handles multiple input, and output audio streams, as well as control register accesses employing a time division multiplexed (TDM) scheme. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution. WM9709 provides support for up to 20-bit operation of outgoing DAC data only. No incoming data is provided other than readback of vendor ID. A read request to any address other than 7C or 7E will respond with all 0s.

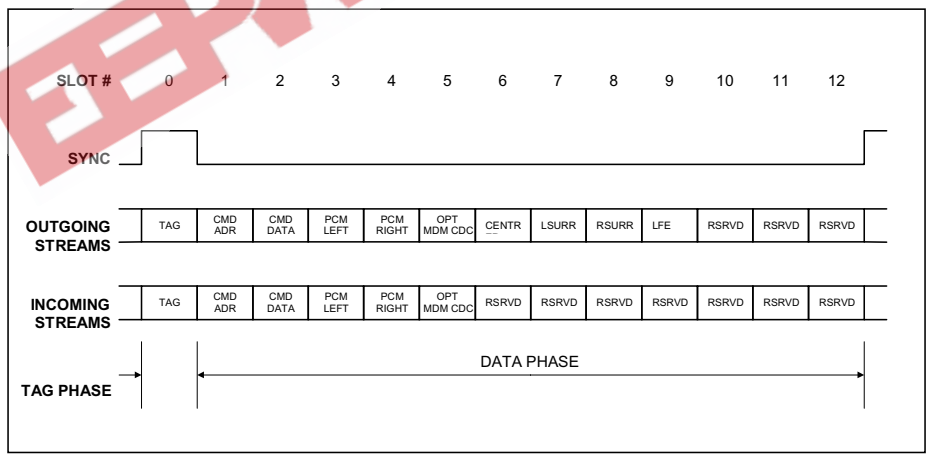


Figure 8 AC-link Standard Bi-directional Audio Frame

Synchronisation of all AC-link data transactions is signaled by the WM9709 controller. When WM9709 operates as a master (ID = 'lo', normal operation) WM9709 drives the serial bit clock BITCLK onto the AC-link, which the AC-link controller then qualifies with a synchronisation signal to construct audio frames. When a multi channel system is implemented using 2 or 3 WM9709 or other AC'97 devices, one of the AC link devices MUST be a master. Other WM9709 devices used as surround or centre/LFE channel devices (by selecting ID = high or 'Z') act as slaves. In this case BITCLK is an input. The system clock is not required for slave devices, which use BITCLK for all internal functions. The BITCLK input is used for all internal filtering operations.

SYNC is fixed at 48 kHz, and is derived by the AC-link controller which divides down the serial clock (BITCLK). BITCLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots. AC-link serial data is transitioned on each rising edge of BITCLK. The receiver of AC-link data, (WM9709 for SDATAOUT data), samples each serial bit on the falling edges of BITCLK.

The AC-link protocol provides for a special 16-bit time slot (slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A '1' in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is "tagged" invalid, WM9709 will ignore the corresponding data slot.

SYNC remains high for a total duration of 16 BITCLKs at the beginning of each audio frame.

The portion of the audio frame where SYNC is high is defined as the "Tag Phase". The remainder of the audio frame where SYNC is low is defined as the "Data Phase". Additionally, for power savings, all clock, sync, and data signals can be halted.

AC-LINK AUDIO OUTPUT FRAME (SDATAOUT)

SDATAOUT, the audio frame data input to the WM9709, contains audio and control data time multiplexed onto one bus. As briefly mentioned earlier, each audio output frame supports up to 12, 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16-bits, which are used for AC-link protocol infrastructure.

The first bit within slot 0 is a global bit (SDATAOUT slot 0, bit 15) which flags the validity for the entire audio frame. If the "Valid Frame" bit is a 1, this indicates that the current audio frame contains at least one time slot of valid data. The next 12-bit positions sampled by the WM9709 indicate which of the corresponding 12 time slots contain valid data.

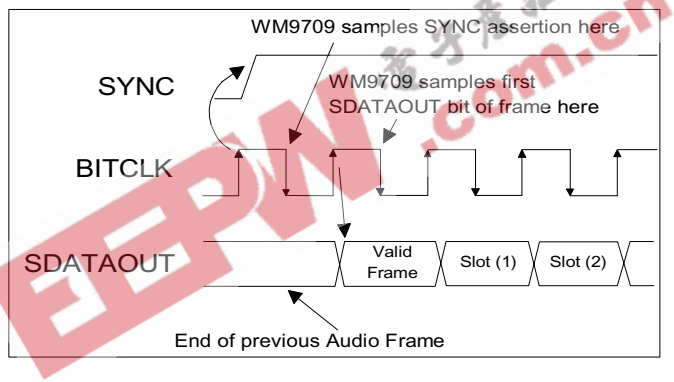


Figure 9 Start of an Audio Output Frame

A new audio output frame begins with a low to high transition of SYNC as shown in Figure 7. SYNC is synchronous to the rising edge of BITCLK. On the immediately following falling edge of BITCLK, WM9709 samples the assertion of SYNC. This falling edge marks the time when both sides of the AC-link are aware of the start of a new audio frame. On the next rising edge of BITCLK, the AC-link controller transitions SDATAOUT into the first bit position of slot 0 ("Valid Frame" bit). Each new bit position is presented to AC-link on a rising edge of BITCLK, and subsequently sampled by the WM9709 on the following falling edge of BITCLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

Baseline AC'97 specified audio functionality MUST ALWAYS sample rate convert to and from a fixed 48 kS/s on the AC'97 controller.

This requirement is necessary to ensure that interoperability between the AC-link controller and WM9709 can be guaranteed by definition for baseline specified AC'97 features.

SDATAOUT's composite stream is MSB justified (MSB first) with all non-valid slot bit positions stuffed with 0s by the AC-link controller.

As an example, consider an 8-bit sample stream that is being played out to one of WM9709's DACs. The first 8-bit positions are presented to the DAC (MSB justified) followed by the next 12-bit-positions, which are stuffed with 0s by the AC-link controller. This ensures that regardless of the resolution of the implemented DAC (16, 18 or 20-bit), the least significant bits will introduce no DC biasing.

When mono audio sample streams are output from the AC-link controller, it is necessary that BOTH left and right sample stream time slots be filled with the same data.

SLOT 1: COMMAND ADDRESS PORT

Bit(19)	Read/write command (1 = read, 0 = write)
Bit(18:12)	Control register index (64 16-bit locations, addressed on even byte boundaries)
Bit(11:0)	Reserved (stuffed with 0s)

The first bit (MSB) sampled by WM9709 indicates whether the current control transaction is a read or write operation. The following 7 bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are reserved and must be stuffed with 0s by the AC-link controller.

In the case of the WM9709, read mode is required only to access the vendor ID register

SLOT 2: COMMAND DATA PORT

The Slot 2 command data port is not normally used by WM9709.

SLOTS 3 & 4: PCM PLAYBACK LEFT & RIGHT CHANNELS

Audio output frame slots 3 & 4 are the composite digital audio left and right playback streams. In a typical 'Games Compatible' PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC-link controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC-link controller must stuff all trailing non-valid bit positions within this time slot with 0s. When WM9709 pin 2 (ID) is held low, data from slots 3 & 4 is mapped onto the DAC inputs.

SLOTS 5: OPTIONAL MODEM LINE CODEC

Audio output frame slot 5 would typically contain the MSB justified modem DAC input data. This optional AC'97 feature is not supported in WM9709, and data is ignored if written to this location.

SLOTS 6 & 9: PCM PLAYBACK CENTRE AND LFE CHANNELS

Audio data corresponding to surround centre and LFE channels is contained in slots 6 & 9. When pin 2 (ID) is left high impedance (not driven), data from these slots is mapped onto the DAC inputs. In this mode BITCLK is an input from the AC-link MASTER.

SLOTS 7 & 8: PCM PLAYBACK SURROUND LEFT & RIGHT CHANNELS

Audio data corresponding to surround left and right channels is contained in slots 7 & 8. When pin 2 (ID) is pulled high, data from these slots is mapped onto the DAC inputs. In this mode BITCLK is an input from the AC-link MASTER.

AC-LINK AUDIO INPUT FRAME (SDATAIN)

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC-link controller. As is the case for an audio output frame, each AC-link audio input frame consists of 12, 20-bit time slots. The WM9709 supports a reduced set of these audio input frames, specifically slots 0,1 and 2.

The first bit within slot 0 is a global bit (SDATAIN slot 0, bit 15) which flags whether WM9709 is in the "DAC Ready" state or not. If the "DAC Ready" bit is a 0, this indicates that WM9709 is not ready for normal operation. When the AC-link "DAC Ready" indicator bit is a 1, it indicates that the AC-link and WM9709 control and status registers are in a fully operational state.

Once WM9709 is sampled "DAC Ready" then the next 12 bit positions sampled by the AC-link controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data. Figure 8 illustrates the time slot based AC-link protocol.

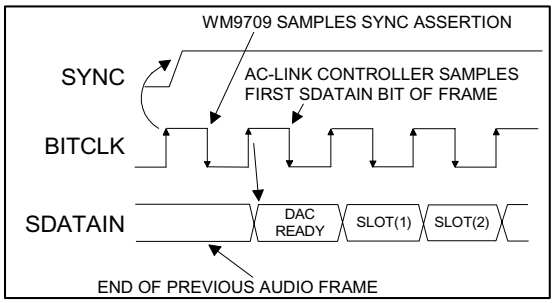


Figure 10 Start of an Audio Input Frame

SDATAIN's composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with 0's by the WM9709. SDATAIN is sampled on the falling edges of BITCLK.

SLOT 1: STATUS ADDRESS PORT

Audio input frame slot 1 echoes the control register index from the read request, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged "valid" by WM9709 during slot 0).

STATUS ADDRESS PORT BIT ASSIGNMENTS:

Bit(19)	RESERVED (stuffed with 0s)
Bit(18:12)	Control register index (echo of register index for which data is being returned)
Bit(11:0)	RESERVED (stuffed with 0s)

The first bit (MSB) generated by WM9709 is always stuffed with a 0. The following 7 bit positions communicate the associated control register address, and the trailing 12-bit positions are stuffed with 0s by WM9709

SLOT 2: STATUS DATA PORT

The status data port delivers 16-bit control register read data.

Bit(19:4)	Control register read data (stuffed with 0s if tagged "invalid" by WM9709)
Bit(3:0)	RESERVED (stuffed with 0s)

If slot 2 is tagged "invalid" by WM9709, then the entire slot will be stuffed with 0s.

The WM9709 will use this port only to return the data value of the vendor ID.

SLOTS 3-12: UNUSED

The remaining slots in the audio input frame are not used by the WM9709. All bits in these slots will be stuffed with 0s.

AC-LINK LOW POWER MODE

Not supported by WM9709

SERIAL INTERFACE REGISTER MAP DESCRIPTION

See Table 1.

Only special production test modes and vendor ID readback are supported by the WM9709 register map. The test mode addresses are chosen to avoid conflict with any data that might be written to normal AC'97 register addresses.

None of the typical AC'97 mixer, control, power up/down control functions are supported by the WM9709.

VENDOR RESERVED REGISTER (INDEX 5AH)

This register is reserved for future use and is vendor specific. Do not write to these registers unless the Vendor ID register has been checked first to ensure that the driver knows the source of the AC'97 component. Values stored in this register are used to provide test modes for the manufacturer.

VENDOR ID REGISTERS (INDEX 7Ch - 7Eh)

This register is for specific vendor identification if so desired. The ID method is Microsoft's Plug and Play Vendor ID code. The first character of that ID is F7 to F0, the second character S7 to S0 and the third T7 to T0. These three characters are ASCII encoded. The REV7 to REV0 field is for the Vendor Revision number. In the WM9709, the vendor ID is set to WML9.

SERIAL INTERFACE REGISTER MAP

The following table shows the function and address of the various control bits that are loaded through the serial interface during write operations.

Reg. Num.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
5Ah	Vendor Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	574D
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV 7	REV 6	REV 5	REV 4	REV 3	REV 2	REV 1	REV 0	4CO9

Table 1 Serial Interface Register Map Description

RECOMMENDED EXTERNAL COMPONENTS

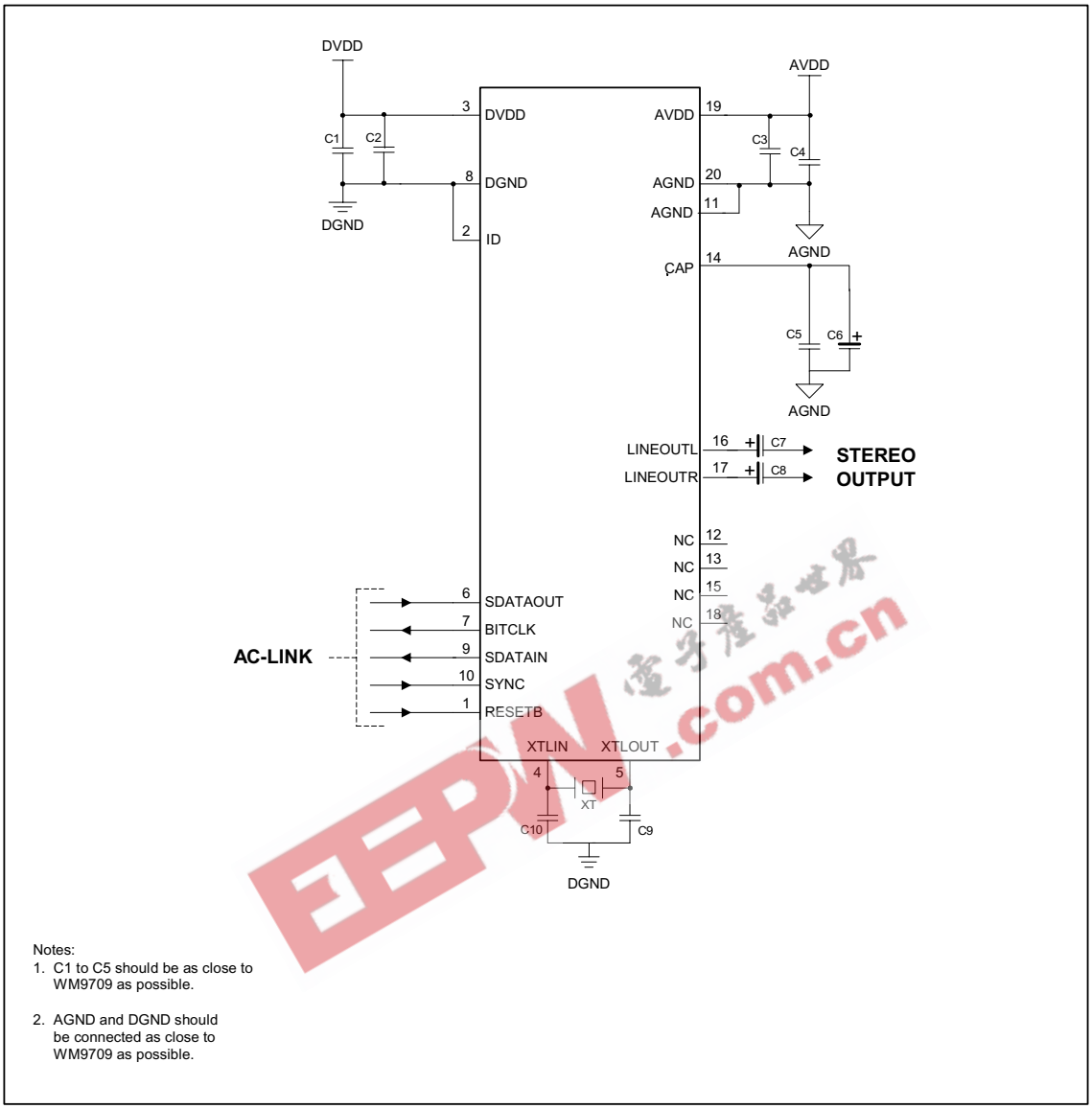


Figure 11 External Components Diagram

RECOMMENDED EXTERNAL COMPONENT VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1 to C4	0.1µF + 1uF	De-coupling for DVDD and AVDD
C5	0.1µF	Reference de-coupling capacitors for DAC
C6	10µF	
C7 to C8	10µF	Output AC coupling caps to remove VREF DC level from outputs.
C9 and C10	22pF	Optional capacitors for better crystal frequency stability.
XT	24.576 MHz	WM9709 master clock frequency. A bias resistor is not required, but if connected will not affect operation if value is large (above 1MΩ).

Table 2 External Component Recommendations

RECOMMENDATIONS FOR 3.3V OPERATION

The WM9709 device performance with AVDD = 3.3V is shown in Electrical Characteristics.

The mid-rail reference is set to AVDD/2. The analogue full-scale output signal is 1Vrms centred at midrail for AVDD=5V. For AVDD=3.3V, the full-scale output is 660mV rms. If 1Vrms output is required, external gain must be increased.

RECOMMENDATIONS FOR EXTERNAL FILTER

For undemanding applications, the output from WM9709 may be used without an external buffer. Typically a simple AC coupling cap of suitable value is used to remove the midrail DC pedestal from the audio signal, with a simple RC filter used to both protect the DAC and remove any residual high frequency RF noise which might appear at the outputs. An RC combination of series 1k resistor and 3.9nF to ground would suffice, and the resulting output impedance of 1k ohm is likely to be acceptable in many applications.

In more demanding applications, such as DVD playback, more filtering and a lower output impedance are often required. Due to the use of a low order sigma delta modulator on WM9709, a second order filter may suffice. Additional filtering may not result in any significant noise reduction. This filter is normally implemented using an active stage, which can then be used to perform the function of increasing the output amplitude of the signal from the WM9709 from typically 1Vrms to the 2Vrms often specified for consumer digital audio equipment. Figure 12 shows an example of a typical 2nd order filter and buffer circuit that might be used. In this case the AC coupling capacitor that would typically be placed between the DAC output and the filter input has been removed in order that the DAC pedestal from the output of the DAC is maintained. This allows use of a single supply opamp, removing the need for a negative supply in the audio subsystem. The output signals now swing around the DC pedestal, the DC offset being removed by the AC coupling capacitor at the filter output.

RECOMMENDATIONS FOR MINIMISING POWER UP/DOWN 'CLICKS'

Removal of power up/down clicks is typically required in consumer electronic equipment. The WM9709 is designed to minimise the start-up and shut down 'click' when power is applied or removed or when the device is switched into or out of its reset mode of operation (RESETB state is changed).

However, because the WM9709 DAC is followed typically by an active filter, power on/off clicks may still occur if this filter circuit is not carefully designed, and/or some form of 'clamp' or 'mute' circuit is not used at the output.

There are two primary concerns when attempting to minimise 'clicks'; one is the issue of charging the AC coupling capacitor in a controlled way and avoiding transients as the DC is established across it. The other is avoiding 'clicks' when the output op-amp is powered up or down.

The first point of charging the capacitor is addressed by providing a control pin to allow the DC at the DAC output to be ramped up or down by tying the DAC output to the CAP pin. This allows the user to choose the external capacitor value to set the time constant. This can minimise the resultant output transient, but it does this by giving it sub-audio characteristics, which may still cause problems in some systems.

The second point of powering up and down the output stage opamp may or may not generate significant 'clicks' depending on how the chosen opamp behaves at this time. Many opamps will exhibit gain inversion when their supply is taken very low. At that point the output typically flips up to the positive supply rail generating a significant output spike. If the choice of filter opamp is based on it being well behaved under these conditions, a non-economic component choice may have to be made.

It is recommended therefore that the whole problem be removed by use of a clamp or mute transistor on the output of each channel, the transistor being turned on at start-up and shut down when required.

The device could be either an appropriate series MOSFET in the signal line, or alternatively a bipolar transistor that clamps the output to ground when the supplies are not stable. Typically low VCESAT transistors are chosen for this function in order to minimise residual DC voltage across the clamp device. The base or gate drive to this device will typically be the OR combination of power supply indicator signals and mute signals from the digital controller. This allows the mute to be applied for example in the case of damaged discs which would otherwise have caused audible noise.

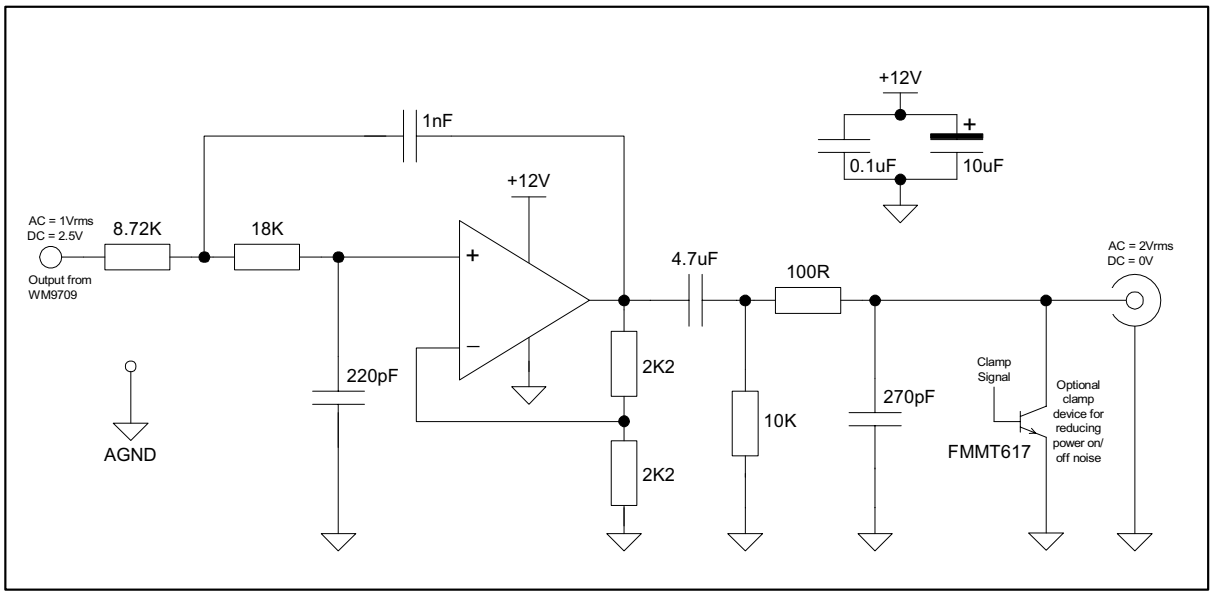
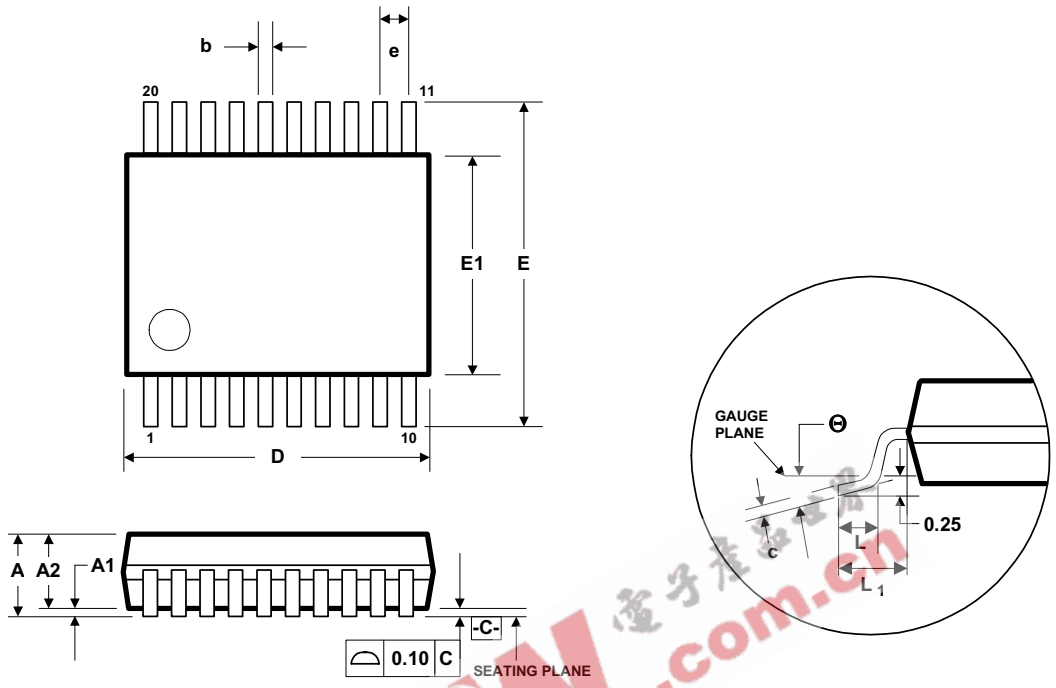


Figure 12 Typical External Filter and Components

PACKAGE DIMENSIONS

DS: 20 PIN SSOP (7.2 x 5.3 x 1.75 mm) **DM0015.B**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	2.0
A_1	0.05	-----	-----
A_2	1.65	1.75	1.85
b	0.22	0.30	0.38
c	0.09	-----	0.25
D	6.90	7.20	7.50
e		0.65 BSC	
E	7.40	7.80	8.20
E_1	5.00	5.30	5.60
L	0.55	0.75	0.95
L_1		0.125 REF	
θ	0^o	4^o	8^o
REF:	JEDEC.95, MO-150		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
D. MEETS JEDEC.95 MO-150, VARIATION = AE. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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