



512Kx8 MONOLITHIC SRAM, SMD 5962-95613

FEATURES

- Access Times 15, 17, 20, 25, 35, 45, 55ns
- MIL-STD-883 Compliant Devices Available
- Revolutionary, Center Power/Ground Pinout JEDEC Approved
 - 36 lead Ceramic SOJ (Package 100)
 - 36 lead Ceramic Flat Pack (Package 226)
- Evolutionary, Corner Power/Ground Pinout JEDEC Approved
 - 32 pin Ceramic DIP (Package 300)
 - 32 lead Ceramic SOJ (Package 101)
 - 32 lead Ceramic Thinpack™ Flat Pack (Package 321)

- 32 pin, Rectangular Ceramic Leadless Chip Carrier (Package 601)
- Commercial, Industrial and Military Temperature Range
- 5V Power Supply
- Low Power CMOS
- Low Power Data Retention for Battery Back-up Operation
- TTL Compatible Inputs and Outputs

*This product is subject to change without notice.

REVOLUTIONARY PINOUT

EVOLUTIONARY PINOUT

36 FLAT PACK
36 CSOJ

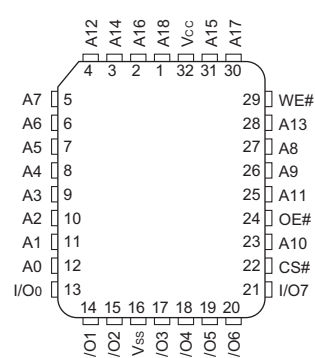
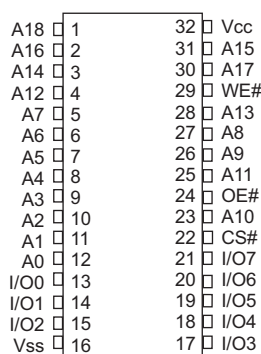
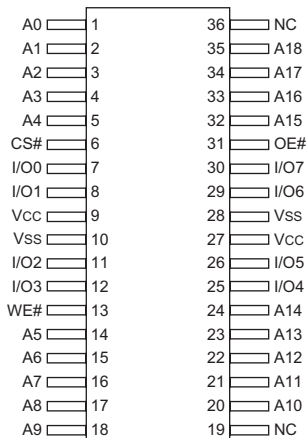
32 DIP
32 CSOJ (DE)
32 FLAT PACK (FF)

32 CLCC

TOP VIEW

TOP VIEW

TOP VIEW



PIN DESCRIPTION

| | |
|-----------------|-------------------|
| A0-18 | Address Inputs |
| I/O 0-7 | Data Input/Output |
| CS# | Chip Select |
| OE# | Output Enable |
| WE# | Write Enable |
| V _{cc} | +5.0V Power |
| GND | Ground |



Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Unit |
|---|------------------|------|----------------------|------|
| Operating Temperature | T _A | -55 | +125 | °C |
| Storage Temperature Range | T _{STG} | -65 | +150 | °C |
| Signal Voltage Range to GND | V _G | -0.5 | V _{CC} -0.5 | V |
| Junction Temperature | T _J | | 150 | °C |
| Supply Voltage Range (V _{CC}) | V _{CC} | -0.5 | 7.0 | V |

Truth Table

| CS# | OE# | WE# | MODE | DATA I/O | POWER |
|-----|-----|-----|-------------|----------|---------|
| H | X | X | Standby | High Z | Standby |
| L | L | H | Read | Data Out | Active |
| L | X | L | Write | Data In | Active |
| L | H | H | Out Disable | High Z | Active |

Recommended Operating Conditions

| Parameter | Symbol | Min | Max | Unit |
|----------------------|-----------------|------|-----------------------|------|
| Supply Voltage | V _{CC} | 4.5 | 5.5 | V |
| Input High Voltage | V _{IH} | 2.2 | V _{CC} + 0.3 | V |
| Input Low Voltage | V _{IL} | -0.3 | +0.8 | V |
| Operating Temp. (Mf) | T _A | -55 | +125 | °C |

Capacitance
(T_A = +25°C)

| Parameter | Symbol | Conditions | Package | Speed (ns) | Max | Unit |
|--------------------|------------------|-------------------------------------|---|------------|-----|------|
| Input capacitance | C _{IN} | V _{IN} = 0 V, f = 1.0 MHz | 32 pin CSOJ, DIP, Flat Pack Evolutionary | 15 to 55 | 20 | pF |
| | | | 32 pin CLCC | 15 to 55 | 15 | pF |
| | | | 36 pin CSOJ & Flat Pack Revolutionary | 15 to 35 | 12 | pF |
| | | | | 45 to 55 | 20 | pF |
| Output capacitance | C _{OUT} | V _{OUT} = 0 V, f = 1.0 MHz | 32 pin CSOJ, DIP, Flat Pack Revolutionary | 15 to 55 | 20 | pF |
| | | | 36 pin CSOJ & Flat Pack Revolutionary | 15 to 35 | 12 | pF |
| | | | | 45 to 55 | 20 | pF |

This parameter is guaranteed by design but not tested.

DC Characteristics - CMOS Compatible

(V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ 125°C)

| Parameter | Symbol | Conditions | Min | Max | Unit |
|---------------------------|-----------------|---|-----|------|------|
| Input Leakage Current | I _{LI} | V _{CC} = 5.5, V _{IN} = GND to V _{CC} | | 10 | A |
| Output Leakage Current | I _{LO} | CS# = V _{IH} , OE# = V _{IH} , V _{OUT} = GND TO V _{CC} | | 10 | A |
| Operating Supply Current* | I _{CC} | CS# = V _{IH} , OE# = V _{IH} , f = 5MHz, V _{CC} = 5.5, | | 160 | mA |
| Standby Current | I _{SS} | CS# = V _{IH} , OE# = V _{IH} , f = 5MHz, V _{CC} = 5.5 | | 0.45 | mA |
| Output Low Voltage | V _{OL} | I _{OL} = 6mA for 17 - 35ns, I _{OL} = 2.1mA for 45 - 55ns, V _{CC} = 4.5 | | 0.4 | V |
| Output High Voltage | V _{OH} | I _{OH} = -4.0mA for 17 - 35ns, I _{OH} = 1.0mA for 45 - 55ns, V _{CC} = 4.5 | 2.4 | | V |

Data retention characteristics for low power "I" version

| Parameter | Symbol | Conditions | Min | Max | Unit |
|-------------------------------|--------------------|--|-----|-----|------|
| Data Retention Supply Voltage | V _{DR} | CS# ³ V _{CC} -0.2V | 2.0 | 5.5 | V |
| Low Power Data Retention | I _{CCDR1} | V _{CC} = 3V | | 7 | mA |
| Low Power Data Retention | I _{CCDR2} | V _{CC} = 2V | | 2 | mA |



AC Characteristics

($V_{CC} = 5.0V, GND = 0V, -55^{\circ}C \leq T_A \leq 125^{\circ}C$)

| Parameter | Symbol | -15 | | -17 | | -20 | | -25 | | -35 | | -45 | | -55 | | Unit |
|------------------------------------|------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | t_{RC} | 15 | | 17 | | 20 | | 25 | | 35 | | 45 | | 55 | | ns |
| Address Access Time | t_{AA} | | 15 | | 17 | | 20 | | 25 | | 35 | | 45 | | 55 | ns |
| Output Hold from Address Change | t_{OH} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Chip Select Access Time | t_{ACS} | | 15 | | 17 | | 20 | | 25 | | 35 | | 45 | | 55 | ns |
| Output Enable to Output Valid | t_{OE} | | 8 | | 9 | | 10 | | 12 | | 25 | | 25 | | 25 | ns |
| Chip Select to Output in Low Z | t_{CLZ1} | 2 | | 2 | | 2 | | 2 | | 4 | | 4 | | 4 | | ns |
| Output Enable to Output in Low Z | t_{OLZ1} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Chip Disable to Output in High Z | t_{CHZ1} | | 8 | | 9 | | 10 | | 12 | | 15 | | 20 | | 20 | ns |
| Output Disable to Output in High Z | t_{OHZ1} | | 8 | | 9 | | 10 | | 12 | | 15 | | 20 | | 20 | ns |

AC Characteristics

($V_{CC} = 5.0V, GND = 0V, -55^{\circ}C \leq T_A \leq 125^{\circ}C$)

| Parameter | Symbol | -15 | | -17 | | -20 | | -25 | | -35 | | -45 | | -55 | | Unit |
|----------------------------------|------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | t_{WC} | 15 | | 17 | | 20 | | 25 | | 35 | | 45 | | 55 | | ns |
| Chip Select to End of Write | t_{CW} | 13 | | 14 | | 14 | | 15 | | 25 | | 35 | | 50 | | ns |
| Address Valid to End of Write | t_{AW} | 13 | | 14 | | 14 | | 15 | | 25 | | 35 | | 50 | | ns |
| Data Valid to End of Write | t_{DW} | 8 | | 9 | | 10 | | 10 | | 20 | | 25 | | 25 | | ns |
| Write Pulse Width | t_{WP} | 13 | | 14 | | 14 | | 15 | | 25 | | 35 | | 40 | | ns |
| Address Setup Time | t_{AS} | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | ns |
| Address Hold Time | t_{AH} | 0 | | 0 | | 0 | | 0 | | 0 | | 5 | | 5 | | ns |
| Output Active from End of Write | t_{OW1} | 2 | | 2 | | 3 | | 4 | | 4 | | 5 | | 5 | | ns |
| Write Enable to Output in High Z | t_{WHZ1} | | 8 | | 9 | | 9 | | 10 | | 15 | | 20 | | 25 | ns |
| Data Hold Time | t_{DH} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT



AC TEST CONDITIONS

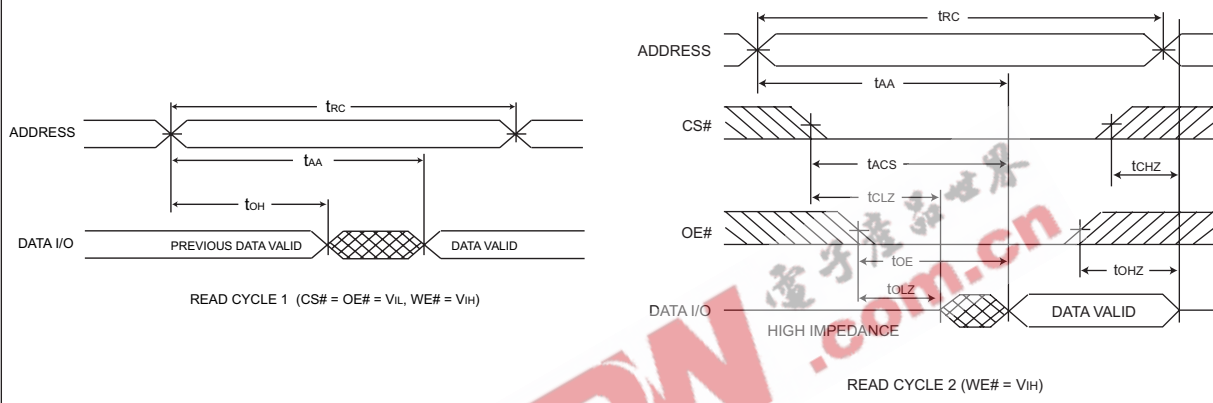
| Parameter | Typ | Unit |
|----------------------------------|----------------------------|------|
| Input Pulse Levels | $V_{IL} = 0, V_{IH} = 3.0$ | V |
| Input Rise and Fall | 5 | ns |
| Input and Output Reference Level | 1.5 | V |
| Output Timing Reference Level | 1.5 | V |

Notes:

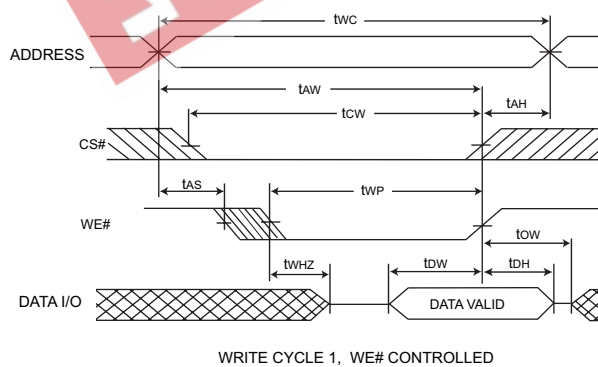
V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance $Z_0 = 75 \Omega$.
 V_Z is typically the midpoint of V_{OH} and V_{OL} .
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.



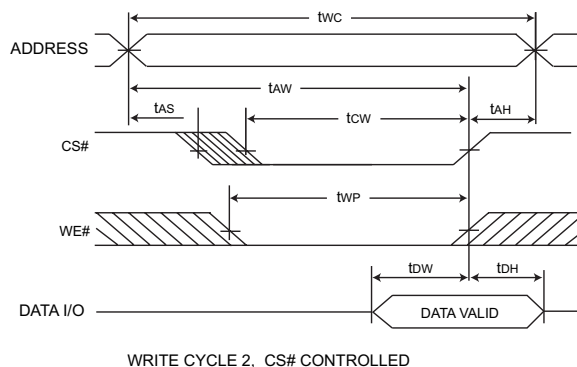
TIMING WAVEFORM - READ CYCLE



WRITE CYCLE - WE# CONTROLLED

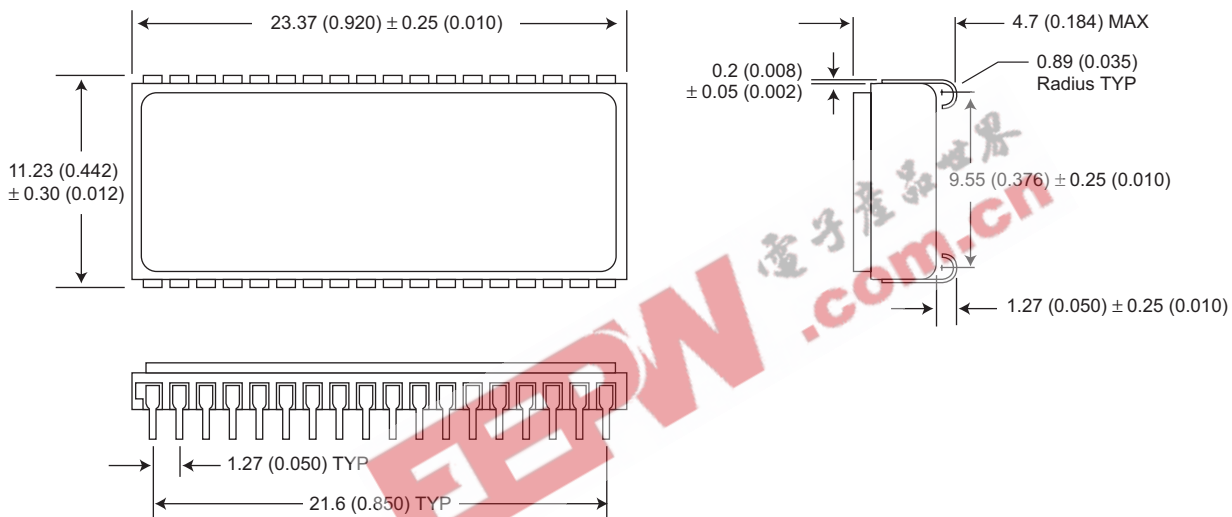


WRITE CYCLE - CS# CONTROLLED



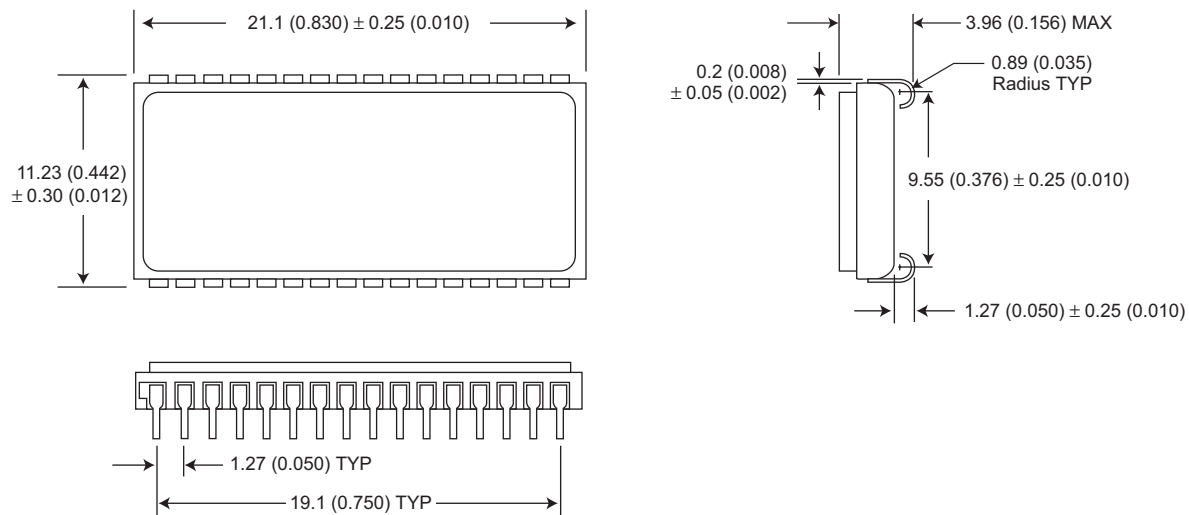


PACKAGE 100: 36 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 101: 32 LEAD, CERAMIC SOJ



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PACKAGE 321: 32 PIN CERAMIC THINPACK™ FLATPACK



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PACKAGE 226: 36 LEAD, CERAMIC FLAT PACK



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



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PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



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ORDERING INFORMATION

W M S 512K 8 X - XXX X X X

WHITE ELECTRONIC DESIGNS CORP. _____

MONOLITHIC _____

SRAM _____

ORGANIZATION, 512K X 8 _____

IMPROVEMENT MARK: _____

- BLANK = STANDARD
- L = LOW POWER DATA RETENTION

ACCESS TIME (NS) _____

PACKAGE: _____

- C = 32 PIN CERAMIC 0.600" DIP (PACKAGE 300)
- CL = 32 PIN RECTANGULAR CERAMIC LEADLESS CHIP CARRIER (PACKAGE 601)
- DE = 32 LEAD CERAMIC SOJ (PACKAGE 101) EVOLUTIONARY
- DJ = 36 LEAD CERAMIC SOJ (PACKAGE 100)
- F = 36 LEAD CERAMIC FLAT PACK (PACKAGE 226)
- FF = 32 LEAD CERAMIC THINPACK™ FLAT PACK (PACKAGE 321)

DEVICE GRADE: _____

- Q = MIL-STD-883 COMPLIANT
- M = MILITARY SCREENED -55°C ≤ TA ≤ 125°C
- I = INDUSTRIAL -40°C ≤ TA ≤ 85°C
- C = COMMERCIAL 0°C ≤ TA ≤ 70°C

LEAD FINISH: _____

- BLANK = GOLD PLATED LEADS
- A = SOLDER DIP LEADS



| DEVICE TYPE | SPEED | PACKAGE | SMD NO. |
|--------------------------|-------|-----------------------|------------------|
| 512K x 8 SRAM Monolithic | 55ns | 32 pin DIP (C) | 5962-95613 05HYX |
| 512K x 8 SRAM Monolithic | 45ns | 32 pin DIP (C) | 5962-95613 06HYX |
| 512K x 8 SRAM Monolithic | 35ns | 32 pin DIP (C) | 5962-95613 07HYX |
| 512K x 8 SRAM Monolithic | 25ns | 32 pin DIP (C) | 5962-95613 08HYX |
| 512K x 8 SRAM Monolithic | 20ns | 32 pin DIP (C) | 5962-95613 09HYX |
| 512K x 8 SRAM Monolithic | 17ns | 32 pin DIP (C) | 5962-95613 10HYX |
| 512K x 8 SRAM Monolithic | 15ns | 32 pin DIP (C) | 5962-95613 14HYX |
| 512K x 8 SRAM Monolithic | 55ns | 32 lead SOJ Evol (DE) | 5962-95613 05HTX |
| 512K x 8 SRAM Monolithic | 45ns | 32 lead SOJ Evol (DE) | 5962-95613 06HTX |
| 512K x 8 SRAM Monolithic | 35ns | 32 lead SOJ Evol (DE) | 5962-95613 07HTX |
| 512K x 8 SRAM Monolithic | 25ns | 32 lead SOJ Evol (DE) | 5962-95613 08HTX |
| 512K x 8 SRAM Monolithic | 20ns | 32 lead SOJ Evol (DE) | 5962-95613 09HTX |
| 512K x 8 SRAM Monolithic | 17ns | 32 lead SOJ Evol (DE) | 5962-95613 10HTX |
| 512K x 8 SRAM Monolithic | 15ns | 32 lead SOJ Evol (DE) | 5962-95613 14HTX |
| 512K x 8 SRAM Monolithic | 55ns | 36 lead SOJ (DJ) | 5962-95613 05HZX |
| 512K x 8 SRAM Monolithic | 45ns | 36 lead SOJ (DJ) | 5962-95613 06HZX |
| 512K x 8 SRAM Monolithic | 35ns | 36 lead SOJ (DJ) | 5962-95613 07HZX |
| 512K x 8 SRAM Monolithic | 25ns | 36 lead SOJ (DJ) | 5962-95613 08HZX |
| 512K x 8 SRAM Monolithic | 20ns | 36 lead SOJ (DJ) | 5962-95613 09HZX |
| 512K x 8 SRAM Monolithic | 17ns | 36 lead SOJ (DJ) | 5962-95613 10HZX |
| 512K x 8 SRAM Monolithic | 15ns | 36 lead SOJ (DJ) | 5962-95613 14HZX |
| 512K x 8 SRAM Monolithic | 55ns | 36 lead Flatpack (F) | 5962-95613 05HXX |
| 512K x 8 SRAM Monolithic | 45ns | 36 lead Flatpack (F) | 5962-95613 06HXX |
| 512K x 8 SRAM Monolithic | 35ns | 36 lead Flatpack (F) | 5962-95613 07HXX |
| 512K x 8 SRAM Monolithic | 25ns | 36 lead Flatpack (F) | 5962-95613 08HXX |
| 512K x 8 SRAM Monolithic | 20ns | 36 lead Flatpack (F) | 5962-95613 09HXX |
| 512K x 8 SRAM Monolithic | 17ns | 36 lead Flatpack (F) | 5962-95613 10HXX |
| 512K x 8 SRAM Monolithic | 15ns | 36 lead Flatpack (F) | 5962-95613 14HXX |