128Kx8 CMOS MONOLITHIC EEPROM, SMD 5962-96796

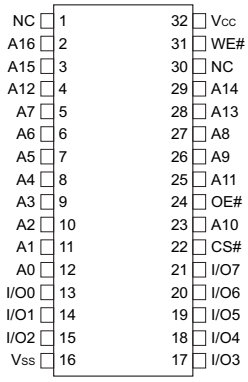
FEATURES

- Read Access Times of 120, 140, 150, 200, 250, 300ns
- JEDEC Approved Packages
  - 32 pin, Hermetic Ceramic, 0.600" DIP (Package 300)
  - 32 lead, Hermetic Ceramic, 0.400" SOJ (Package 101)
- Commercial, Industrial and Military Temperature Ranges
- MIL-STD-883 Compliant Devices Available
- Write Endurance 10,000 Cycles
- Data Retention at 25°C, 10 Years
- Low Power CMOS Operation
- Automatic Page Write Operation
  - Internal Address and Data Latches for 128 Bytes
  - Internal Control Timer
- Page Write Cycle Time 10ms Max.
- Data Polling for End of Write Detection
- Hardware and Software Data Protection
- TTL Compatible Inputs and Outputs

This product is subject to change without notice.

FIGURE 1 –

Pin Configuration
32 DIP
32 CSOJ
Top View



Pin Description

A0-16	Address Inputs
I/O0-7	Data Input/Output
CS#	Chip Selects
OE#	Output Enable
WE#	Write Enable
Vcc	+5.0v Power
Vss	Ground

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol		Unit
Operating Temperature	T_A	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Signal Voltage Relative to GND	V_G	-0.6 to + 6.25	V
Voltage on OE# and A9		-0.6 to +13.5	V

NOTE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C

TRUTH TABLE

CS#	OE#	WE#	Mode	Data I/O
H	X	X	Standby	High Z
L	L	H	Read	Data Out
L	H	L	Write	Data In
X	H	X	Out Disable	High Z/Data Out
X	X	H	Write	
X	L	X	Inhibit	

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V, f = 1MHz	20	pF
Output Capacitance	C_{OUT}	$V_{I/O}$ = 0 V, f = 1MHz	20	pF

This parameter is guaranteed by design but not tested.

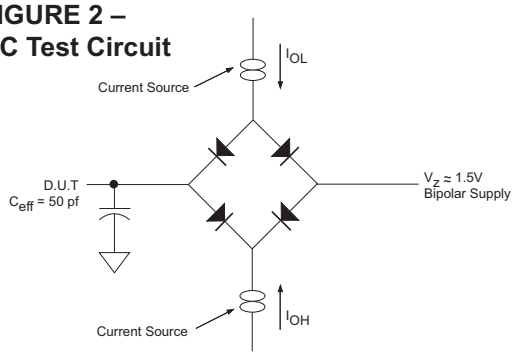
DC CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	CS# = V_{IH}, OE# = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current	I_{CC}	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		80	mA
Standby Current	I_{SB}	CS# = V_{IH}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		0.625	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA, V_{CC} = 4.5V		0.45	V
Output High Voltage	V_{OH}	I_{OH} = -400µA, V_{CC} = 4.5V	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

FIGURE 2 – AC Test Circuit



AC TEST CONDITIONS

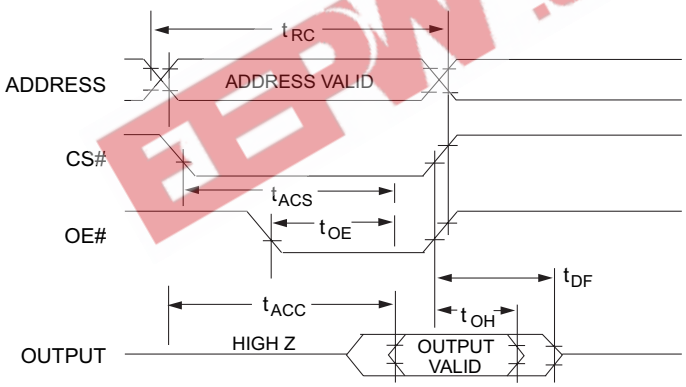
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes: V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

READ

Figure 3 shows Read cycle waveforms. A read cycle begins with selection address, chip select and output enable. Chip select is accomplished by placing the CS# line low. Output enable is done by placing the OE# line low. The memory places the selected data byte on I/O0 through I/O7 after the access time. The output of the memory is placed in a high impedance state shortly after either the OE# line or CS# line is returned to a high level.

FIGURE 3 – READ WAVEFORMS



NOTE:
OE# may be delayed up to t_{ACS}- t_{OE} after the falling edge of CS# without impact on t_{OE} or by t_{ACC}- t_{OE} after an address change without impact on t_{ACC}.

AC READ CHARACTERISTICS (See Figure 3)

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Read Cycle Parameter	Symbol	-120		-140		-150		-200		-250		-300		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		140		150		200		250		300		ns
Address Access Time	t_{ACC}		120		140		150		200		250		300	ns
Chip Select Access Time	t_{ACS}		120		140		150		200		250		300	ns
Output Hold from Address Change, OE# or CS#	t_{OH}	0		0		0		0		0		0		ns
Output Enable to Output Valid	t_{OE}	0	50	0	55	0	55	0	55	0	85	0	85	ns
Chip Select or OE# to High Z Output	t_{DF}		60		70		70		70		70		70	ns

WRITE

Write operations are initiated when both CS# and WE# are low and OE# is high. The EEPROM devices support both a CS# and WE# controlled write cycle. The address is latched by the falling edge of either CS# or WE#, whichever occurs last.

The data is latched internally by the rising edge of either CS# or WE#, whichever occurs first. A byte write operation will automatically continue to completion.

WRITE CYCLE TIMING

Figures 4 and 5 show the write cycle timing relationships. A write cycle begins with address application, write enable and chip select. Chip select is accomplished by placing the CS# line low. Write enable consists of setting the WE# line low. The write cycle begins when the last of either CS# or WE# goes low.

The WE# line transition from high to low also initiates an internal 150µsec delay timer to permit page mode operation. Each subsequent WE# transition from high to low that occurs before the completion of the 150µsec time out will restart the timer from zero. The operation of the timer is the same as a retriggerable one-shot.

AC WRITE CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	128Kx8		Unit
		Min	Max	
Write Cycle Time, TYP = 6ms	t_{WC}		10	ms
Address Set-up Time	t_{AS}	10		ns
Write Pulse Width (WE# or CS#)	t_{WP}	100		ns
Chip Select Set-up Time	t_{CS}	0		ns
Address Hold Time	t_{AH}	100		ns
Data Hold Time	t_{DH}	10		ns
Chip Select Hold Time	t_{CH}	0		ns
Data Set-up Time	t_{DS}	50		ns
Output Enable Set-up Time	t_{OES}	0		ns
Output Enable Hold Time	t_{OEH}	0		ns
Write Pulse Width High	t_{WPH}	50		ns

FIGURE 4 – WRITE WAVEFORMS WE# CONTROLLED

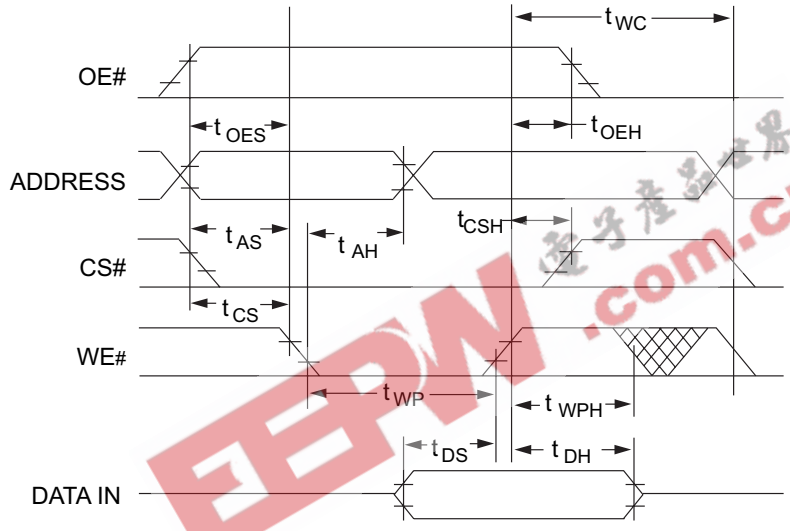
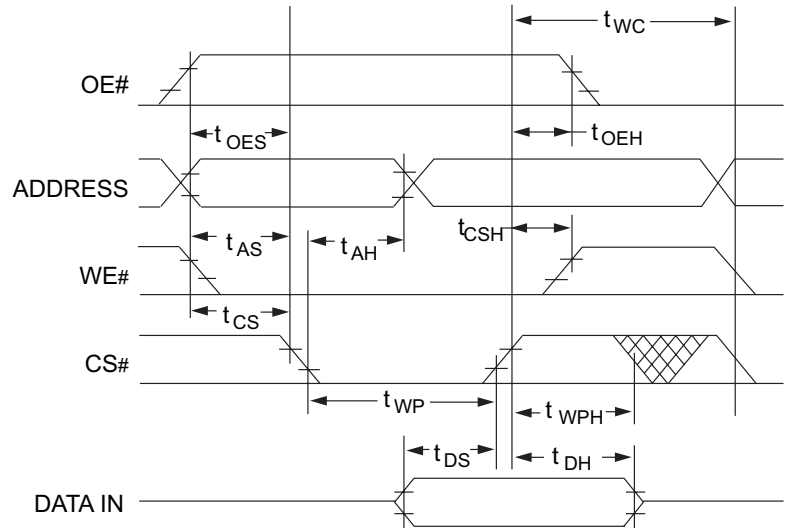


FIGURE 5 – WRITE WAVEFORMS CS# CONTROLLED



DATA POLLING

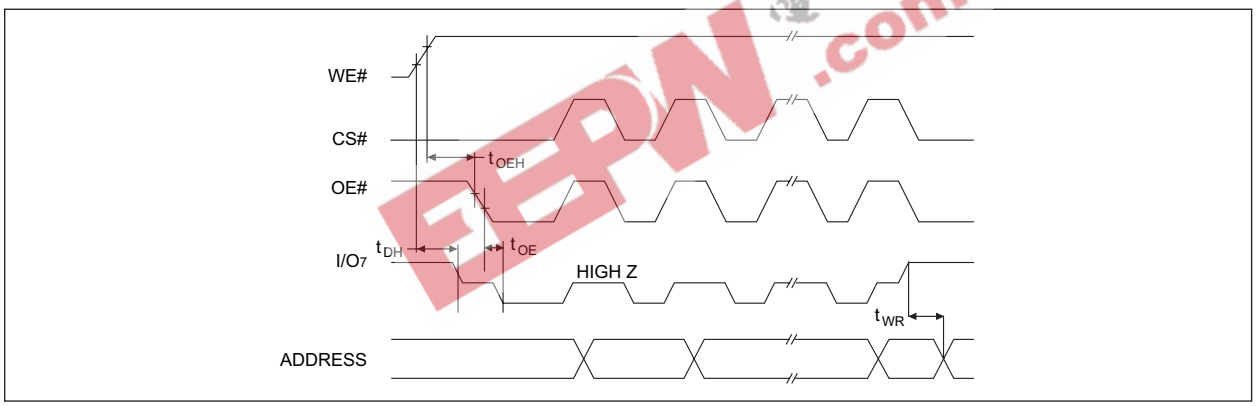
The WME128K8-XXX offers a data polling feature which allows a faster method of writing to the device. Figure 6 shows the timing diagram for this function. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data on I/O7. Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. Data polling may begin at any time during the write cycle.

DATA POLLING CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Min	Max	Unit
Data Hold Time	tdh	10		ns
OE# Hold Time	toeh	10		ns
OE# To Output Valid	toe		55	ns
Write Recovery Time	twr	0		ns

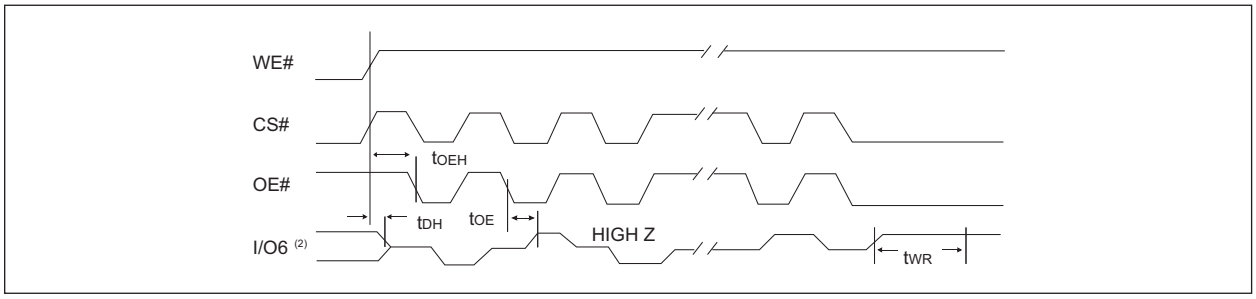
FIGURE 6 – DATA POLLING WAVEFORMS



TOGGLE BIT: In addition to DATA# Polling another method for determining the end of a write cycle is provided . During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

TOGGLE BUT CHARACTERISTICS(1)

Symbol	Parameter	Min	Max	Units
tDH	Data Hold Time	10		ns
tOEH	OE Hold Time	10		ns
tOE	OE to Output Delay			ns
tOEHP	OE High Pulse	150		ns
tWR	Write Recovery Time	0		ns



NOTE:
1. Toggling either OE# or CS# or both OE# and CS# will operate toggle bit.
2. Beginning and ending state of I/O6 will vary
3. Any address location may be used but the address should not vary.

PAGE WRITE OPERATION

The WME128K8-XXX has a page write operation that allows one to 128 bytes of data to be written into the device and consecutively loads during the internal programming period. Successive bytes may be loaded in the same manner after the first data byte has been loaded. An internal timer begins a time out operation at each write cycle. If another write cycle is completed within 150µs or less, a new time out period begins. Each write cycle restarts the delay period. The write cycles can be continued as long as the interval is less than the time out period.

The usual procedure is to increment the least significant address lines from A0 through A6 at each write cycle. In this manner a page of up to 128 bytes can be loaded in to the EEPROM in a burst mode before beginning the relatively long interval programming cycle.

After the 150µs time out is completed, the EEPROM begins an internal write cycle. During this cycle the entire page of bytes will be written at the same time. The internal programming cycle is the same regardless of the number of bytes accessed.

PAGE WRITE CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Page Mode Write Characteristics	Symbol			Unit
Parameter		**Min**	**Max**	
Write Cycle Time, TYP = 6ms	t_{wc}		10	ms
Address Set-up Time	t_{as}	10		ns
Address Hold Time (1)	t_{ah}	100		ns
Data Set-up Time	t_{ds}	50		ns
Data Hold Time	t_{dh}	10		ns
Write Pulse Width	t_{wp}	100		ns
Byte Load Cycle Time	t_{blc}		150	µs
Write Pulse Width High	t_{wph}	50		ns

1. Page address must remain valid for duration of write cycle.

FIGURE 7 – PAGE MODE WRITE WAVEFORMS

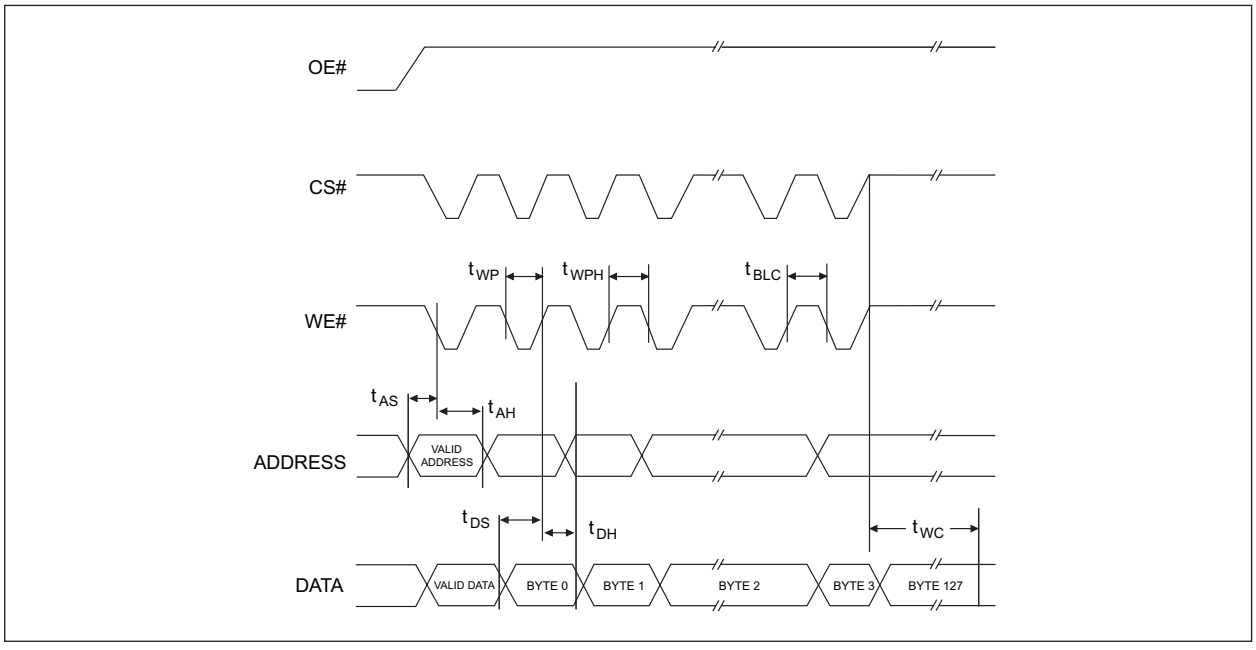
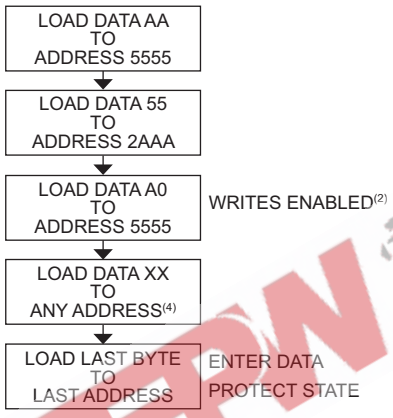
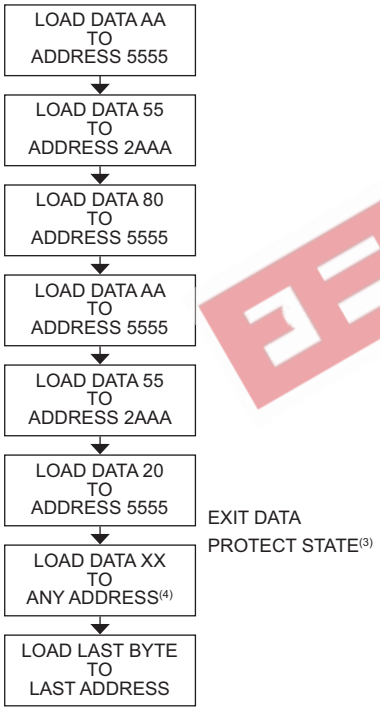


FIGURE 8 – SOFTWARE DATA PROTECTION ENABLE ALGORITHM(1)



NOTES:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A_{16} - A_0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data to be loaded.

FIGURE 9 –
SOFTWARE BLOCK DATA PROTECTION
DISABLE ALGORITHM(1)



NOTES:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A16 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data may be loaded.

SOFTWARE DATA PROTECTION

A software write protection feature may be enabled or disabled by the user. When shipped by White Microelectronics, the WME128K8-XXX has the feature disabled. Write access to the device is unrestricted.

To enable software write protection, the user writes three access code bytes to three special internal locations. Once write protection has been enabled, each write to the EEPROM must use the same three byte write sequence to permit writing. After setting software Data protection, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No Data will be written to the device; however, for the duration of t_{WC}. The write protection feature can be disabled by a six byte write sequence of specific data to specific locations. Power transitions will not reset the software write protection.

The software write protection guards against inadvertent writes during power transitions or unauthorized modification using a PROM programmer.

HARDWARE DATA PROTECTION

These features protect against inadvertent writes to the WME128K8-XXX. These are included to improve reliability during normal operation:

a) V_{CC} power on delay

As V_{CC} climbs past 3.8V typical the device will wait 5msec typical before allowing write cycles.

b) V_{CC} sense

While below 3.8V typical write cycles are inhibited.

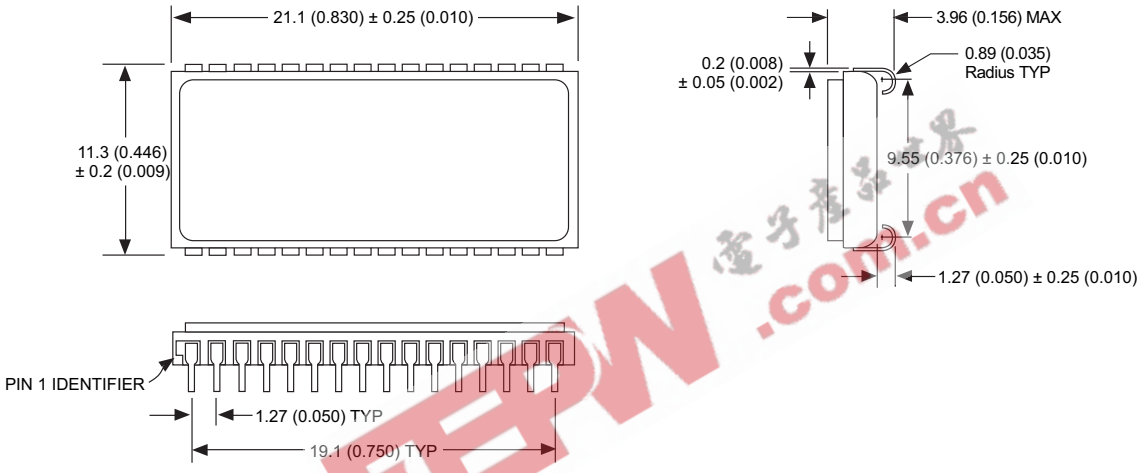
c) Write inhibiting

Holding OE# low and either CS# or WE# high inhibits write cycles.

d) Noise filter

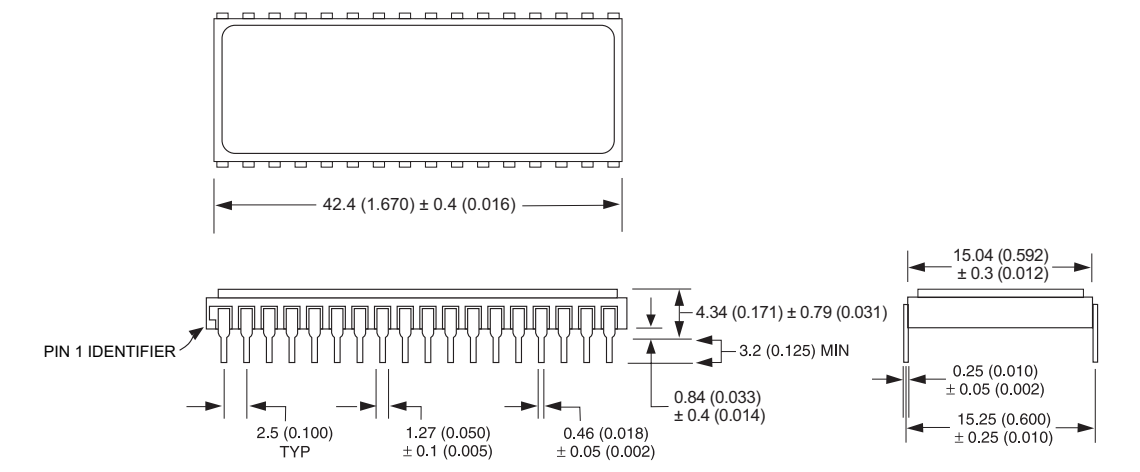
Pulses of <15ns (typ) on WE# or CS# will not initiate a write cycle.

PACKAGE 101: 32 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



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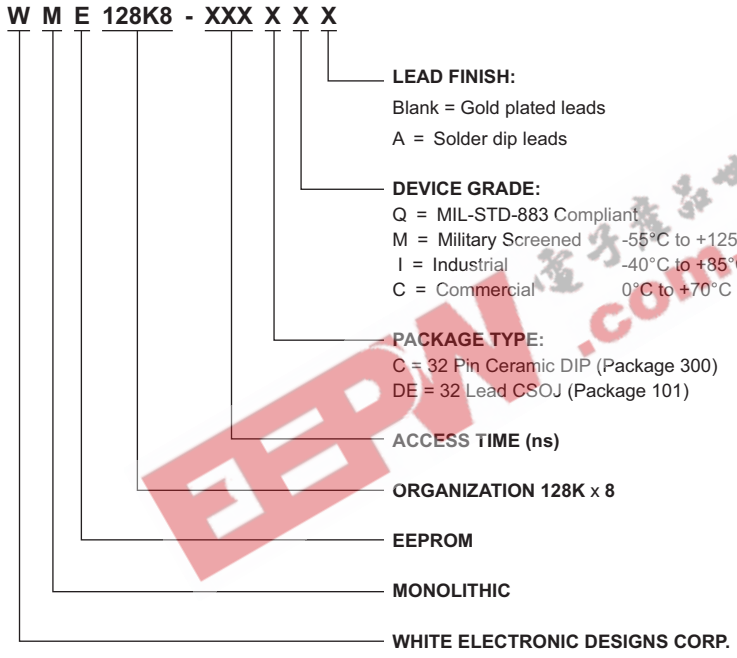
ORDERING INFORMATION



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
128K x 8 EEPROM Monolithic	300ns	32 pin DIP (C)	5962-96796 01HYX
128K x 8 EEPROM Monolithic	250ns	32 pin DIP (C)	5962-96796 02HYX
128K x 8 EEPROM Monolithic	200ns	32 pin DIP (C)	5962-96796 03HYX
128K x 8 EEPROM Monolithic	150ns	32 pin DIP (C)	5962-96796 04HYX
128K x 8 EEPROM Monolithic	140ns	32 pin DIP (C)	5962-96796 05HYX
128K x 8 EEPROM Monolithic	120ns	32 pin DIP (C)	5962-96796 06HYX
128K x 8 EEPROM Monolithic	300ns	32 lead SOJ (DE)	5962-96796 01HXX
128K x 8 EEPROM Monolithic	250ns	32 lead SOJ (DE)	5962-96796 02HXX
128K x 8 EEPROM Monolithic	200ns	32 lead SOJ (DE)	5962-96796 03HXX
128K x 8 EEPROM Monolithic	150ns	32 lead SOJ (DE)	5962-96796 04HXX
128K x 8 EEPROM Monolithic	140ns	32 lead SOJ (DE)	5962-96796 05HXX
128K x 8 EEPROM Monolithic	120ns	32 lead SOJ (DE)	5962-96796 06HXX