



128Kx8 3.3V MONOLITHIC SRAM

PRELIMINARY*

FEATURES

- Access Times 15, 17, 20, 25, 35ns
- Revolutionary, Center Power/Ground Pinout JEDEC Approved
 - 32 lead Ceramic SOJ (Package 101)
 - 32 lead Ceramic Flat Pack (Package 220)**
- Evolutionary, Corner Power/Ground Pinout JEDEC Approved
 - 32 pin Ceramic DIP (Package 300)
- 32 pin, Rectangular Ceramic Leadless Chip Carrier (Package 601)

- MIL-STD-883 Compliant Devices Available
- Commercial, Industrial and Military Temperature Range
- 3.3 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs

* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

** Package under development.

REVOLUTIONARY PINOUT

EVOLUTIONARY PINOUT

32 CSOJ (DR)
32 FLATPACK (FR)**

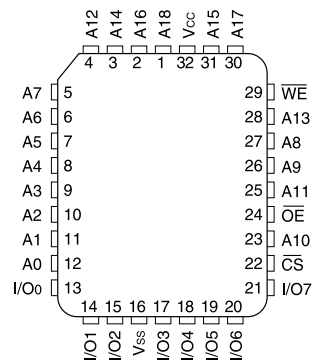
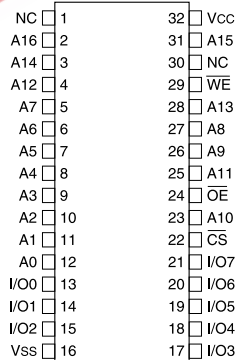
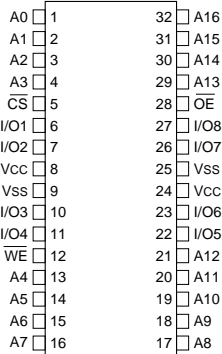
32 DIP (C)

32 CLCC

TOP VIEW

TOP VIEW

TOP VIEW



PIN DESCRIPTION

A0-16	Address Inputs
I/O0-7	Data Input/Outputs
\overline{CS}	Chip Select
\overline{OE}	Output Enable
\overline{WE}	Write Enable
Vcc	+3.3V Power
Vss	Ground
NC	Not Connected



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} +0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	5.5	V

TRUTH TABLE

\overline{CS}	\overline{OE}	\overline{WE}	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	3.0	3.6	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C

CAPACITANCE
(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C _{IN}	V _{IN} = 0V, f = 1.0MHz	20	pF
Output capacitance	C _{OUT}	V _{OUT} = 0V, f = 1.0MHz	20	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 3.3V ±0.3V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	Units		
			Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = 3.3, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	\overline{CS} = V _{IH} , \overline{OE} = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current (x 32 Mode)	I _{CC}	\overline{CS} = V _{IL} , \overline{OE} = V _{IH} , f = 5MHz, V _{CC} = 3.3		120	mA
Standby Current	I _{SB}	\overline{CS} = V _{IH} , \overline{OE} = V _{IH} , f = 5MHz, V _{CC} = 3.3		8	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4		V

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance Z₀ = 75 Ω.
 V_Z is typically the midpoint of V_{OH} and V_{OL}.
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.



AC CHARACTERISTICS
(V_{CC} = 3.3V, T_A = -55°C to +125°C)

Parameter	Symbol	-15		-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle												
Read Cycle Time	t _{RC}	15		17		20		25		35		ns
Address Access Time	t _{AA}		15		17		20		25		35	ns
Output Hold from Address Change	t _{OH}	0		0		0		0		0		ns
Chip Select Access Time	t _{ACS}		15		17		20		25		35	ns
Output Enable to Output Valid	t _{OE}		10		11		12		15		20	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	5		5		5		5		5		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	5		5		5		5		5		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		8		9		10		12		15	ns
Output Disable to Output in High Z	t _{OHZ} ¹		8		9		10		12		15	ns

1. This parameter is guaranteed by design but not tested.

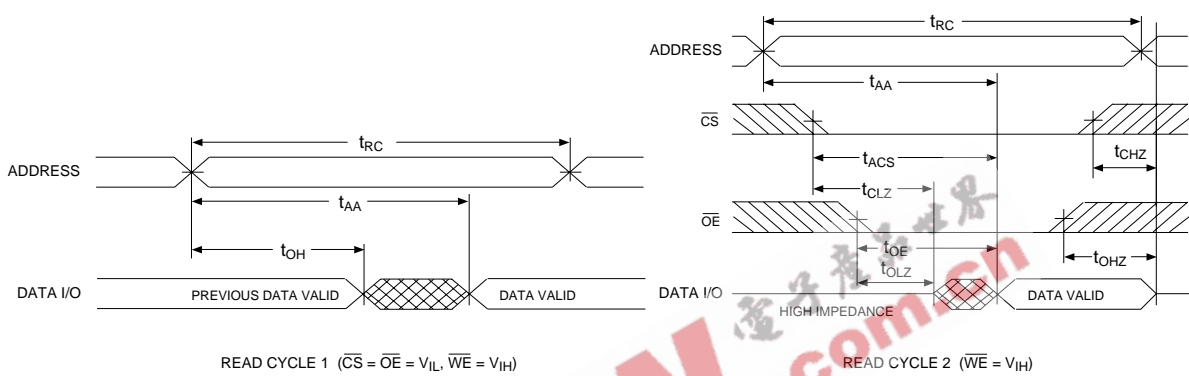
AC CHARACTERISTICS
(V_{CC} = 3.3V, T_A = -55°C to +125°C)

Parameter	Symbol	-15		-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle												
Write Cycle Time	t _{WC}	15		17		20		25		35		ns
Chip Select to End of Write	t _{CW}	13		14		15		20		30		ns
Address Valid to End of Write	t _{AW}	13		14		15		20		30		ns
Data Valid to End of Write	t _{DW}	10		11		12		15		18		ns
Write Pulse Width	t _{WP}	13		14		15		20		30		ns
Address Setup Time	t _{AS}	0		0		0		0		0		ns
Address Hold Time	t _{AH}	0		0		0		0		0		ns
Output Active from End of Write	t _{OW} ¹	5		5		5		5		5		ns
Write Enable to Output in High Z	t _{WHZ} ¹		8		9		10		10		15	ns
Data Hold Time	t _{DH}	0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.



TIMING WAVEFORM - READ CYCLE



WRITE CYCLE - \overline{WE} CONTROLLED



WRITE CYCLE - \overline{CS} CONTROLLED





PACKAGE 101: 32 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 220: 32 LEAD, CERAMIC FLAT PACK



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PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 601: 32 PIN, RECTANGULAR CERAMIC LEADLESS CHIP CARRIER



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

W M S 128K8 V - XXX X X X

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:

- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE:

- C = 32 Pin Ceramic .600" DIP (Package 300)
- CL = 32 Pin Rectangular Ceramic Leadless Chip Carrier (Package 601)
- DR = 32 Lead Ceramic SOJ (Package 101) Revolutionary
- FR = 32 Lead Ceramic Flat Pack (Package 220**) Revolutionary

ACCESS TIME (ns)

IMPROVEMENT MARK:

- Low Voltage Supply 3.3V ± 10%

ORGANIZATION, 128K x 8

SRAM

MONOLITHIC

WHITE ELECTRONIC DESIGNS CORP.

** Package under development.