



## 512Kx8 MONOLITHIC FLASH, SMD 5962-96692

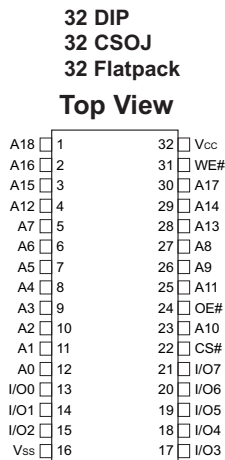
### FEATURES

- Access Times of 60, 70, 90, 120, 150ns
- Packaging
  - 32 pin, Hermetic Ceramic, 0.600" DIP (Package 300)
  - 32 lead, Hermetic Ceramic, 0.400" SOJ (Package 101)
  - 32 pin, Rectangular Ceramic Leadless Chip Carrier (Package 601)
  - 32 lead Flatpack (Package 220)
- 1,000,000 Erase/Program Cycles Minimum
- Sector Erase Architecture
  - 8 equal size sectors of 64K bytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Programming. 5V ± 10% Supply.
- Low Power CMOS
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Page Program Operation and Internal Program Control Time.

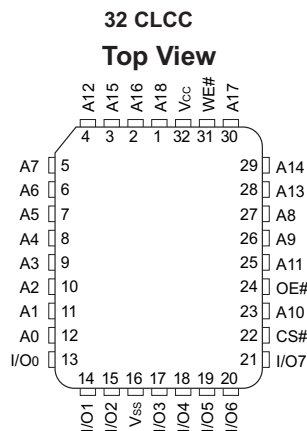
Note: For programming information refer to Flash Programming 4M5 Application Note.

This product is subject to change without notice.

#### Pin Configuration For WMF512K8-XXX5



#### Pin Configuration For WMF512K8-XCLX5



#### Pin Description

|        |                   |
|--------|-------------------|
| A0-18  | Address Inputs    |
| I/O0-7 | Data Input/Output |
| CS#    | Chip Select       |
| OE#    | Output Enable     |
| WE#    | Write Enable      |
| Vcc    | +5.0V Power       |
| Vss    | Ground            |



**ABSOLUTE MAXIMUM RATINGS (1)**

| Parameter  |               | Unit   |
|--|---------------|--------|
| Operating Temperature                                | -55 to +125   | °C     |
| Supply Voltage (V <sub>CC</sub> ) (1)                | -2.0 to +7.0  | V      |
| Signal Voltage Range(any pin except A9) (2)          | -2.0 to +7.0  | V      |
| Storage Temperature Range                            | -65 to +150   | °C     |
| Lead Temperature (soldering, 10 seconds)             | +300          | °C     |
| Data Retention Mil Temp                              | 20            | years  |
| Endurance - erase/program cycles (Mil Temp)          | 100,000 min   | cycles |
| A9 Voltage for sector protect (V <sub>ID</sub> ) (3) | -2.0 to +14.0 | V      |

**RECOMMENDED OPERATING CONDITIONS**

| Parameter                     | Symbol          | Min  | Max                   | Unit |
|-------------------------------|-----------------|------|-----------------------|------|
| Supply Voltage                | V <sub>CC</sub> | 4.5  | 5.5                   | V    |
| Input High Voltage            | V <sub>IH</sub> | 2.0  | V <sub>CC</sub> + 0.5 | V    |
| Input Low Voltage             | V <sub>IL</sub> | -0.5 | +0.8                  | V    |
| Operating Temp. (Mil.)        | T <sub>A</sub>  | -55  | +125                  | °C   |
| Operating Temp. (Ind.)        | T <sub>A</sub>  | -40  | +85                   | °C   |
| A9 Voltage for Sector Protect | V <sub>ID</sub> | 11.5 | 12.5                  | V    |

NOTES:

- Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot V<sub>SS</sub> to -2.0 V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is V<sub>CC</sub> + 0.5V. During voltage transitions, outputs may overshoot to V<sub>CC</sub> + 2.0 V for periods of up to 20ns.
- Minimum DC input voltage on A9 pin is -0.5V. During voltage transitions, A9 may overshoot V<sub>SS</sub> to -2V for periods of up to 20ns. Maximum DC input voltage on A9 is +13.5V which may overshoot to 14.0 V for periods up to 20ns.

**CAPACITANCE**

T<sub>A</sub> = +25°C

| Parameter                 | Symbol | Conditions                          | Max | Unit |
|---------------------------|--------|-------------------------------------|-----|------|
| Address Input capacitance | CAD    | V <sub>I/O</sub> = 0 V, f = 1.0 MHz | 15  | pF   |
| Output Enable capacitance | COE    | V <sub>IN</sub> = 0 V, f = 1.0 MHz  | 15  | pF   |
| Write Enable capacitance  | CWE    | V <sub>IN</sub> = 0 V, f = 1.0 MHz  | 15  | pF   |
| Chip Select capacitance   | CCS    | V <sub>IN</sub> = 0 V, f = 1.0 MHz  | 15  | pF   |
| Data I/O capacitance      | CI/O   | V <sub>I/O</sub> = 0 V, f = 1.0 MHz | 15  | pF   |

This parameter is guaranteed by design but not tested.

**DC CHARACTERISTICS — CMOS COMPATIBLE**

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

| Parameter   | Symbol             | Conditions  | Min                    | Max  | Unit |
|---|--------------------|---|------------------------|------|------|
| Input Leakage Current                                   | I <sub>LI</sub>    | V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub> |                        | 10   | μA   |
| Output Leakage Current                                  | I <sub>LOx32</sub> | V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub> |                        | 10   | μA   |
| V <sub>CC</sub> Active Current for Read (1)             | I <sub>CC1</sub>   | CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub> , f = 5MHz        |                        | 50   | mA   |
| V <sub>CC</sub> Active Current for Program or Erase (2) | I <sub>CC2</sub>   | CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub>                   |                        | 60   | mA   |
| V <sub>CC</sub> Standby Current                         | I <sub>CC4</sub>   | V <sub>CC</sub> = 5.5, CS# = V <sub>IH</sub> , f = 5MHz         |                        | 1.6  | mA   |
| Output Low Voltage                                      | V <sub>OL</sub>    | I <sub>OL</sub> = 8.0 mA, V <sub>CC</sub> = 4.5                 |                        | 0.45 | V    |
| Output High Voltage                                     | V <sub>OH1</sub>   | I <sub>OH</sub> = -2.5 mA, V <sub>CC</sub> = 4.5                | 0.85 x V <sub>CC</sub> |      | V    |
| Low V <sub>CC</sub> Lock-Out Voltage                    | V <sub>LKO</sub>   |   | 3.2                    | 4.2  | V    |

NOTES:

- The I<sub>CC</sub> current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with OE# at V<sub>IH</sub>.
- I<sub>CC</sub> active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions: V<sub>IL</sub> = 0.3V, V<sub>IH</sub> = V<sub>CC</sub> - 0.3V



**AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, CS# CONTROLLED**

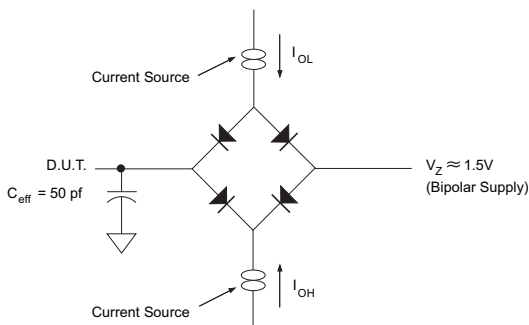
V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

| Parameter                                  | Symbol             |                  | -60 |     | -70 |     | -90 |     | -120 |     | -150 |     | Unit |
|--|--------------------|------------------|-----|-----|-----|-----|-----|-----|------|-----|------|-----|------|
|  |                    |                  | Min | Max | Min | Max | Min | Max | Min  | Max | Min  | Max |      |
| Write Cycle Time                           | t <sub>WAV</sub>   | t <sub>WIC</sub> | 60  |     | 70  |     | 90  |     | 120  |     | 150  |     | ns   |
| Write Enable Setup Time                    | t <sub>WLEL</sub>  | t <sub>WIS</sub> | 0   |     | 0   |     | 0   |     | 0    |     | 0    |     | ns   |
| Chip Select Pulse Width                    | t <sub>ELEH</sub>  | t <sub>CP</sub>  | 40  |     | 45  |     | 45  |     | 50   |     | 50   |     | ns   |
| Address Setup Time                         | t <sub>AVEL</sub>  | t <sub>AS</sub>  | 0   |     | 0   |     | 0   |     | 0    |     | 0    |     | ns   |
| Data Setup Time                            | t <sub>DVEH</sub>  | t <sub>DS</sub>  | 40  |     | 45  |     | 45  |     | 50   |     | 50   |     | ns   |
| Data Hold Time                             | t <sub>HDX</sub>   | t <sub>DH</sub>  | 0   |     | 0   |     | 0   |     | 0    |     | 0    |     | ns   |
| Address Hold Time                          | t <sub>ELAX</sub>  | t <sub>AH</sub>  | 40  |     | 45  |     | 45  |     | 50   |     | 50   |     | ns   |
| Chip Select Pulse Width High               | t <sub>EHEL</sub>  | t <sub>CPH</sub> | 20  |     | 20  |     | 20  |     | 20   |     | 20   |     | ns   |
| Duration of Byte Programming Operation (1) | t <sub>WHWH1</sub> |                  |     | 300 |     | 300 |     | 300 |      | 300 |      | 300 | μs   |
| Sector Erase Time (2)                      | t <sub>WHWH2</sub> |                  |     | 15  |     | 15  |     | 15  |      | 15  |      | 15  | sec  |
| Read Recovery Time                         | t <sub>RHEL</sub>  |                  | 0   |     | 0   |     | 0   |     | 0    |     | 0    |     | ns   |
| Chip Programming Time                      |                    |                  |     | 11  |     | 11  |     | 11  |      | 11  |      | 11  | sec  |
| Chip Erase Time (3)                        |                    |                  |     | 64  |     | 64  |     | 64  |      | 64  |      | 64  | sec  |

NOTES:

1. Typical value for t<sub>WHWH1</sub> is 7μs.
2. Typical value for t<sub>WHWH2</sub> is 1sec.
3. Typical value for Chip Erase time is 8sec.

**AC TEST CIRCUIT**



**AC Test Conditions**

| Parameter                        | Typ  | Unit |
|----------------------------------|--|------|
| Input Pulse Levels               | V <sub>IL</sub> = 0, V <sub>IH</sub> = 3.0 | V    |
| Input Rise and Fall              | 5  | ns   |
| Input and Output Reference Level | 1.5  | V    |
| Output Timing Reference Level    | 1.5  | V    |

Notes:

V<sub>Z</sub> is programmable from -2V to +7V.  
 I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.  
 Tester Impedance Z<sub>0</sub> = 75 Ω.  
 V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.  
 I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.  
 ATE tester includes jig capacitance.



**AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, WE# CONTROLLED**

V<sub>CC</sub> = 5.0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

| Parameter                                  | Symbol             |                  | -60 |     | -70 |     | -90 |     | -120 |     | -150 |     | Unit |
|--|--------------------|------------------|-----|-----|-----|-----|-----|-----|------|-----|------|-----|------|
|  |                    |                  | Min | Max | Min | Max | Min | Max | Min  | Max | Min  | Max |      |
| Write Cycle Time                           | t <sub>AVAV</sub>  | t <sub>WC</sub>  | 60  |     | 70  |     | 90  |     | 120  |     | 150  |     | ns   |
| Chip Select Setup Time                     | t <sub>ELWL</sub>  | t <sub>CS</sub>  | 0   |     | 0   |     | 0   |     | 0    |     | 0    |     | ns   |
| Write Enable Pulse Width                   | t <sub>WLWH</sub>  | t <sub>WP</sub>  | 40  |     | 45  |     | 45  |     | 50   |     | 50   |     | ns   |
| Address Setup Time                         | t <sub>AVWH</sub>  | t <sub>AS</sub>  | 0   |     | 0   |     | 0   |     | 0    |     | 0    |     | ns   |
| Data Setup Time                            | t <sub>DVWH</sub>  | t <sub>DS</sub>  | 40  |     | 45  |     | 45  |     | 50   |     | 50   |     | ns   |
| Data Hold Time                             | t <sub>WHDX</sub>  | t <sub>DH</sub>  | 0   |     | 0   |     | 0   |     | 0    |     | 0    |     | ns   |
| Address Hold Time                          | t <sub>WHAX</sub>  | t <sub>AH</sub>  | 40  |     | 45  |     | 45  |     | 50   |     | 50   |     | ns   |
| Write Enable Pulse Width High              | t <sub>HWHL</sub>  | t <sub>WPH</sub> | 20  |     | 20  |     | 20  |     | 20   |     | 20   |     | ns   |
| Duration of Byte Programming Operation (1) | t <sub>WHWH1</sub> |                  |     | 300 |     | 300 |     | 300 |      | 300 |      | 300 | μs   |
| Sector Erase Time (2)                      | t <sub>WHWH2</sub> |                  |     | 15  |     | 15  |     | 15  |      | 15  |      | 15  | sec  |
| Read Recovery Time before Write            | t <sub>GHWL</sub>  |                  | 0   |     | 0   |     | 0   |     | 0    |     | 0    |     | ms   |
| VCC Set-up Time                            |                    | t <sub>VCS</sub> | 50  |     | 50  |     | 50  |     | 50   |     | 50   |     | μs   |
| Chip Programming Time                      |                    |                  |     | 11  |     | 11  |     | 11  |      | 11  |      | 11  | sec  |
| Output Enable Setup Time                   |                    | t <sub>OES</sub> | 0   |     | 0   |     | 0   |     | 0    |     | 0    |     | ns   |
| Output Enable Hold Time (4)                |                    | t <sub>OEH</sub> | 10  |     | 10  |     | 10  |     | 10   |     | 10   |     | ns   |
| Chip Erase Time (3)                        |                    |                  |     | 64  |     | 64  |     | 64  |      | 64  |      | 64  | sec  |

NOTES:

1. Typical value for t<sub>WHWH1</sub> is 7μs.
2. Typical value for t<sub>WHWH2</sub> is 1sec.
3. Typical value for Chip Erase time is 8sec.
4. For Toggle and Data# Polling.

**AC CHARACTERISTICS – READ ONLY OPERATIONS**

V<sub>CC</sub> = 5.0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

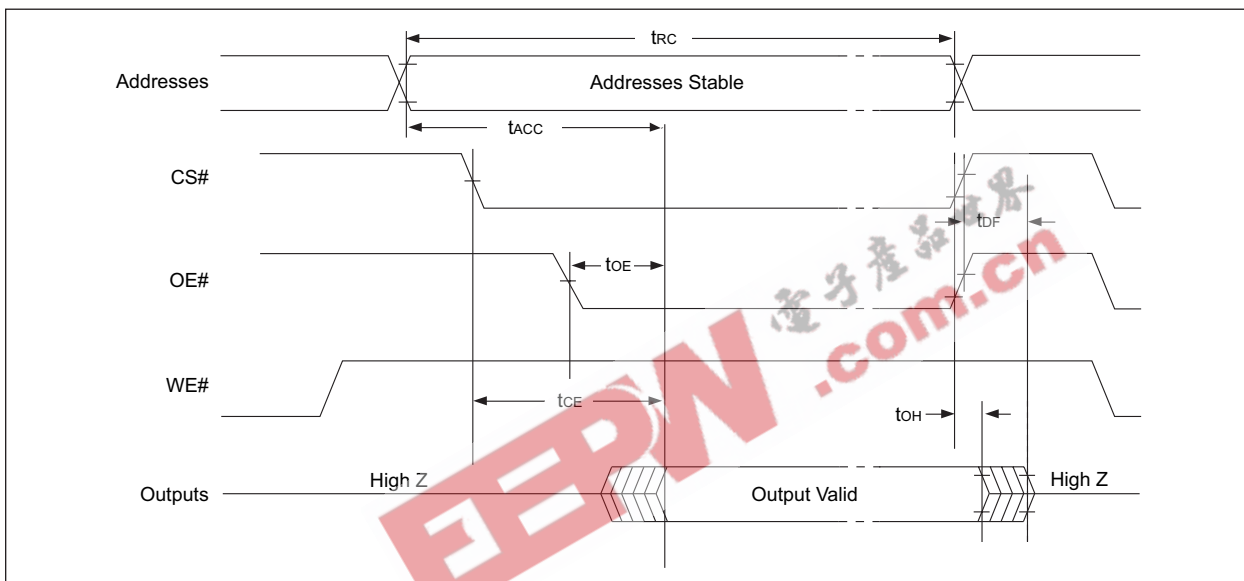
| Parameter   | Symbol            |                  | -60 |     | -70 |     | -90 |     | -120 |     | -150 |     | Unit |
|---|-------------------|------------------|-----|-----|-----|-----|-----|-----|------|-----|------|-----|------|
|   |                   |                  | Min | Max | Min | Max | Min | Max | Min  | Max | Min  | Max |      |
| Read Cycle Time   | t <sub>AVAV</sub> | t <sub>RC</sub>  | 60  |     | 70  |     | 90  |     | 120  |     | 150  |     | ns   |
| Address Access Time   | t <sub>AVQV</sub> | t <sub>ACC</sub> |     | 60  |     | 70  |     | 90  |      | 120 |      | 150 | ns   |
| Chip Select Access Time   | t <sub>ELQV</sub> | t <sub>CE</sub>  |     | 60  |     | 70  |     | 90  |      | 120 |      | 150 | ns   |
| Output Enable to Output Valid                                   | t <sub>GLQV</sub> | t <sub>OE</sub>  |     | 35  |     | 35  |     | 35  |      | 50  |      | 55  | ns   |
| Chip Select to Output High Z (1)                                | t <sub>EHQZ</sub> | t <sub>DF</sub>  |     | 20  |     | 20  |     | 20  |      | 30  |      | 35  | ns   |
| Output Enable High to Output High Z (1)                         | t <sub>GHQZ</sub> | t <sub>DF</sub>  |     | 20  |     | 20  |     | 20  |      | 30  |      | 35  | ns   |
| Output Hold from Address, CS# or OE# Change, whichever is First | t <sub>AXQX</sub> | t <sub>OH</sub>  | 0   |     | 0   |     | 0   |     | 0    |     | 0    |     | ns   |

NOTES:

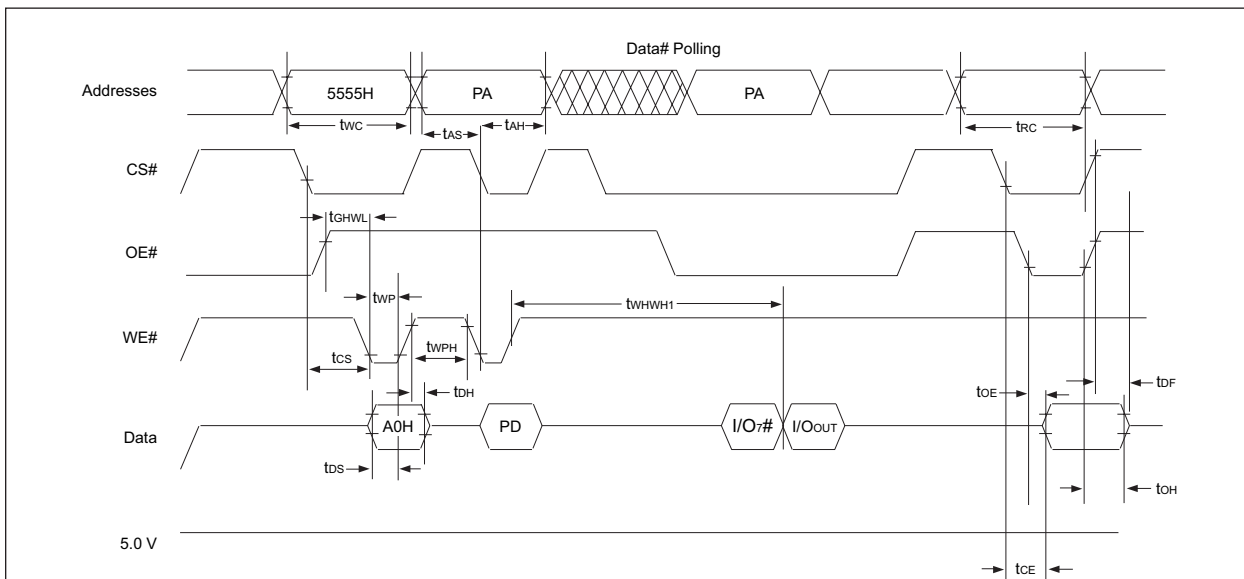
1. Guaranteed by design, but not tested



AC WAVEFORMS FOR READ OPERATIONS



WRITE/ERASE/PROGRAM OPERATION, WE# CONTROLLED

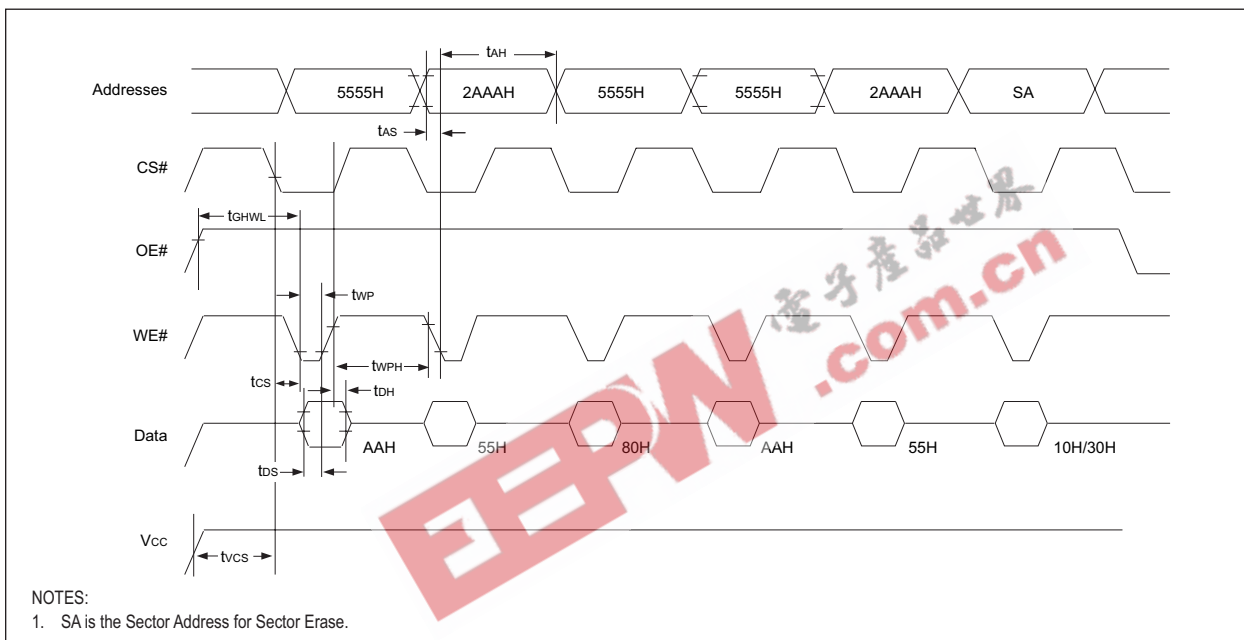


NOTES:

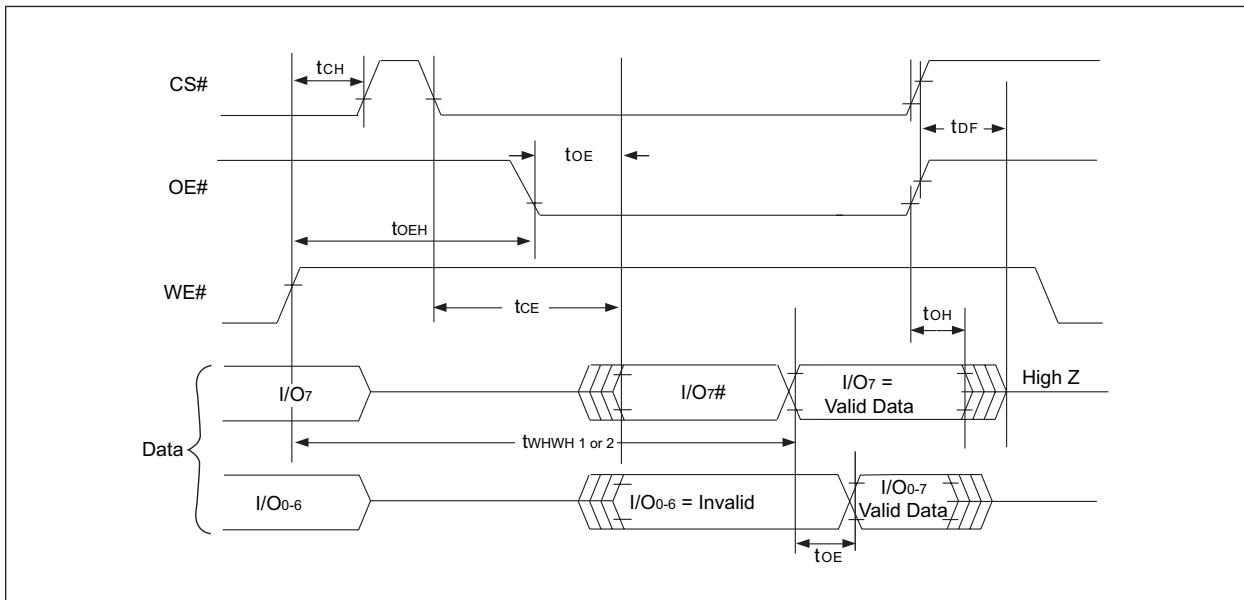
- 1. PA is the address of the memory location to be programmed.
- 2. PD is the data to be programmed at byte address.
- 3. I/O# is the output of the complement of the data written to the device.
- 4. I/Oout is the output of the data written to the device.
- 5. Figure indicates last two bus cycles of four bus cycle sequence.



AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS

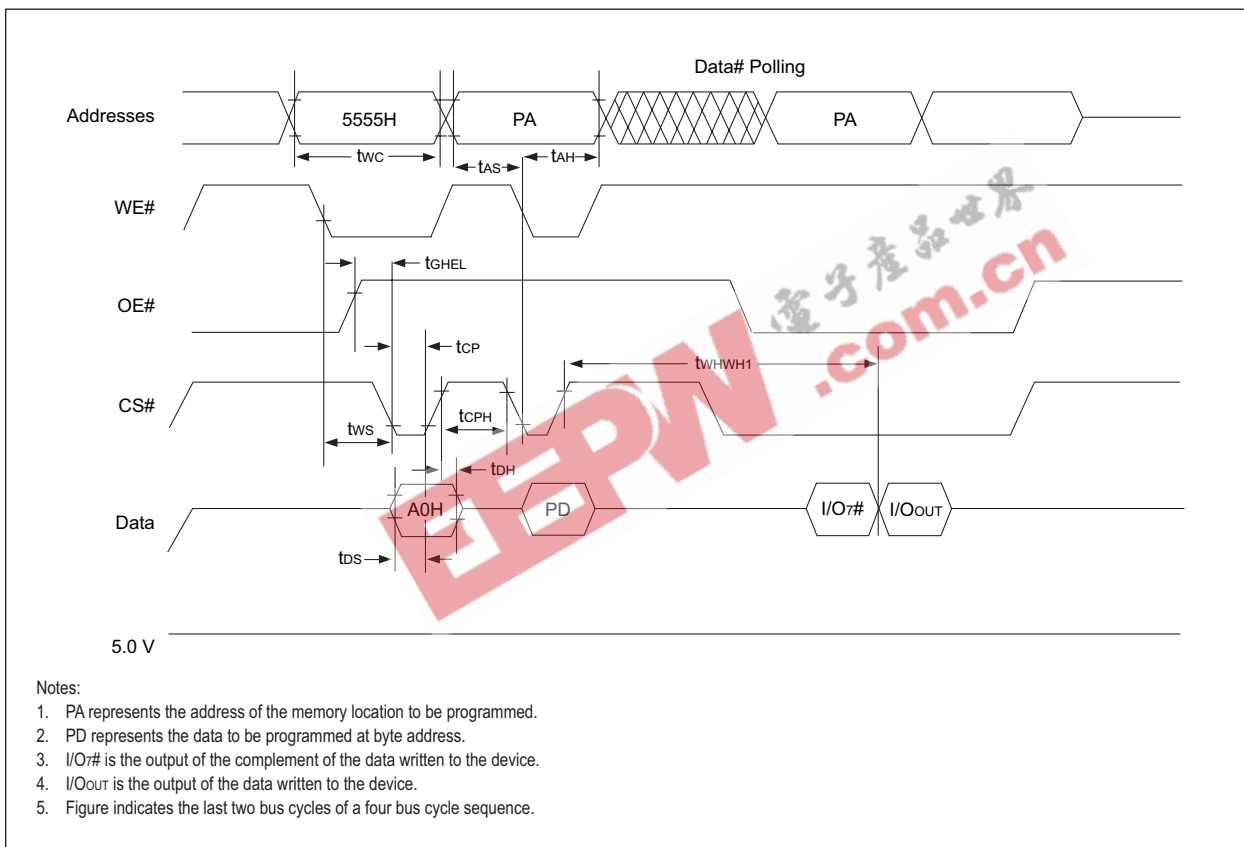


AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS



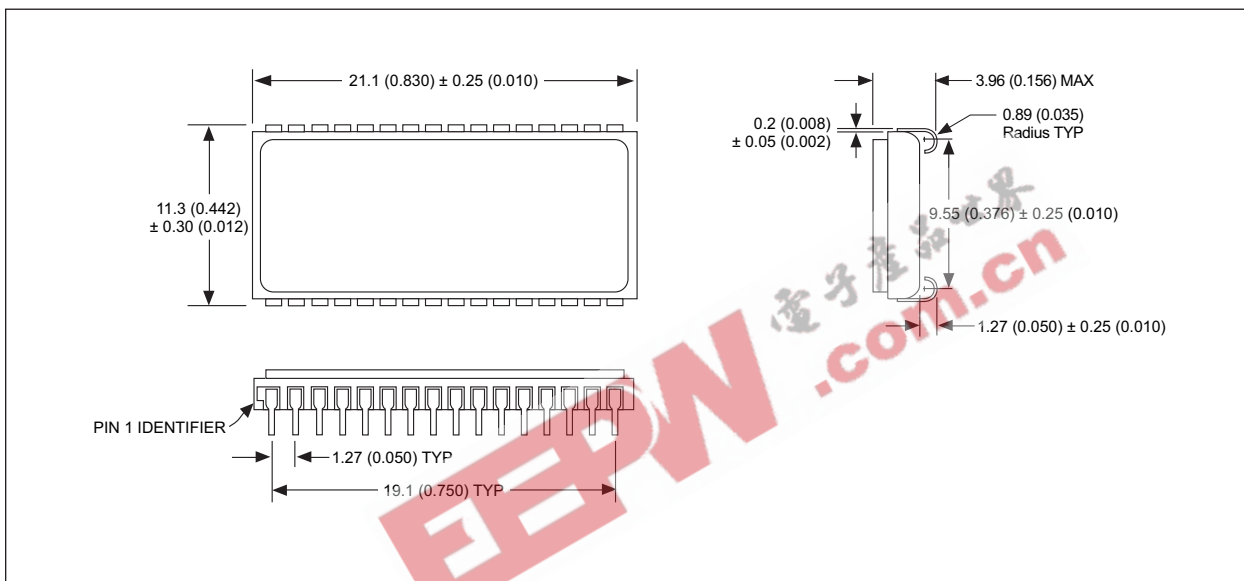


ALTERNATE CS# CONTROLLED PROGRAMMING OPERATION TIMINGS



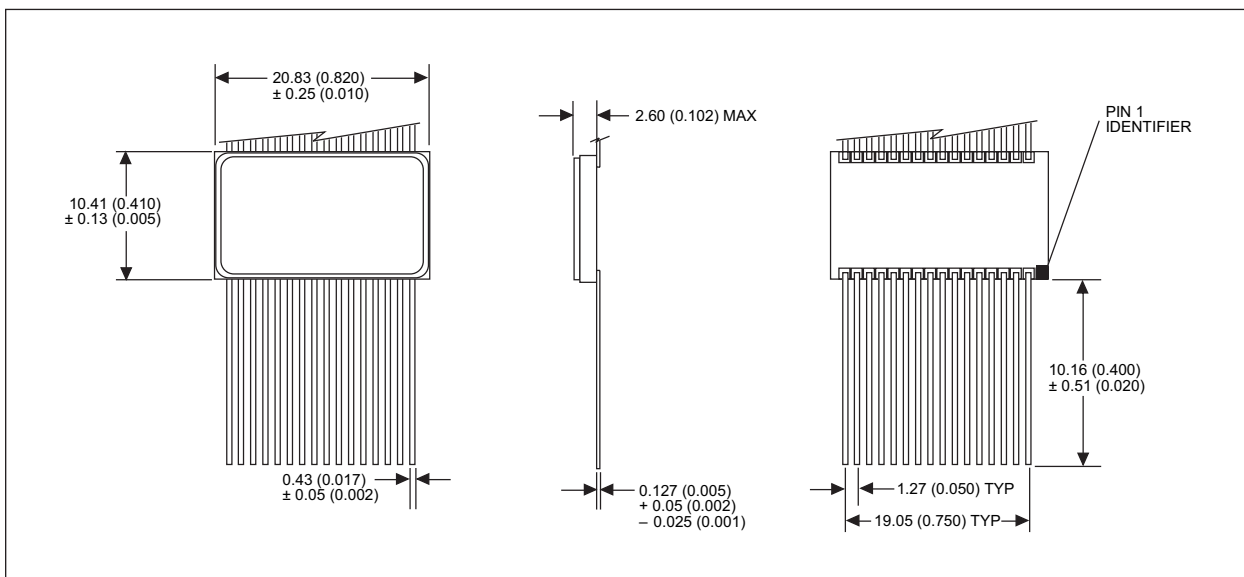


PACKAGE 101: 32 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 220: 32 LEAD, CERAMIC FLATPACK

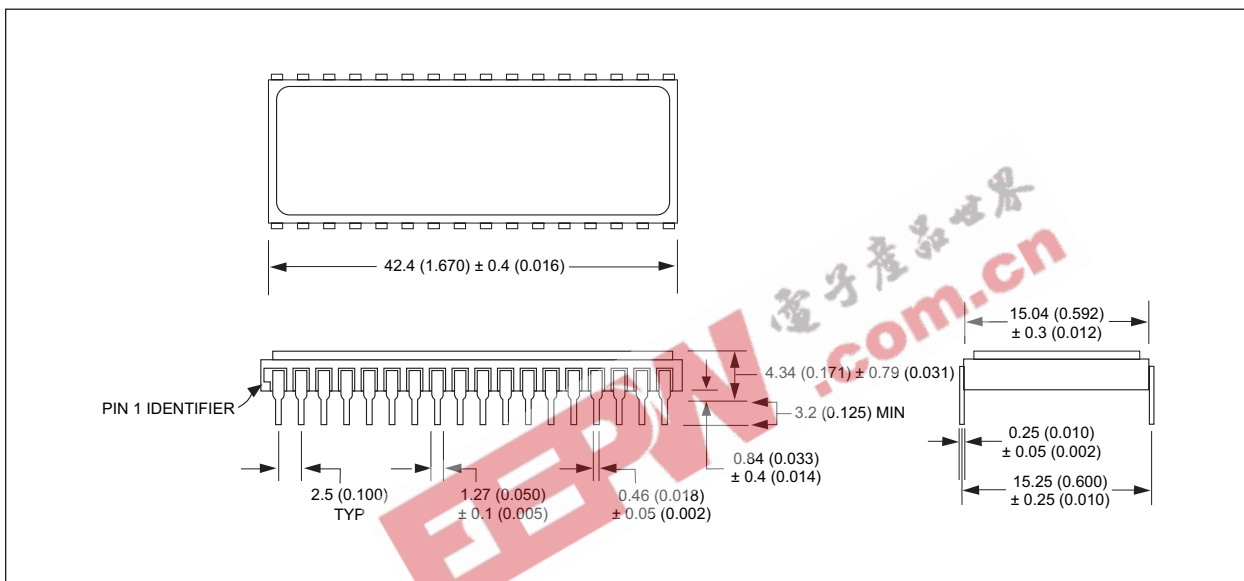


ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES





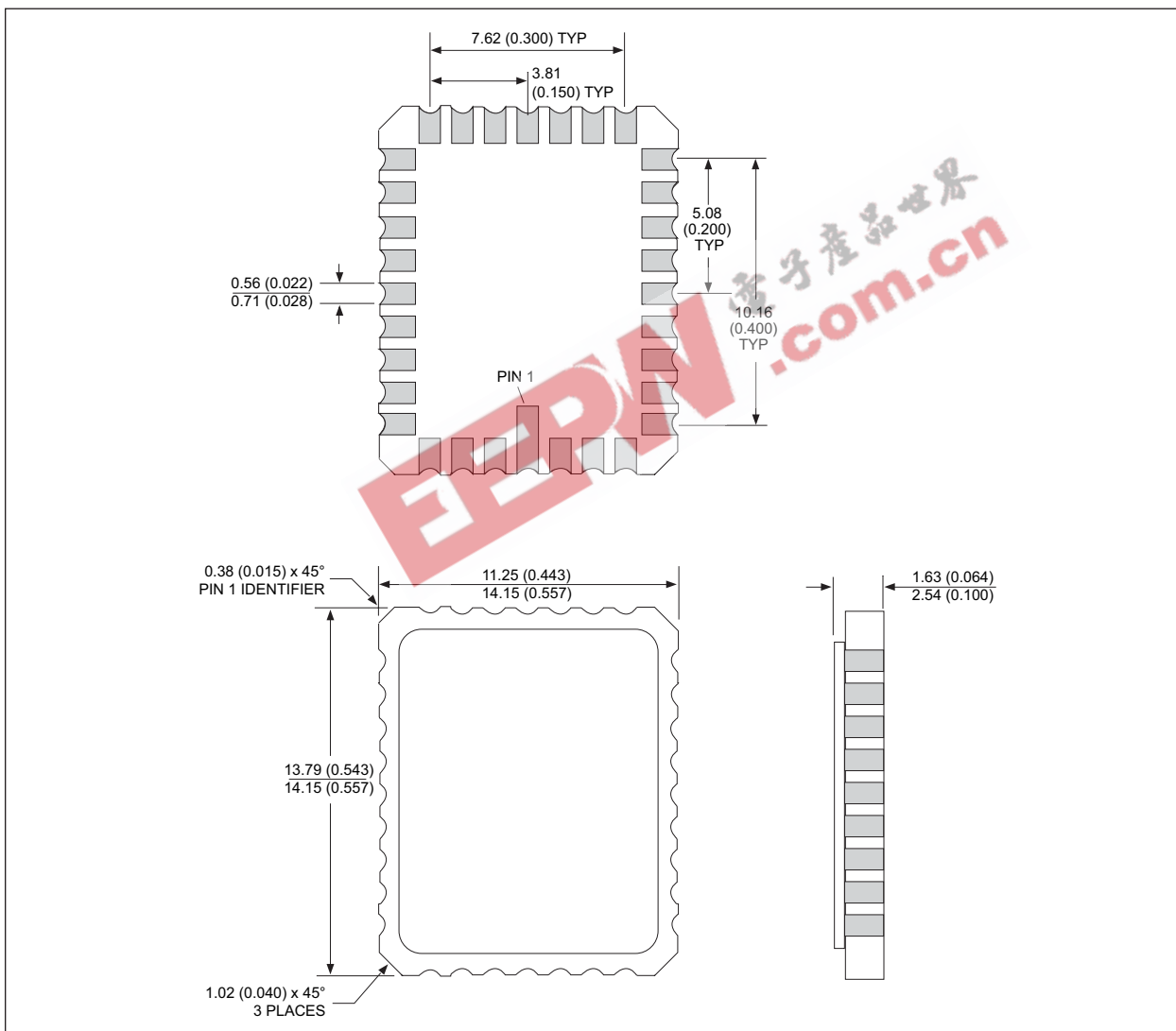
**PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 601: 32 PIN, RECTANGULAR CERAMIC LEADLESS CHIP CARRIER



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



**ORDERING INFORMATION**

W M F 512K 8 - XXX X X 5 X

WHITE ELECTRONIC DESIGNS CORP.

MONOLITHIC

Flash

ORGANIZATION, 512K x 8

ACCESS TIME (ns)

PACKAGE TYPE:

- C = 32 Pin Ceramic DIP (Package 300)
- CL = 32 Pin Rectangular Ceramic Leadless Chip Carrier (Package 601)
- DE = 32 Lead Ceramic SOJ (Package 101)
- FE = 32 Lead Flatpack (Package 220)

DEVICE GRADE:

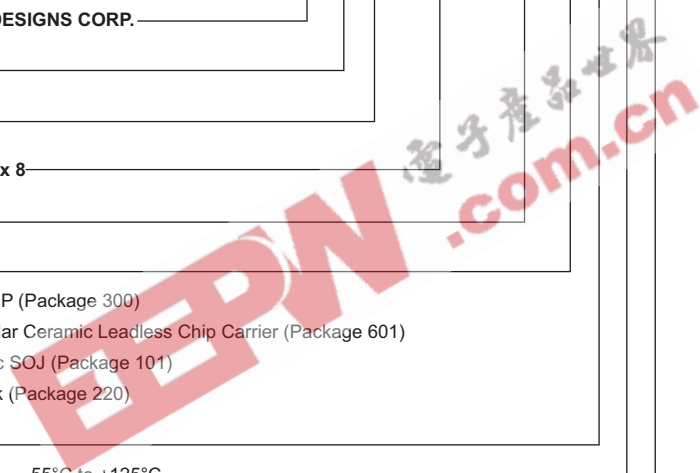
- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

V<sub>PP</sub> PROGRAMMING VOLTAGE

5 = 5V

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads





| DEVICE TYPE               | SECTOR SIZE | SPEED | PACKAGE               | SMD NO.          |
|---------------------------|-------------|-------|-----------------------|------------------|
| 512K x 8 Flash Monolithic | 64KByte     | 150ns | 32 pin DIP (C)        | 5962-96692 01HXX |
| 512K x 8 Flash Monolithic | 64KByte     | 120ns | 32 pin DIP (C)        | 5962-96692 02HXX |
| 512K x 8 Flash Monolithic | 64KByte     | 90ns  | 32 pin DIP (C)        | 5962-96692 03HXX |
| 512K x 8 Flash Monolithic | 64KByte     | 70ns  | 32 pin DIP (C)        | 5962-96692 04HXX |
| 512K x 8 Flash Monolithic | 64KByte     | 150ns | 32 lead SOJ (DE)      | 5962-96692 01HYX |
| 512K x 8 Flash Monolithic | 64KByte     | 120ns | 32 lead SOJ (DE)      | 5962-96692 02HYX |
| 512K x 8 Flash Monolithic | 64KByte     | 90ns  | 32 lead SOJ (DE)      | 5962-96692 03HYX |
| 512K x 8 Flash Monolithic | 64KByte     | 70ns  | 32 lead SOJ (DE)      | 5962-96692 04HYX |
| 512K x 8 Flash Monolithic | 64KByte     | 150ns | 32 lead Flatpack (FE) | 5962-96692 01HUX |
| 512K x 8 Flash Monolithic | 64KByte     | 120ns | 32 lead Flatpack (FE) | 5962-96692 02HUX |
| 512K x 8 Flash Monolithic | 64KByte     | 90ns  | 32 lead Flatpack (FE) | 5962-96692 03HUX |
| 512K x 8 Flash Monolithic | 64KByte     | 70ns  | 32 lead Flatpack (FE) | 5962-96692 04HUX |
| 512K x 8 Flash Monolithic | 64KByte     | 150ns | 32 lead Flatpack (FF) | 5962-96692 01HTX |
| 512K x 8 Flash Monolithic | 64KByte     | 120ns | 32 lead Flatpack (FF) | 5962-96692 02HTX |
| 512K x 8 Flash Monolithic | 64KByte     | 90ns  | 32 lead Flatpack (FF) | 5962-96692 03HTX |
| 512K x 8 Flash Monolithic | 64KByte     | 70ns  | 32 lead Flatpack (FF) | 5962-96692 04HTX |

**Document Title**

512K x 8 Flash Monolithic

**Revision History**

| Rev #  | History   | Release Date   | Status      |
|--|---|----------------|-------------|
| Rev 1  | Initial Release   | September 1996 | Preliminary |
|  | Changes (Pg. 1)   | May 1997       | Final       |
|  | 1.1 Change status to Final                              |                |             |
|  | Changes (Pg. 1)   | February 1998  | Final       |
|  | 1.1 Correct typo of Ceramic                             |                |             |
|  | Changes (Pg. 10)  | April 1998     | Final       |
|  | 1.1 Remove pedestal from Flatpack package drawing       |                |             |
| Rev 2  | Changes (Pg. 1)   | February 1999  | Final       |
|  | 1.1 Change name from 'FP' to Flatpack                   |                |             |
| Rev 2  | Changes (Pg. 1, 2, 3, 4, 13)                            | May 1999       | Final       |
|  | 2.1 Change number of max program/erases to 1,000,000    |                |             |
|  | 2.2 Change temperature of max program/erases to 25C     |                |             |
|  | 2.3 Absolute Maximum Ratings Table:                     |                |             |
|  | 2.3.1 Change Data Retention to 20years                  |                |             |
|  | 2.3.2 Change Endurance to 100,000 cycles minimum        |                |             |
|  | 2.4 Write/Erase/Program Operations Tables:              |                |             |
|  | 2.4.1 Change $t_{WHWH1}$ to 300 $\mu$ s                 |                |             |
|  | 2.4.2 Add Note (1) Typical $t_{WHWH1} = 7\mu$ s         |                |             |
|  | 2.4.3 Change $t_{WHWH2}$ to 15sec                       |                |             |
|  | 2.4.4 Add Note (2) Typical $t_{WHWH2} = 1$ sec          |                |             |
|  | 2.4.5 Change Chip Programming Time to 11 sec            |                |             |
|  | 2.4.6 Change Chip Erase Time to 64 sec                  |                |             |
|  | 2.4.7 Add Note (3) Chip Erase Time = 8 sec              |                |             |
|  | 2.5 Ordering Information                                |                |             |
|  | 2.5.1 Change Company Name to White EDC                  |                |             |
|  | 2.6 Change Title Style to new WEDC look                 |                |             |
| Rev 3  | Changes (Pg. 1, 2, 10, 12, 13)                          | May 1999       | Final       |
|  | 3.1 Change package 206 to package 220                   |                |             |
|  | 3.2 Remove temperature range notice for Endurance       |                |             |
| Rev 4  | 3.3 Change width spec to 0.457" minimum for package 601 |                |             |
|  | Changes (Pg. 1, 3, 4)                                   | January 2003   | Final       |
| 4.1 Add 60ns speed grade option                    |   |                |             |
| Rev 5  | Changes (Pg. 1, 11, 13)                                 | April 2005     | Final       |
|  | 5.1 Add 'T' case outline for 'FF' package               |                |             |
| Rev 6  | Changes (Pg. 1, 13)                                     | November 2005  | Final       |
|  | 6.1 Change revision history Rev 2.4.1 to 300 $\mu$ s    |                |             |
| 6.2 Change revision history Rev 2.4.2 to 7 $\mu$ s |   |                |             |