



## 128Kx8 MONOLITHIC FLASH, SMD 5962-96690

### FEATURES

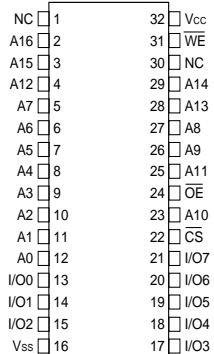
- Access Times of 50\*, 60, 70, 90, 120, 150ns
- Packaging
  - 32 lead, Hermetic Ceramic, 0.400" SOJ (Package 101)
  - 32 pin, Hermetic Ceramic, 0.600" DIP (Package 300)
  - 32 lead, Flatpack (Package 220)
  - 32 lead, Formed Flatpack (Package 221)
  - 32 pin, Rectangular Ceramic Leadless Chip Carrier (Package 601)
- 100,000 Erase/Program Cycles Minimum
- Sector Erase Architecture
  - 8 equal size sectors of 16KBytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 128Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Programming. 5V ±10% Supply.
- Low Power CMOS
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Page Program Operation and Internal Program Control Time.

*Note: For programming information refer to Flash Programming 1M5 Application Note.*

*\* The access time of 50ns is available in Industrial and Commercial temperature ranges only.*

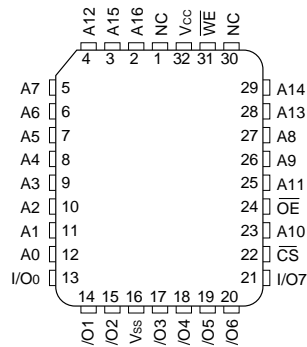
#### PIN CONFIGURATION FOR WMF128K8-XXX5

32 DIP  
32 CSOJ  
32 FLATPACK  
TOP VIEW



#### PIN CONFIGURATION FOR WMF128K8-XCLX5

32 CLCC  
TOP VIEW



#### PIN DESCRIPTION

A0-16	Address Inputs
I/O0-7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vcc	+5.0V Power
Vss	Ground



**ABSOLUTE MAXIMUM RATINGS (1)**

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage Range (Vcc)	-2.0 to +7.0	V
Signal voltage range (any pin except A9) (2)	-2.0 to +7.0	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Data Retention Mil Temp	10	years
Endurance (write/erase cycles) Mil Temp	10,000 min.	cycles
A9 Voltage for sector protect (V <sub>ID</sub> ) (3)	-2.0 to +14.0	V

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Input High Voltage	V <sub>IH</sub>	2.0	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.5	+0.8	V
Operating Temp. (Mil.)	T <sub>A</sub>	-55	+125	°C
Operating Temp. (Ind.)	T <sub>A</sub>	-40	+85	°C
A9 Voltage for Sector Protect	V <sub>ID</sub>	11.5	12.5	V

**CAPACITANCE**  
(T<sub>A</sub> = +25°C)

Parameter	Symbol	Conditions	Max	Unit
Address Input capacitance	C <sub>AD</sub>	V <sub>I/O</sub> = 0 V, f = 1.0 MHz	15	pF
Output Enable capacitance	C <sub>OE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	15	pF
Write Enable capacitance	C <sub>WE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	15	pF
Chip Select capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	15	pF
Data I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V, f = 1.0 MHz	15	pF

This parameter is guaranteed by design but not tested.

**NOTES:**

- Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot V<sub>SS</sub> to -2.0 V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is V<sub>CC</sub> + 0.5V. During voltage transitions, outputs may overshoot to V<sub>CC</sub> + 2.0 V for periods of up to 20ns.
- Minimum DC input voltage on A9 pin is -0.5V. During voltage transitions, A9 may overshoot V<sub>SS</sub> to -2V for periods of up to 20ns. Maximum DC input voltage on A9 is +13.5V which may overshoot to 14.0 V for periods up to 20ns.

**DC CHARACTERISTICS - CMOS COMPATIBLE**  
(V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10	µA
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10	µA
V <sub>CC</sub> Active Current for Read (1)	I <sub>CC1</sub>	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}$		35	mA
V <sub>CC</sub> Active Current for Program or Erase (2)	I <sub>CC2</sub>	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}$		50	mA
V <sub>CC</sub> Standby Current	I <sub>CC3</sub>	V <sub>CC</sub> = 5.5, $\overline{CS} = V_{IH}, f = 5\text{MHz}$		1.6	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0 mA, V <sub>CC</sub> = 4.5		0.45	V
Output High Voltage	V <sub>OH1</sub>	I <sub>OH</sub> = -2.5 mA, V <sub>CC</sub> = 4.5	0.85 x V <sub>CC</sub>		V
Output High Voltage	V <sub>OH2</sub>	I <sub>OH</sub> = -100 µA, V <sub>CC</sub> = 4.5	V <sub>CC</sub> - 0.4		V
Low V <sub>CC</sub> Lock Out Voltage	V <sub>LKO</sub>		3.2		V

**NOTES:**

- The I<sub>CC</sub> current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with  $\overline{OE}$  at V<sub>IH</sub>.
- I<sub>CC</sub> active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions: V<sub>IL</sub> = 0.3V, V<sub>IH</sub> = V<sub>CC</sub> - 0.3V

**AC TEST CIRCUIT**

The diagram shows an AC test circuit for a device under test (D.U.T.). It consists of a bridge circuit with four resistors. Two current sources are connected to the top and bottom nodes of the bridge, with currents labeled I<sub>OL</sub> and I<sub>OH</sub>. The D.U.T. is connected to the left node of the bridge. A capacitor C<sub>eff</sub> = 50 pf is connected to the left node. The right node of the bridge is connected to a bipolar supply V<sub>Z</sub> ≈ 1.5V. The bridge resistors are labeled with their respective current sources.

**AC TEST CONDITIONS**

Parameter	Typ	Unit
Input Pulse Levels	V <sub>IL</sub> = 0, V <sub>IH</sub> = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

**NOTES:**  
V<sub>Z</sub> is programmable from -2V to +7V.  
I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.  
Tester Impedance Z<sub>0</sub> = 75 Ω.  
V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.  
I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.  
ATE tester includes jig capacitance.



**AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS,  $\overline{WE}$  CONTROLLED**  
 (Vcc = 5.0V, Vss = 0V, TA = -55°C to +125°C)

Parameter	Symbol		-50		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	50		60		70		90		120		150		ns
Chip Select Setup Time	tELWL	tCS	0		0		0		0		0		0		ns
Write Enable Pulse Width	twLWH	tWP	25		30		35		45		50		50		ns
Address Setup Time	tAVWL	tAS	0		0		0		0		0		0		ns
Data Setup Time	tdVWH	tDS	25		30		30		45		50		50		ns
Data Hold Time	tWHDX	tDH	0		0		0		0		0		0		ns
Address Hold Time	twLAX	tAH	40		45		45		45		50		50		ns
Chip Select Hold Time	twHEH	tCH	0		0		0		0		0		0		ns
Write Enable Pulse Width High	twHWL	tWPH	20		20		20		20		20		20		ns
Duration of Byte Programming Operation (min)	twHWH1		14		14		14		14		14		14		μs
Sector Erase Time	twHWH2		2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	sec
Read Recovery Time Before Write	tGHWL		0		0		0		0		0		0		ns
Vcc Setup Time	tvCS		50		50		50		50		50		50		μs
Chip Programming Time				12.5		12.5		12.5		12.5		12.5		12.5	sec
Output Enable Setup Time	toES		0		0		0		0		0		0		ns
Output Enable Hold Time (1)	toEH		10		10		10		10		10		10		ns

1. For Toggle and Data Polling.

**AC CHARACTERISTICS – READ ONLY OPERATIONS**  
 (Vcc = 5.0V, Vss = 0V, TA = -55°C to +125°C)

Parameter	Symbol		-50		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Read Cycle Time	tAVAV	trc	50		60		70		90		120		150		ns
Address Access Time	tAVQV	tACC		50		60		70		90		120		150	ns
Chip Select Access Time	tELOV	tCE		50		60		70		90		120		150	ns
$\overline{OE}$ to Output Valid	tGLOV	toE		25		30		35		40		50		55	ns
Chip Select to Output High Z (1)	teHOZ	toF		20		20		20		25		30		35	ns
$\overline{OE}$ High to Output High Z (1)	tGHOZ	toF		20		20		20		25		30		35	ns
Output Hold from Address, CS or $\overline{OE}$ Change, whichever is first	tAXQX	toH	0		0		0		0		0		0		ns

1. Guaranteed by design, not tested.

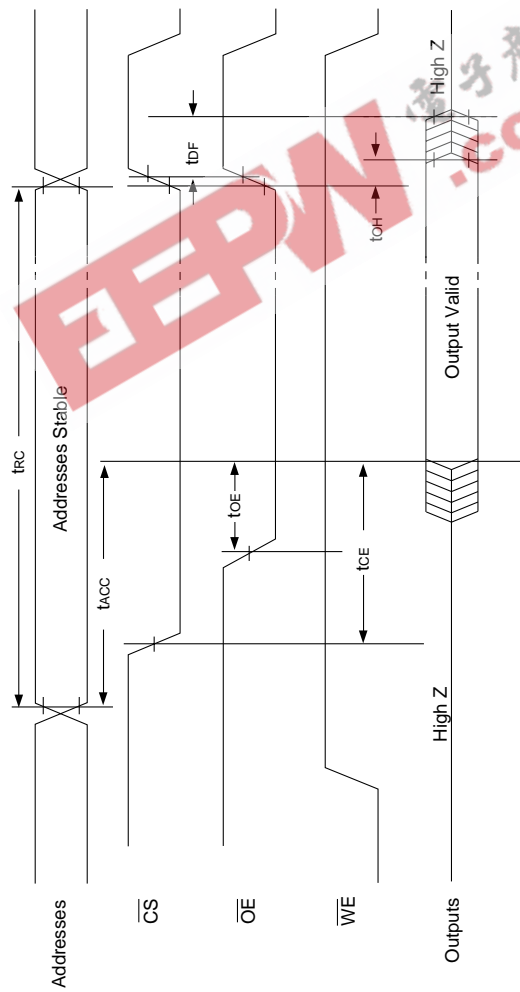


**AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS,  $\overline{CS}$  CONTROLLED**  
 (V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol		-50		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>AVAV</sub>	t <sub>WC</sub>	50		60		70		90		120		150		ns
$\overline{WE}$ Setup Time	t <sub>WLLEL</sub>	t <sub>WS</sub>	0		0		0		0		0		0		ns
$\overline{CS}$ Pulse Width	t <sub>ELEH</sub>	t <sub>CP</sub>	25		30		35		45		50		50		ns
Address Setup Time	t <sub>AVEL</sub>	t <sub>AS</sub>	0		0		0		0		0		0		ns
Data Setup Time	t <sub>DVEH</sub>	t <sub>DS</sub>	25		30		30		45		50		50		ns
Data Hold Time	t <sub>EHDX</sub>	t <sub>DH</sub>	0		0		0		0		0		0		ns
Address Hold Time	t <sub>ELAX</sub>	t <sub>AH</sub>	40		45		45		45		50		50		ns
$\overline{WE}$ Hold from $\overline{WE}$ High	t <sub>EHWH</sub>	t <sub>WH</sub>	0		0		0		0		0		0		ns
$\overline{CS}$ Pulse Width High	t <sub>EHEL</sub>	t <sub>CPH</sub>	20		20		20		20		20		20		ns
Duration of Programming Operation	t <sub>WHWH1</sub>		14		14		14		14		14		14		μs
Duration of Erase Operation	t <sub>WHWH2</sub>		2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	sec
Read Recovery before Write	t <sub>GHLEL</sub>		0		0		0		0		0		0		ns
Chip Programming Time				12.5		12.5		12.5		12.5		12.5		12.5	sec

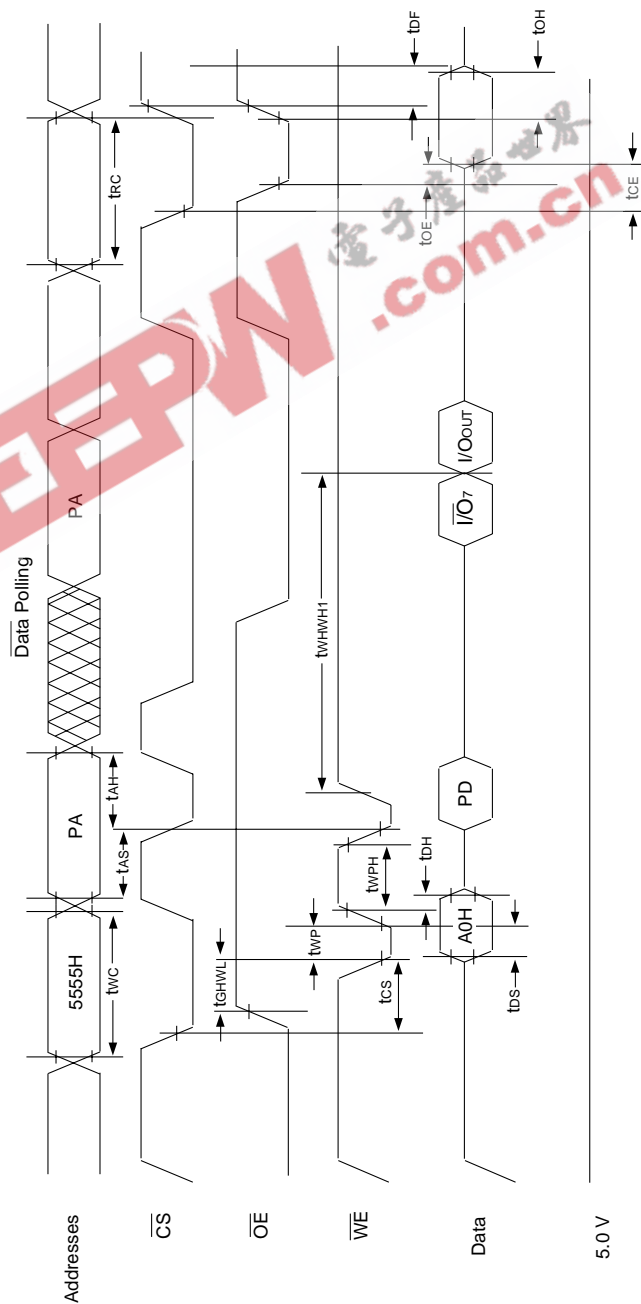


AC WAVEFORMS FOR READ OPERATIONS





WRITE/ERASE/PROGRAM OPERATION, WE CONTROLLED

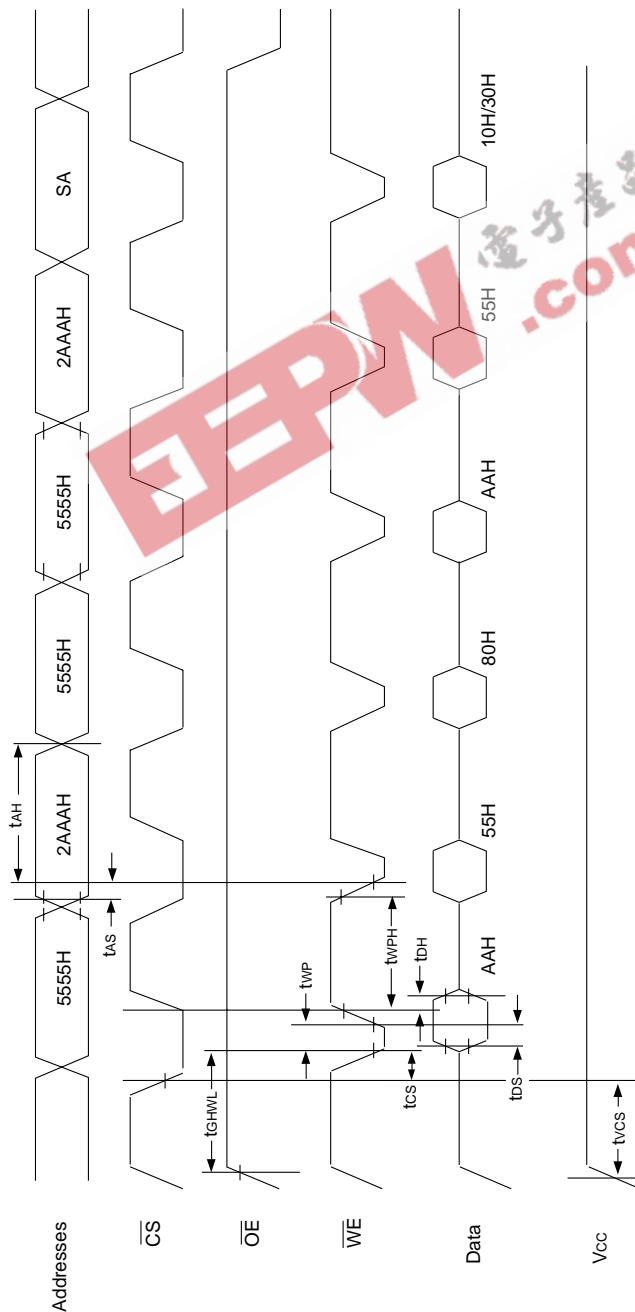


NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. I/O7 is the output of the complement of the data written to the device.
4. I/Oout is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.



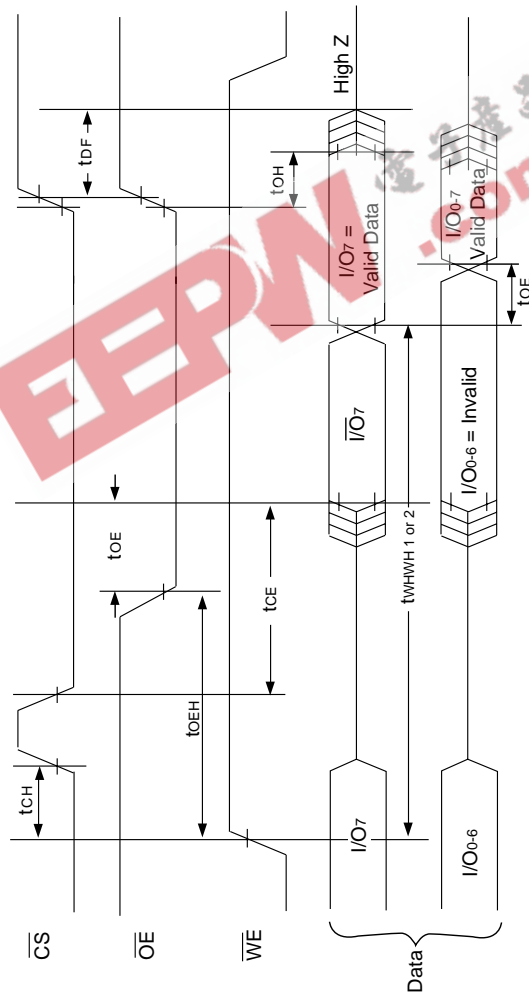
AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



**NOTES:**  
1. SA is the sector address for Sector Erase.



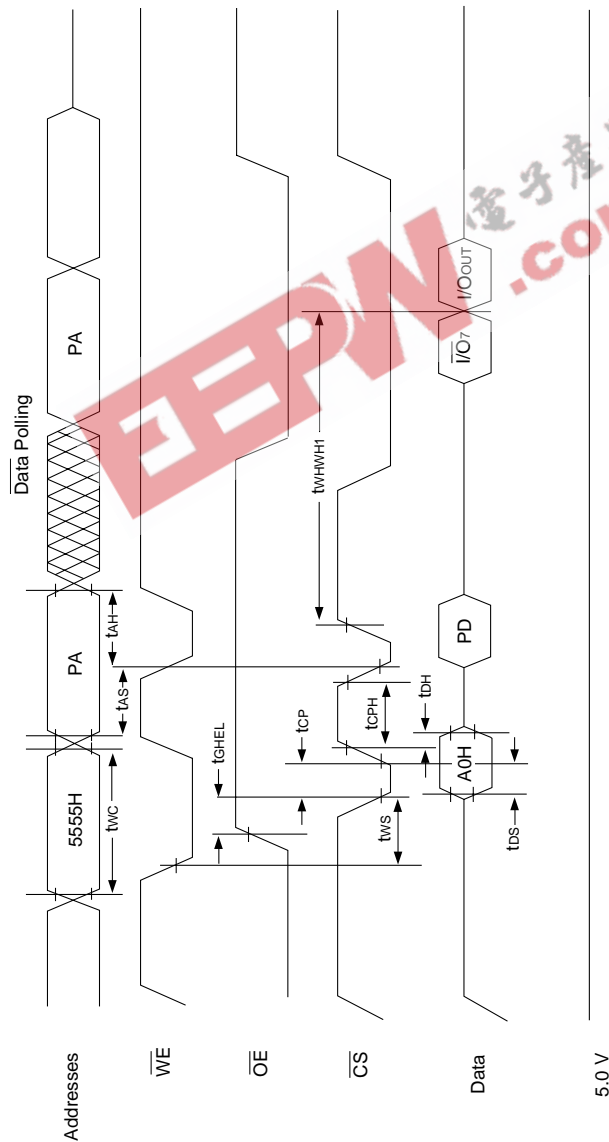
AC WAVEFORMS FOR DATA POLLING DURING EMBEDDED ALGORITHM OPERATIONS







WRITE/ERASE/PROGRAM OPERATION,  $\overline{CS}$  CONTROLLED

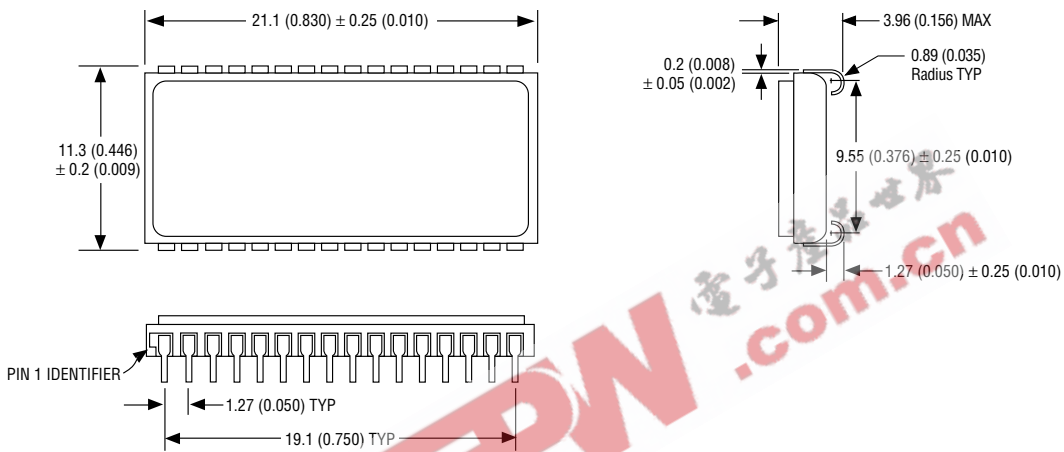


NOTES:

- 1. PA represents the address of the memory location to be programmed.
- 2. PD represents the data to be programmed at byte address.
- 3.  $\overline{I/O}$  is the output of the complement of the data written to the device.
- 4.  $\overline{I/Oout}$  is the output of the data written to the device.
- 5. Figure indicates the last two bus cycles of a four bus cycle sequence.

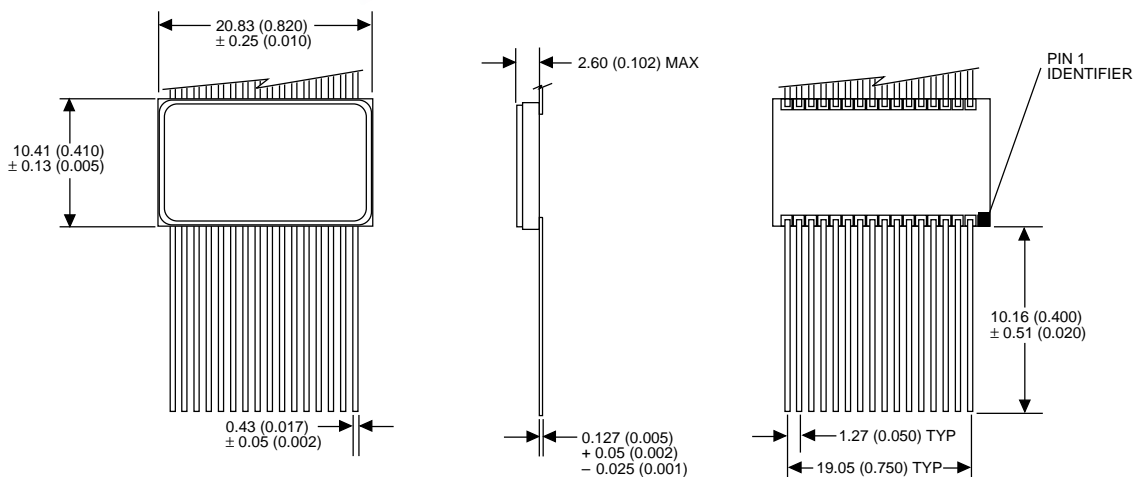


**PACKAGE 101: 32 LEAD, CERAMIC SOJ**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

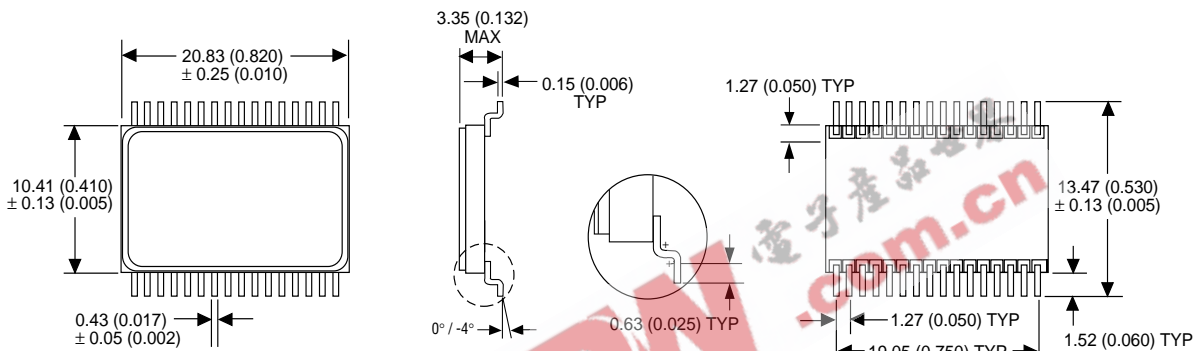
**PACKAGE 220: 32 LEAD, CERAMIC FLATPACK**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

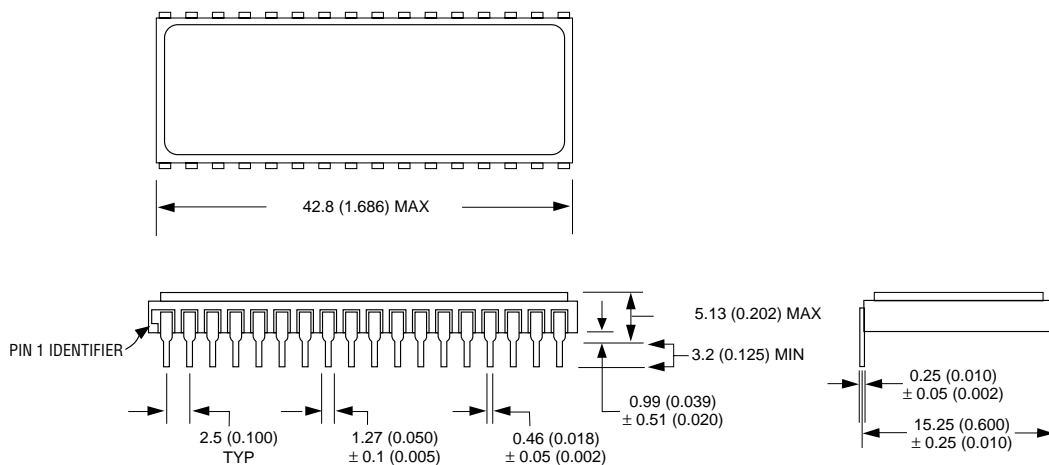


**PACKAGE 221: 32 LEAD, FORMED CERAMIC FLATPACK**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

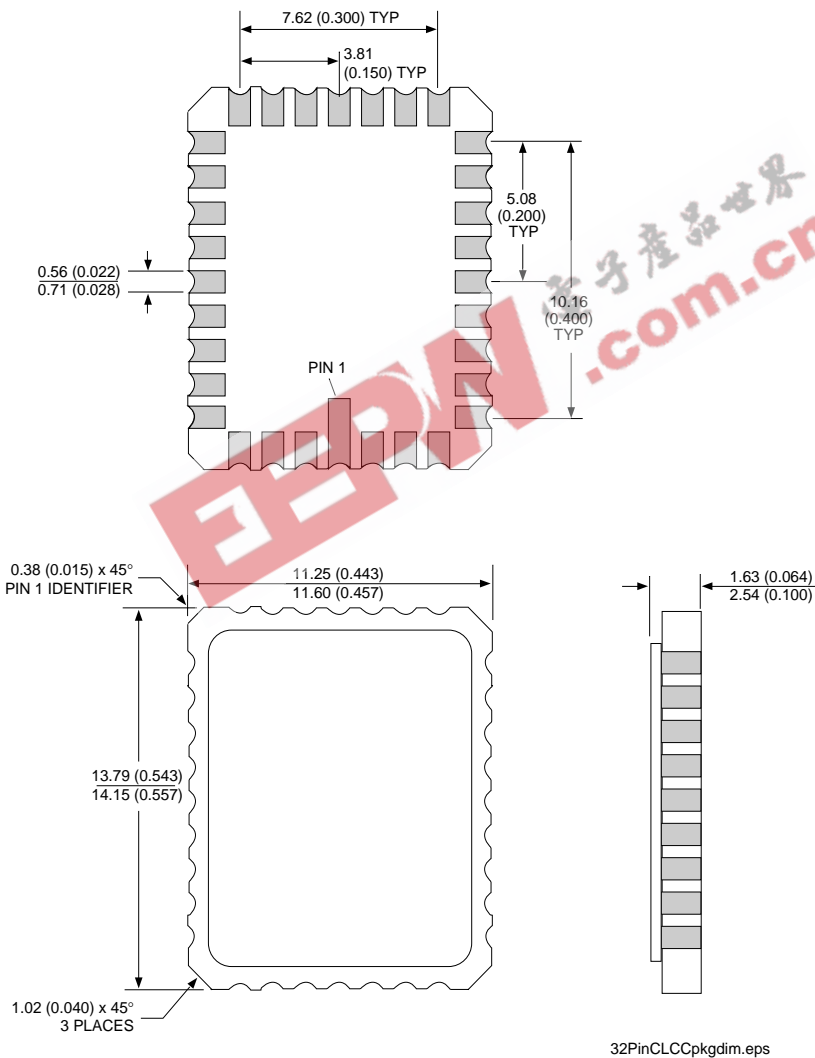
**PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



**PACKAGE 601: 32 PIN, RECTANGULAR CERAMIC LEADLESS CHIP CARRIER**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

W M F 128K8 - XXX X X 5 X

LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

V<sub>PP</sub> PROGRAMMING VOLTAGE

5 = 5V

DEVICE GRADE:

Q = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

PACKAGE TYPE:

DE = 32 Lead Ceramic SOJ (Package 101)

C = 32 Pin Ceramic DIP (Package 300)

FE = 32 Lead Ceramic Flatpack (Package 220)

FF = 32 Lead Formed Ceramic Flatpack (Package 221)

CL = 32 Pin rectangular Ceramic Leadless Chip Carrier (Package 601)

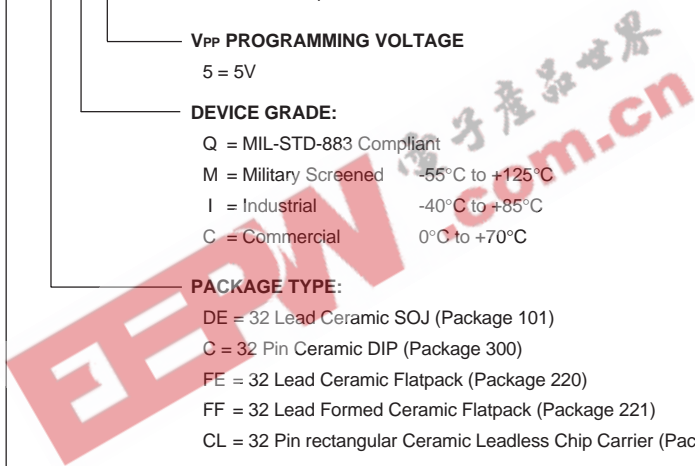
ACCESS TIME (ns)

ORGANIZATION, 128K x 8

Flash

MONOLITHIC

WHITE ELECTRONIC DESIGNS CORP.





DEVICE TYPE	SECTOR SIZE	SPEED	PACKAGE	SMD NO.
128K x 8 Flash Monolithic	16KByte	150ns	32 pin DIP (C)	5962-96690 01HYX
128K x 8 Flash Monolithic	16KByte	120ns	32 pin DIP (C)	5962-96690 02HYX
128K x 8 Flash Monolithic	16KByte	90ns	32 pin DIP (C)	5962-96690 03HYX
128K x 8 Flash Monolithic	16KByte	70ns	32 pin DIP (C)	5962-96690 04HYX
128K x 8 Flash Monolithic	16KByte	60ns	32 pin DIP (C)	5962-96690 05HYX
128K x 8 Flash Monolithic	16KByte	150ns	32 lead SOJ (DE)	5962-96690 01HXX
128K x 8 Flash Monolithic	16KByte	120ns	32 lead SOJ (DE)	5962-96690 02HXX
128K x 8 Flash Monolithic	16KByte	90ns	32 lead SOJ (DE)	5962-96690 03HXX
128K x 8 Flash Monolithic	16KByte	70ns	32 lead SOJ (DE)	5962-96690 04HXX
128K x 8 Flash Monolithic	16KByte	60ns	32 lead SOJ (DE)	5962-96690 05HXX
128K x 8 Flash Monolithic	16KByte	150ns	32 lead Flatpack (FE)	5962-96690 01HTX
128K x 8 Flash Monolithic	16KByte	120ns	32 lead Flatpack (FE)	5962-96690 02HTX
128K x 8 Flash Monolithic	16KByte	90ns	32 lead Flatpack (FE)	5962-96690 03HTX
128K x 8 Flash Monolithic	16KByte	70ns	32 lead Flatpack (FE)	5962-96690 04HTX
128K x 8 Flash Monolithic	16KByte	60ns	32 lead Flatpack (FE)	5962-96690 05HTX
128K x 8 Flash Monolithic	16KByte	150ns	32 lead Formed Flatpack (FF)	5962-96690 01HUX
128K x 8 Flash Monolithic	16KByte	120ns	32 lead Formed Flatpack (FF)	5962-96690 02HUX
128K x 8 Flash Monolithic	16KByte	90ns	32 lead Formed Flatpack (FF)	5962-96690 03HUX
128K x 8 Flash Monolithic	16KByte	70ns	32 lead Formed Flatpack (FF)	5962-96690 04HUX
128K x 8 Flash Monolithic	16KByte	60ns	32 lead Formed Flatpack (FF)	5962-96690 05HUX