



## 512Kx8 MONOLITHIC FLASH, SMD 5962-96692

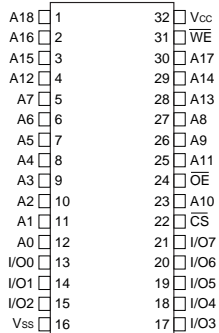
### FEATURES

- Access Times of 70, 90, 120, 150ns
- Packaging
  - 32 pin, Hermetic Ceramic, 0.600" DIP (Package 300)
  - 32 lead, Hermetic Ceramic, 0.400" SOJ (Package 101)
  - 32 pin, Rectangular Ceramic Leadless Chip Carrier (Package 601)
  - 32 lead Flatpack (Package 220)
- 1,000,000 Erase/Program Cycles Minimum
- Sector Erase Architecture
  - 8 equal size sectors of 64K bytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Programming. 5V ±10% Supply.
- Low Power CMOS
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Page Program Operation and Internal Program Control Time.

*Note: For programming information refer to Flash Programming 4M5 Application Note.*

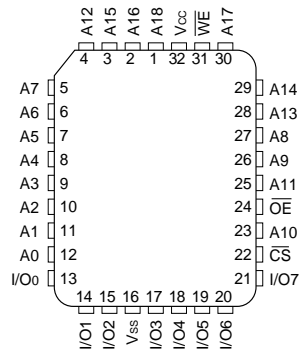
#### PIN CONFIGURATION FOR WMF512K8-XXX5

32 DIP  
32 CSOJ  
32 Flatpack  
TOP VIEW



#### PIN CONFIGURATION FOR WMF512K8-XCLX5

32 CLCC  
TOP VIEW



#### PIN DESCRIPTION

|        |                   |
|--------|-------------------|
| A0-18  | Address Inputs    |
| I/O0-7 | Data Input/Output |
| CS     | Chip Select       |
| OE     | Output Enable     |
| WE     | Write Enable      |
| Vcc    | +5.0V Power       |
| Vss    | Ground            |



**ABSOLUTE MAXIMUM RATINGS (1)**

| Parameter  |               | Unit   |
|--|---------------|--------|
| Operating Temperature  | -55 to +125   | °C     |
| Supply Voltage (V <sub>CC</sub> ) (1)                            | -2.0 to +7.0  | V      |
| Signal Voltage Range(any pin except A <sub>9</sub> ) (2)         | -2.0 to +7.0  | V      |
| Storage Temperature Range  | -65 to +150   | °C     |
| Lead Temperature (soldering, 10 seconds)                         | +300          | °C     |
| Data Retention Mil Temp  | 20            | years  |
| Endurance - erase/program cycles (Mil Temp)                      | 100,000 min   | cycles |
| A <sub>9</sub> Voltage for sector protect (V <sub>ID</sub> ) (3) | -2.0 to +14.0 | V      |

**NOTES:**

1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot V<sub>SS</sub> to -2.0 V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is V<sub>CC</sub> + 0.5V. During voltage transitions, outputs may overshoot to V<sub>CC</sub> + 2.0 V for periods of up to 20ns.
3. Minimum DC input voltage on A<sub>9</sub> pin is -0.5V. During voltage transitions, A<sub>9</sub> may overshoot V<sub>SS</sub> to -2V for periods of up to 20ns. Maximum DC input voltage on A<sub>9</sub> is +13.5V which may overshoot to 14.0 V for periods up to 20ns.

**RECOMMENDED OPERATING CONDITIONS**

| Parameter                                 | Symbol          | Min  | Max                   | Unit |
|---|-----------------|------|-----------------------|------|
| Supply Voltage                            | V <sub>CC</sub> | 4.5  | 5.5                   | V    |
| Input High Voltage                        | V <sub>IH</sub> | 2.0  | V <sub>CC</sub> + 0.5 | V    |
| Input Low Voltage                         | V <sub>IL</sub> | -0.5 | +0.8                  | V    |
| Operating Temp. (Mil.)                    | T <sub>A</sub>  | -55  | +125                  | °C   |
| Operating Temp. (Ind.)                    | T <sub>A</sub>  | -40  | +85                   | °C   |
| A <sub>9</sub> Voltage for Sector Protect | V <sub>ID</sub> | 11.5 | 12.5                  | V    |

**CAPACITANCE**

(T<sub>A</sub> = +25°C)

| Parameter                 | Symbol           | Conditions                          | Max | Unit |
|---------------------------|------------------|-------------------------------------|-----|------|
| Address Input capacitance | C <sub>AD</sub>  | V <sub>I/O</sub> = 0 V, f = 1.0 MHz | 15  | pF   |
| Output Enable capacitance | C <sub>OE</sub>  | V <sub>IN</sub> = 0 V, f = 1.0 MHz  | 15  | pF   |
| Write Enable capacitance  | C <sub>WE</sub>  | V <sub>IN</sub> = 0 V, f = 1.0 MHz  | 15  | pF   |
| Chip Select capacitance   | C <sub>CS</sub>  | V <sub>IN</sub> = 0 V, f = 1.0 MHz  | 15  | pF   |
| Data I/O capacitance      | C <sub>I/O</sub> | V <sub>I/O</sub> = 0 V, f = 1.0 MHz | 15  | pF   |

This parameter is guaranteed by design but not tested.

**DC CHARACTERISTICS - CMOS COMPATIBLE**

(V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C to +125°C)

| Parameter   | Symbol             | Conditions  |                        |      | Unit |
|---|--------------------|---|------------------------|------|------|
|   |                    |   | Min                    | Max  |      |
| Input Leakage Current                                   | I <sub>LI</sub>    | V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>   |                        | 10   | µA   |
| Output Leakage Current                                  | I <sub>LOx32</sub> | V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>   |                        | 10   | µA   |
| V <sub>CC</sub> Active Current for Read (1)             | I <sub>CC1</sub>   | $\overline{CS} = V_{IL}, \overline{OE} = V_{IH}, f = 5\text{MHz}$ |                        | 50   | mA   |
| V <sub>CC</sub> Active Current for Program or Erase (2) | I <sub>CC2</sub>   | $\overline{CS} = V_{IL}, \overline{OE} = V_{IH}$                  |                        | 60   | mA   |
| V <sub>CC</sub> Standby Current                         | I <sub>CC4</sub>   | V <sub>CC</sub> = 5.5, $\overline{CS} = V_{IH}, f = 5\text{MHz}$  |                        | 1.6  | mA   |
| Output Low Voltage                                      | V <sub>OL</sub>    | I <sub>OL</sub> = 8.0 mA, V <sub>CC</sub> = 4.5                   |                        | 0.45 | V    |
| Output High Voltage                                     | V <sub>OH1</sub>   | I <sub>OH</sub> = -2.5 mA, V <sub>CC</sub> = 4.5                  | 0.85 x V <sub>CC</sub> |      | V    |
| Low V <sub>CC</sub> Lock-Out Voltage                    | V <sub>LKO</sub>   |   | 3.2                    | 4.2  | V    |

**NOTES:**

1. The I<sub>CC</sub> current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with  $\overline{OE}$  at V<sub>IH</sub>.
2. I<sub>CC</sub> active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: V<sub>IL</sub> = 0.3V, V<sub>IH</sub> = V<sub>CC</sub> - 0.3V



**AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS,  $\overline{CS}$  CONTROLLED**

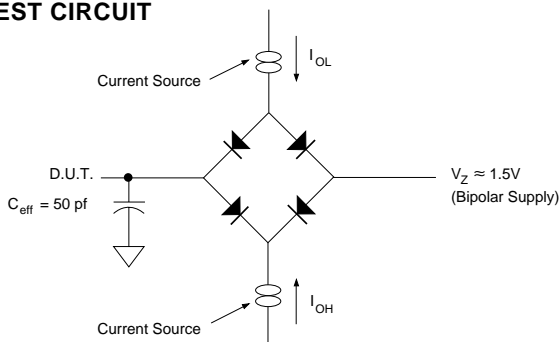
( $V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55^{\circ}C$  to  $+125^{\circ}C$ )

| Parameter                                  | Symbol |      | -70 |     | -90 |     | -120 |     | -150 |     | Unit    |
|--|--------|------|-----|-----|-----|-----|------|-----|------|-----|---------|
|  |        |      | Min | Max | Min | Max | Min  | Max |      |     |         |
| Write Cycle Time                           | tAVAV  | tWC  | 70  |     | 90  |     | 120  |     | 150  |     | ns      |
| Write Enable Setup Time                    | tWLLEL | tWS  | 0   |     | 0   |     | 0    |     | 0    |     | ns      |
| Chip Select Pulse Width                    | tELEH  | tCP  | 45  |     | 45  |     | 50   |     | 50   |     | ns      |
| Address Setup Time                         | tAVEL  | tAS  | 0   |     | 0   |     | 0    |     | 0    |     | ns      |
| Data Setup Time                            | tDVEH  | tDS  | 45  |     | 45  |     | 50   |     | 50   |     | ns      |
| Data Hold Time                             | tEHDX  | tDH  | 0   |     | 0   |     | 0    |     | 0    |     | ns      |
| Address Hold Time                          | tELAX  | tAH  | 45  |     | 45  |     | 50   |     | 50   |     | ns      |
| Chip Select Pulse Width High               | tEHEL  | tCPH | 20  |     | 20  |     | 20   |     | 20   |     | ns      |
| Duration of Byte Programming Operation (1) | tWHWH1 |      |     | 300 |     | 300 |      | 300 |      | 300 | $\mu$ s |
| Sector Erase Time (2)                      | tWHWH2 |      |     | 15  |     | 15  |      | 15  |      | 15  | sec     |
| Read Recovery Time                         | tGHEL  |      | 0   |     | 0   |     | 0    |     | 0    |     | ns      |
| Chip Programming Time                      |        |      |     | 11  |     | 11  |      | 11  |      | 11  | sec     |
| Chip Erase Time (3)                        |        |      |     | 64  |     | 64  |      | 64  |      | 64  | sec     |

**NOTES:**

1. Typical value for tWHWH1 is 7 $\mu$ s.
2. Typical value for tWHWH2 is 1sec.
3. Typical value for Chip Erase time is 8sec.

**AC TEST CIRCUIT**



**AC TEST CONDITIONS**

| Parameter                        | Typ                        | Unit |
|----------------------------------|----------------------------|------|
| Input Pulse Levels               | $V_{IL} = 0, V_{IH} = 3.0$ | V    |
| Input Rise and Fall              | 5                          | ns   |
| Input and Output Reference Level | 1.5                        | V    |
| Output Timing Reference Level    | 1.5                        | V    |

**NOTES:**

- $V_z$  is programmable from -2V to +7V.
- $I_{OL}$  &  $I_{OH}$  programmable from 0 to 16mA.
- Tester Impedance  $Z_0 = 75 \Omega$ .
- $V_z$  is typically the midpoint of  $V_{OH}$  and  $V_{OL}$ .
- $I_{OL}$  &  $I_{OH}$  are adjusted to simulate a typical resistive load circuit.
- ATE tester includes jig capacitance.



**AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS,  $\overline{WE}$  CONTROLLED**

(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = -55°C to +125°C)

| Parameter                                  | Symbol |      | -70 |     | -90 |     | -120 |     | -150 |     | Unit |
|--|--------|------|-----|-----|-----|-----|------|-----|------|-----|------|
|  |        |      | Min | Max | Min | Max | Min  | Max | Min  | Max |      |
| Write Cycle Time                           | tAVAV  | tWC  | 70  |     | 90  |     | 120  |     | 150  |     | ns   |
| Chip Select Setup Time                     | tELWL  | tCS  | 0   |     | 0   |     | 0    |     | 0    |     | ns   |
| Write Enable Pulse Width                   | tWLWH  | tWP  | 45  |     | 45  |     | 50   |     | 50   |     | ns   |
| Address Setup Time                         | tAVWH  | tAS  | 0   |     | 0   |     | 0    |     | 0    |     | ns   |
| Data Setup Time                            | tDVWH  | tDS  | 45  |     | 45  |     | 50   |     | 50   |     | ns   |
| Data Hold Time                             | tWHDX  | tDH  | 0   |     | 0   |     | 0    |     | 0    |     | ns   |
| Address Hold Time                          | tWHAX  | tAH  | 45  |     | 45  |     | 50   |     | 50   |     | ns   |
| Write Enable Pulse Width High              | tWHWL  | tWPH | 20  |     | 20  |     | 20   |     | 20   |     | ns   |
| Duration of Byte Programming Operation (1) | tWHWH1 |      |     | 300 |     | 300 |      | 300 |      | 300 | μs   |
| Sector Erase Time (2)                      | tWHWH2 |      |     | 15  |     | 15  |      | 15  |      | 15  | sec  |
| Read Recovery Time before Write            | tGHWL  |      | 0   |     | 0   |     | 0    |     | 0    |     | ms   |
| V <sub>CC</sub> Set-up Time                |        | tVCS | 50  |     | 50  |     | 50   |     | 50   |     | μs   |
| Chip Programming Time                      |        |      |     | 11  |     | 11  |      | 11  |      | 11  | sec  |
| Output Enable Setup Time                   |        | tOES | 0   |     | 0   |     | 0    |     | 0    |     | ns   |
| Output Enable Hold Time (4)                |        | tOEH | 10  |     | 10  |     | 10   |     | 10   |     | ns   |
| Chip Erase Time (3)                        |        |      |     | 64  |     | 64  |      | 64  |      | 64  | sec  |

**NOTES:**

1. Typical value for t<sub>WHWH1</sub> is 7μs.
2. Typical value for t<sub>WHWH2</sub> is 1sec.
3. Typical value for Chip Erase time is 8sec.
4. For Toggle and Data Polling.

**AC CHARACTERISTICS – READ ONLY OPERATIONS**

(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = -55°C to +125°C)

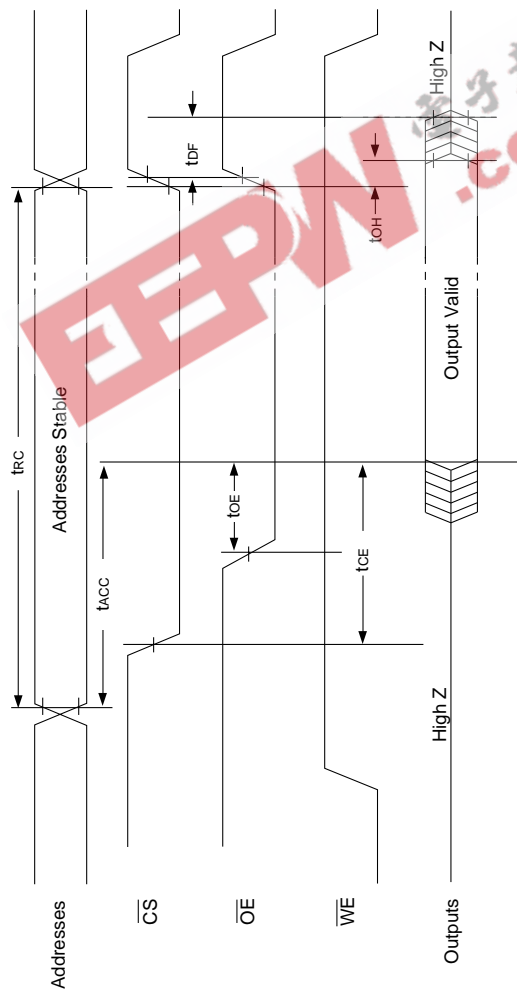
| Parameter   | Symbol |      | -70 |     | -90 |     | -120 |     | -150 |     | Unit |
|---|--------|------|-----|-----|-----|-----|------|-----|------|-----|------|
|   |        |      | Min | Max | Min | Max | Min  | Max | Min  | Max |      |
| Read Cycle Time   | tAVAV  | tRC  | 70  |     | 90  |     | 120  |     | 150  |     | ns   |
| Address Access Time   | tAVOV  | tACC |     | 70  |     | 90  |      | 120 |      | 150 | ns   |
| Chip Select Access Time   | tELQV  | tCE  |     | 70  |     | 90  |      | 120 |      | 150 | ns   |
| Output Enable to Output Valid   | tGLOV  | tOE  |     | 35  |     | 35  |      | 50  |      | 55  | ns   |
| Chip Select to Output High Z (1)  | tEHQZ  | tDF  |     | 20  |     | 20  |      | 30  |      | 35  | ns   |
| Output Enable High to Output High Z (1)   | tGHQZ  | tDF  |     | 20  |     | 20  |      | 30  |      | 35  | ns   |
| Output Hold from Address, $\overline{CS}$ or $\overline{OE}$ Change, whichever is First | tAXOX  | tOH  | 0   |     | 0   |     | 0    |     | 0    |     | ns   |

**NOTES:**

1. Guaranteed by design, but not tested

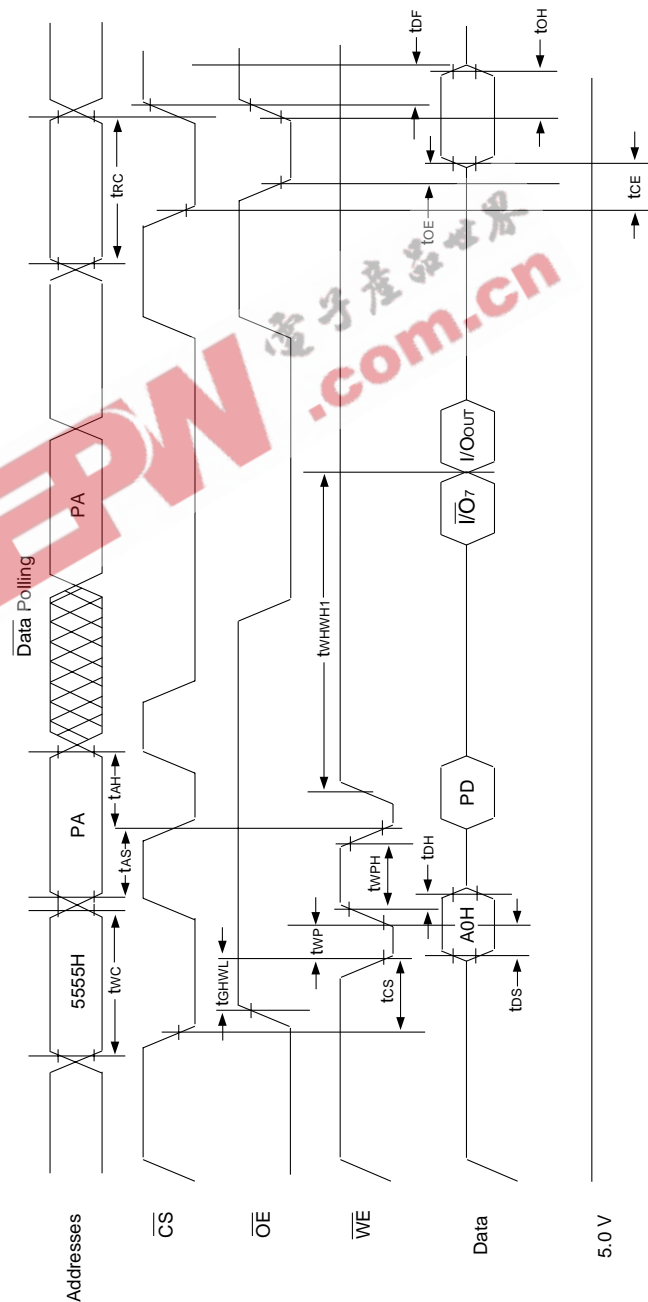


AC WAVEFORMS FOR READ OPERATIONS





**WRITE/ERASE/PROGRAM  
OPERATION, WE CONTROLLED**



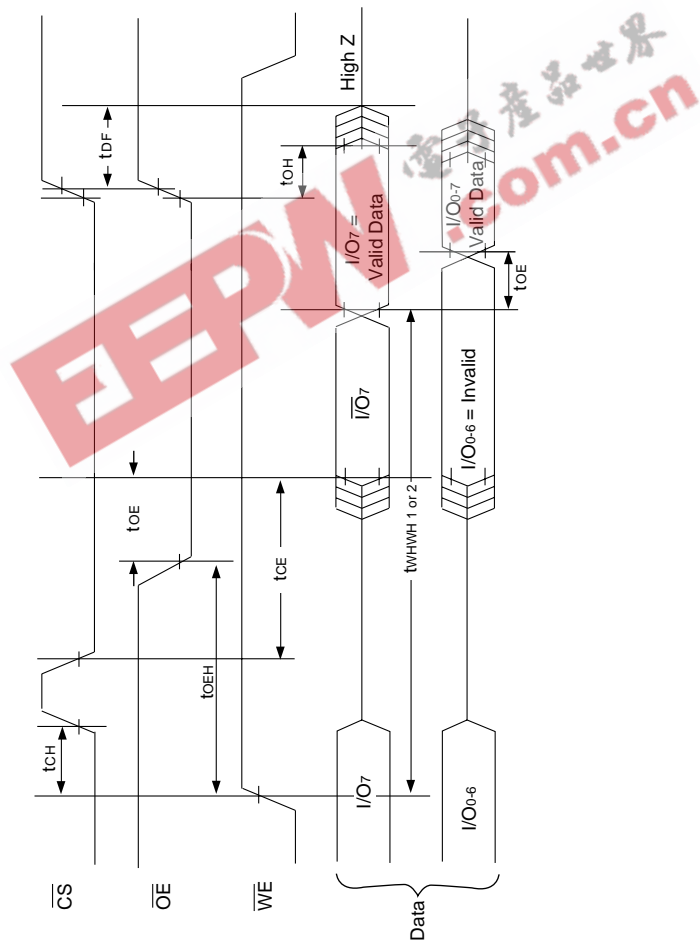
**NOTES:**

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. I/O is the output of the complement of the data written to the device.
4. I/Oout is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.





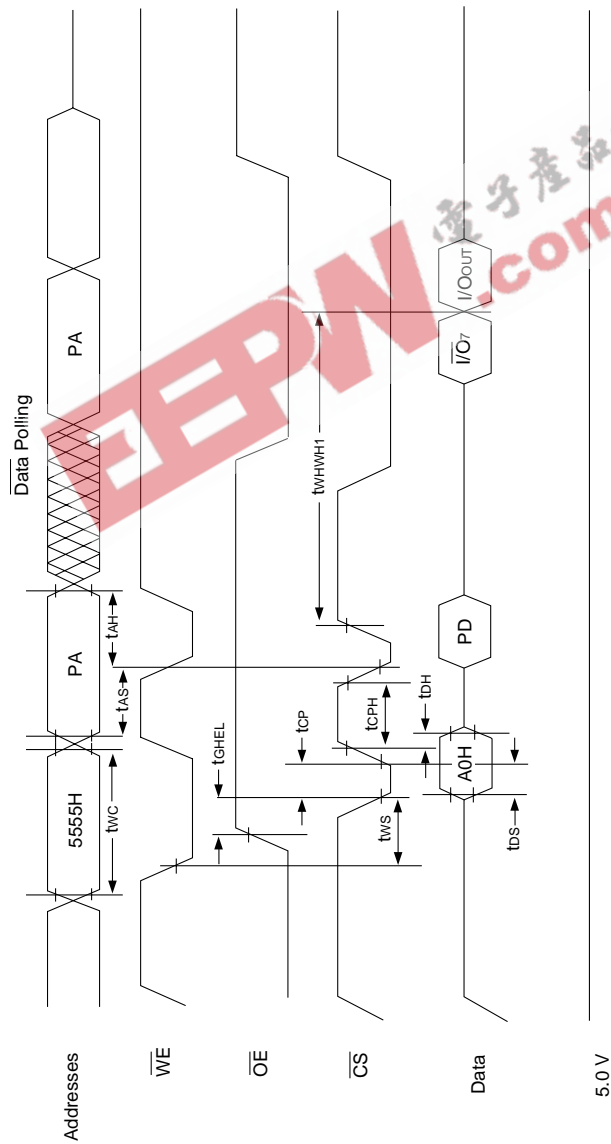
AC WAVEFORMS FOR DATA POLLING  
DURING EMBEDDED ALGORITHM OPERATIONS







ALTERNATE  $\overline{CS}$  CONTROLLED PROGRAMMING OPERATION TIMINGS

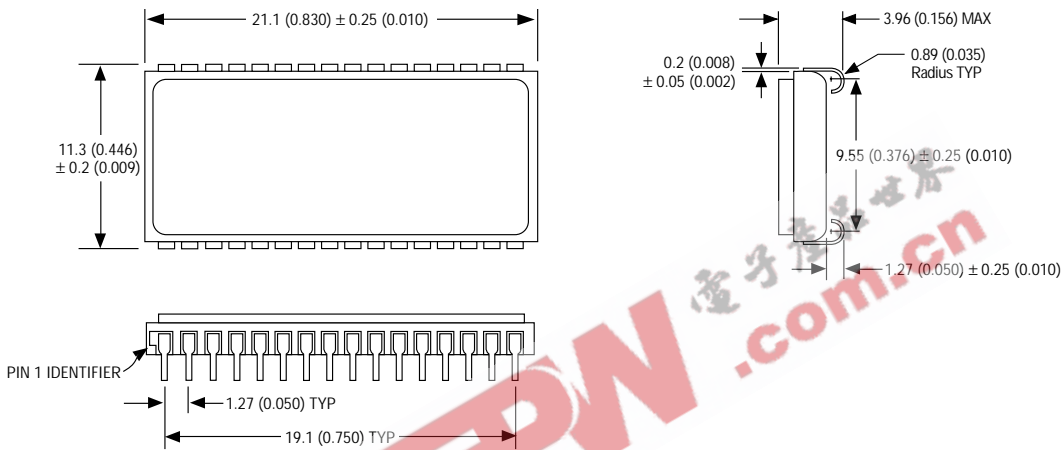


NOTES:

- 1. PA represents the address of the memory location to be programmed.
- 2. PD represents the data to be programmed at byte address.
- 3.  $\overline{I/O}$  is the output of the complement of the data written to the device.
- 4. I/Oout is the output of the data written to the device.
- 5. Figure indicates the last two bus cycles of a four bus cycle sequence.

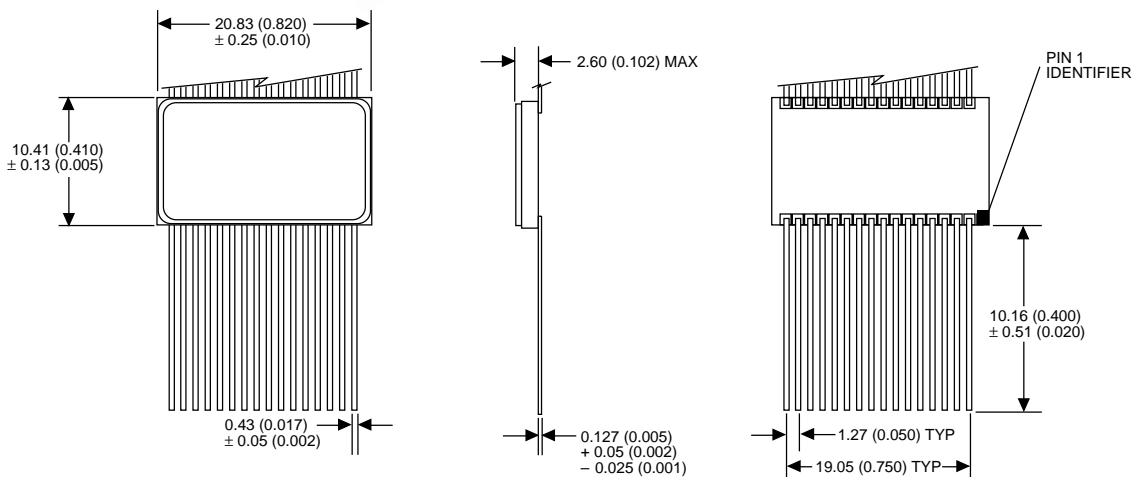


**PACKAGE 101: 32 LEAD, CERAMIC SOJ**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

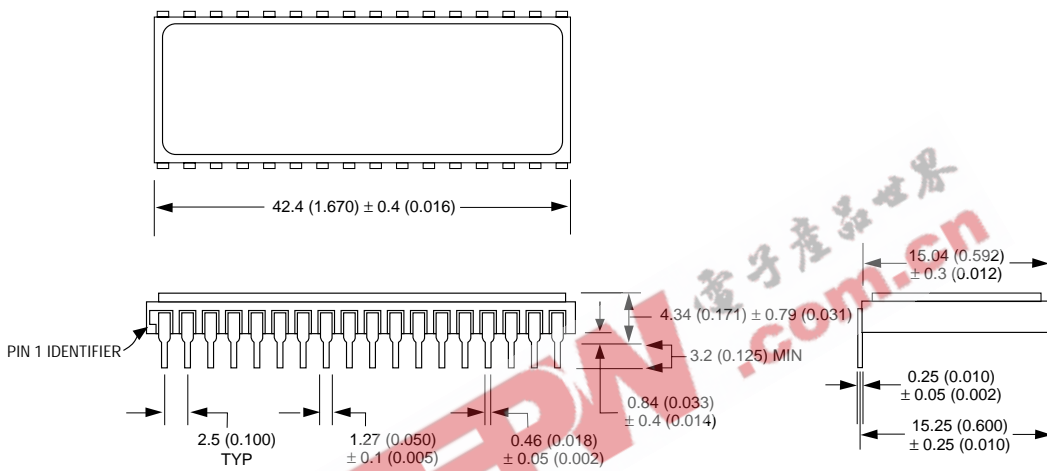
**PACKAGE 220: 32 LEAD, CERAMIC FLATPACK**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



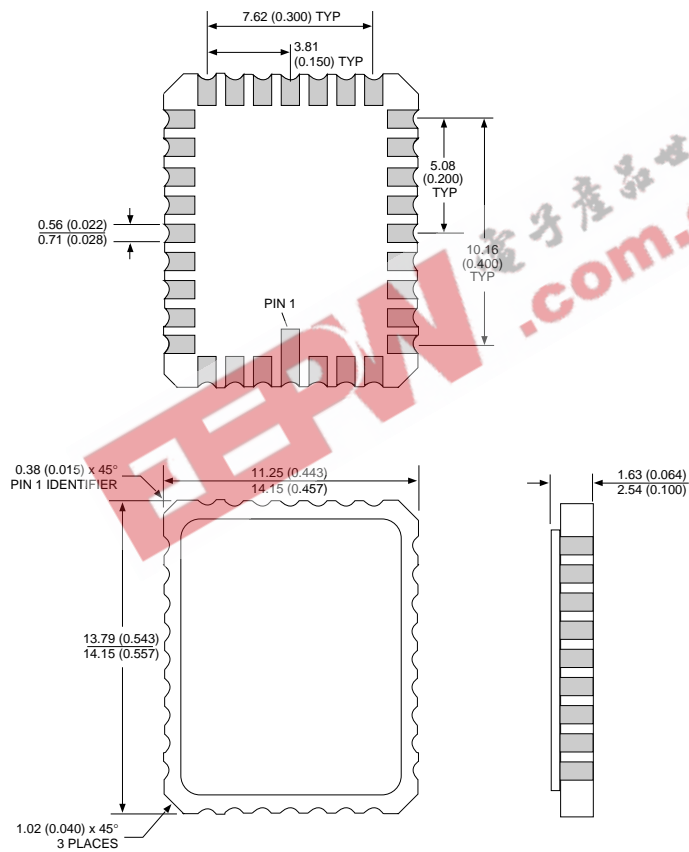
PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 601: 32 PIN, RECTANGULAR CERAMIC LEADLESS CHIP CARRIER



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



**ORDERING INFORMATION**

**W M F 512K 8 - XXX X X 5 X**

**LEAD FINISH:**

- Blank = Gold plated leads
- A = Solder dip leads

**V<sub>PP</sub> PROGRAMMING VOLTAGE**

5 = 5V

**DEVICE GRADE:**

- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

**PACKAGE TYPE:**

- C = 32 Pin Ceramic DIP (Package 300)
- CL = 32 Pin Rectangular Ceramic Leadless Chip Carrier (Package 601)
- DE = 32 Lead Ceramic SOJ (Package 101)
- FE = 32 Lead Flatpack (Package 220)

**ACCESS TIME (ns)**

**ORGANIZATION, 512K x 8**

Flash

MONOLITHIC

WHITE ELECTRONIC DESIGNS CORP.

| DEVICE TYPE               | SECTOR SIZE | SPEED | PACKAGE               | SMD NO.          |
|---------------------------|-------------|-------|-----------------------|------------------|
| 512K x 8 Flash Monolithic | 64KByte     | 150ns | 32 pin DIP (C)        | 5962-96692 01HXX |
| 512K x 8 Flash Monolithic | 64KByte     | 120ns | 32 pin DIP (C)        | 5962-96692 02HXX |
| 512K x 8 Flash Monolithic | 64KByte     | 90ns  | 32 pin DIP (C)        | 5962-96692 03HXX |
| 512K x 8 Flash Monolithic | 64KByte     | 70ns  | 32 pin DIP (C)        | 5962-96692 04HXX |
| 512K x 8 Flash Monolithic | 64KByte     | 150ns | 32 lead SOJ (DE)      | 5962-96692 01HYX |
| 512K x 8 Flash Monolithic | 64KByte     | 120ns | 32 lead SOJ (DE)      | 5962-96692 02HYX |
| 512K x 8 Flash Monolithic | 64KByte     | 90ns  | 32 lead SOJ (DE)      | 5962-96692 03HYX |
| 512K x 8 Flash Monolithic | 64KByte     | 70ns  | 32 lead SOJ (DE)      | 5962-96692 04HYX |
| 512K x 8 Flash Monolithic | 64KByte     | 150ns | 32 lead Flatpack (FE) | 5962-96692 01HUX |
| 512K x 8 Flash Monolithic | 64KByte     | 120ns | 32 lead Flatpack (FE) | 5962-96692 02HUX |
| 512K x 8 Flash Monolithic | 64KByte     | 90ns  | 32 lead Flatpack (FE) | 5962-96692 03HUX |
| 512K x 8 Flash Monolithic | 64KByte     | 70ns  | 32 lead Flatpack (FE) | 5962-96692 04HUX |