WM8753L

Hi-Fi and Telephony Dual CODEC

DESCRIPTION

The WM8753L is a low power, high quality stereo CODEC with integrated Voice CODEC designed for portable digital telephony applications such as mobile phone, or headset with Hi-Fi playback capability.

The device integrates dual interfaces to two differentially connected microphones, and includes drivers for speakers, headphone and earpiece. External component requirements are reduced as no separate microphone or headphone amplifiers are required, and Cap-less connections can be made to all loads. Advanced on-chip digital signal processing performs tone control, Bass Boost and automatic level control for the microphone or line input through the ADC. The two ADCs may be used to support Voice noise cancellation in a partnering DSP, or for stereo recording.

The WM8753L Hi-Fi DAC can operate as a master or a slave, with various master clock frequencies including 12 or 24MHz for USB devices, 13MHz or 19.2MHz for cellular systems, or standard 256fs rates like 12.288MHz and 24.576MHz. Internal PLLs generate all required clocks for both Voice and Hi-Fi converters. If audio system clocks already exist, the PLLs may be committed to alternative uses.

The WM8753L operates at a nominal supply voltage of 2V, although the digital core can operate at voltages down to 1.42V to save power, and the maximum for all supplies is 3.6 Volts. Different sections of the chip can also be powered down under software control.

FEATURES

- **Hi-Fi DAC:** interfaced over I²S type link
- Audio sample rates:
  8, 11.025, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96
- DAC SNR 98dB, THD -84dB ('A' weighted @ 48kHz)
- ADC SNR 95dB, THD -82dB ('A' weighted @ 48kHz)
- On-chip Headphone Driver with cap-less output option
  - 40mW output power on 16Ω / 3.3V
  - with 16Ω load: SNR 90dB, THD –75dB
  - with 10kΩ load: SNR 94dB, THD –90dB
- On-chip speaker driver with 0.5W into 8R
- **Voice CODEC:** interfaced over Voice interface
- supports sample rates from 8ks/s to 48ks/s
- ADC and DAC SNR 82dB, THD -74dB
- Two Differential Microphone Interfaces
  - Dual ADCs support noise cancellation in external DSP
  - Programmable ALC / Noise Gate
- Low-noise bias supplied for electret microphones

Other Features

- On-chip PLLs supporting 12, 13, 19.2MHz and other clocks
- Cap-less connection options to headphones, earpiece, spkr.
- Low power, low voltage
  - 1.8V to 3.6V (digital core: 1.42V to 3.6V)
  - power consumption <20mW all-on with 2V supplies
  - <12mW for PCM CODEC operation
- 7x7x0.9mm QFN package, 5x5x0.9mm BGA package

APPLICATIONS

- MP3 Player / Recorder mobile phone
- Bluetooth stereo headset

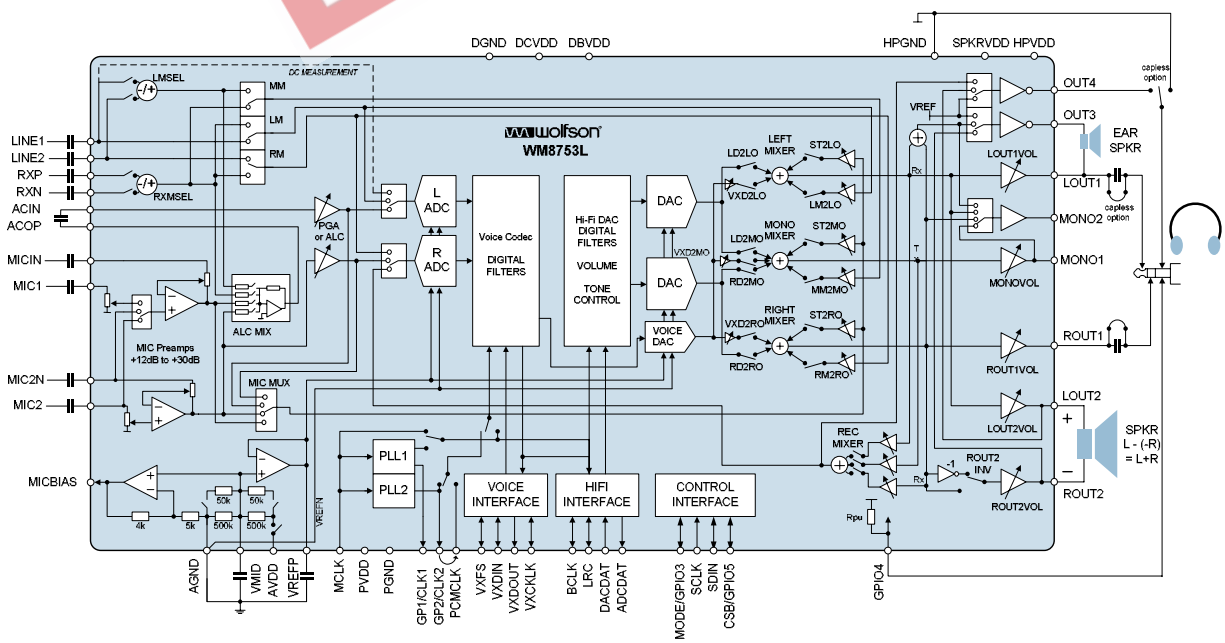
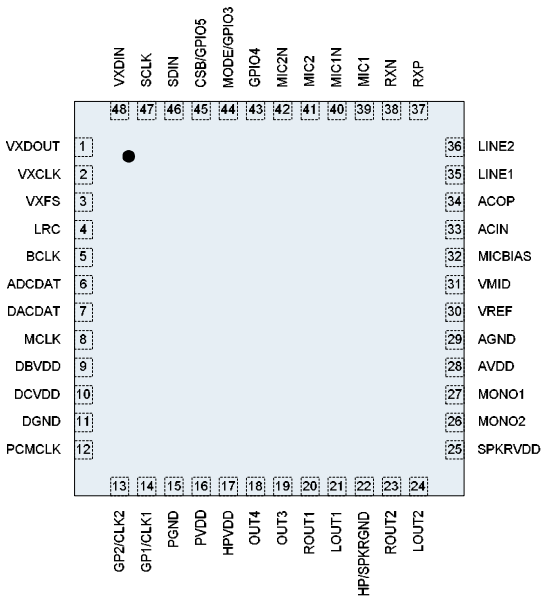


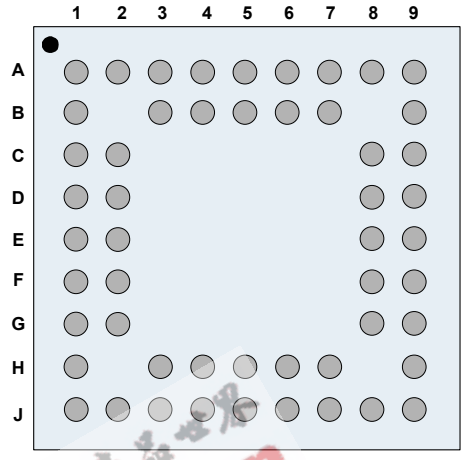
TABLE OF CONTENTS

PIN CONFIGURATION - QFN



(TOP VIEW)

PIN CONFIGURATION - BGA



(TOP VIEW)

ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8753LGEFL/V	-25°C to +85°C	48-lead QFN (7x7x0.9mm) (Pb-free)	MSL3	260°C
WM8753LGEFL/RV	-25°C to +85°C	48-lead QFN (7x7x0.9mm) (Pb-free, tape and reel)	MSL3	260°C
WM8753LGEB/V	-25°C to +85°C	52-ball BGA (5x5x0.9mm) (Pb-free)	MSL3	260°C
WM8753LGEB/RV	-25°C to +85°C	52-ball BGA (5x5x0.9mm) (Pb-free, tape and reel)	MSL3	260°C

Note:

QFN Reel quantity = 2,200

BGA Reel quantity = 3,500

PIN DESCRIPTION

BGA	QFN	NAME	TYPE	DESCRIPTION
J2	1	VXDOUT	Digital Output	Voice ADC Output
H3	2	VXCLK	Digital Input/Output	Voice CODEC data clock / ADC frame clock
J3	3	VXFS	Digital Input/Output	Voice CODEC Frame Sync
H4	4	LRC	Digital Input/Output	DAC Frame Sync
J4	5	BCLK	Digital Input/Output	DAC data clock input / output
J5	6	ADCDAT	Digital Output	ADC Digital Audio Data Alternative Output
H5	7	DACDAT	Digital Input	DAC Digital Audio Data Input
J6	8	MCLK	Digital Input	Master Clock Input
H6	9	DBVDD	Supply	Digital Buffer Supply (supply for digital I/O buffers)
J7	10	DCVDD	Supply	Digital Core Supply (supply for digital logic, except I/O buffers)
H7	11	DGND	Supply	Digital ground (all digital logic)
J8	12	PCMCLK	Digital Input	VOICE CODEC master clock input (may be looped from PLL output)
J9	13	GP2/CLK2	Digital Output	General Purpose Output 2, usually PLL2 output
G8	14	GP1/CLK1	Digital Output	General Purpose Output 1, usually PLL1 output
H9	15	PGND	Supply	PLL ground
G9	16	PVDD	Supply	PLL Supply
F9	17	HPVDD	Supply	Headphone Supply
E9	18	OUT4	Analogue Output	Analogue Output 4 (Headphone driver)
E8	19	OUT3	Analogue Output	Analogue Output 3 (Headphone driver)
D9	20	ROUT1	Analogue Output	Headphone Output Right
D8	21	LOUT1	Analogue Output	Headphone Output Left
C9	22	HP/SPKRGND	Supply	Headphone and Speaker ground
B9	23	ROUT2	Analogue Output	Speaker Output Right
A9	24	LOUT2	Analogue Output	Speaker Output Left
A8	25	SPKRVDD	Supply	Speaker Supply
B7	26	MONO2	Analogue Output	Mono analogue output 2
B6	27	MONO1	Analogue Output	Mono analogue output 1
A6	28	AVDD	Supply	Analogue supply (feeds ADC and DAC)
A5	29	AGND	Supply	Analogue ground (feeds ADC and DAC)
B5	30	VREF	Reference	Buffered ADC and DAC Reference voltage
A4	31	VMID	Reference	Decoupling for ADC and DAC reference voltage
B4	32	MICBIAS	Analogue Output	Microphone Bias
A3	33	ACIN	Analogue Input	AC coupled input to ALC PGA in record path
B3	34	ACOP	Analogue Output	ALC Mix output
A2	35	LINE1	Analogue Input	Left Channel Input
A1	36	LINE2	Analogue Input	Right Channel input
B1	37	RXP	Analogue Input	RX mono differential input positive signal
C2	38	RXN	Analogue Input	RX mono differential input negative signal
C1	39	MIC1	Analogue Input	Mic Pre-amp input 1
D2	40	MIC1N	Analogue Input	Mic Pre-amp 1 common mode or negative input
D1	41	MIC2	Analogue Input	Mic Pre-amp input 2
E2	42	MIC2N	Analogue Input	Mic Pre-amp 2 common mode or negative input
E1	43	GPIO4	Digital input/Output	GPIO (General Purpose input/output) usually headphone jack insert autodetect with selectable pull-up/pull-down.
F1	44	MODE/GPIO3	Digital Input / Output	Control interface Mode select on reset or GPIO3
F2	45	CSB/GPIO5	Digital Input / Output	3-wire MPU Chip Select / 2-wire MPU interface address selection or GPIO5
G1	46	SDIN	Digital Input / Output	3-wire MPU Data Input / 2-wire MPU Date Input / Acknowledge
H1	47	SCLK	Digital Input	3-wire MPU Clock Input / 2-wire MPU Clock Input
J1	48	VXDIN	Digital Input	VOICE DAC Input

Note: 1. It is recommended that the QFN ground paddle is connected to analogue ground on the application PCB

2. Unused BGA pins F8, C8, G2, A7

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages	-0.3V	+4.5V
Voltage range digital inputs	DGND - 0.3V	DVDD + 0.3V
Voltage range analogue inputs	AGND - 0.3V	AVDD + 0.3V
Operating temperature range, T_A	-25°C	+85°C
Storage temperature after soldering	-65°C	+150°C

Notes:

1. Analogue, PLL and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other.
3. DCVDD must be less than or equal to AVDD.

SIMULATED THERMAL PROPERTIES

POWER INPUT (WATTS)	THETA Ja (°C/W)	THETA Jc (°C/W)	Tj (°C)	Tc(°C)
1 Watt	48.8	17.4	73.8	26.5
0.5 Watt	48.9	18.2	49.4	25.7

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD		1.42		3.6	V
Digital supply range (Buffer)	DBVDD		1.8		3.6	V
Analogue supplies range	AVDD		1.8		3.6	V
PLL supplies range	PLLVDD		1.8		3.6	V
Ground	DGND,AGND,PLLGND, HP/SPKRGND			0		V

ELECTRICAL CHARACTERISTICS

Test Conditions
DCVDD = 1.5V, AVDD = HPVDD = DBVDD = SPKRVDD = PLLVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (LINE1, LINE2, RXP, RXN)						
Full-scale Input Signal Level (0dB) – note this changes with AVDD	V_{INFS}			1.0		Vrms
Input Capacitance	$C_{LINE1/2,}$ RXP/N			10		pF
Microphone Preamp Inputs (MIC1, MIC1N, MIC2, MIC2N)						
Full-scale Input Signal Level (0dB) – note this changes with AVDD	V_{INFS}			177 -12		mVrms dBV
Mic preamp gain range			12		30	dB
Mic preamp equivalent input noise	At 30dB gain			TBD		uV
Input resistance	$R_{MIC1N,}$ R_{MIC2N}	Gain set to 30dB		5		kΩ
Input resistance	$R_{MIC1N,}$ R_{MIC2N}	Gain set to 24dB		10		kΩ
Input resistance	$R_{MIC1N,}$ R_{MIC2N}	Gain set to 18dB		18		kΩ
Input resistance	$R_{MIC1N,}$ R_{MIC2N}	Gain set to 12dB		33		kΩ
Input resistance	$R_{MIC1,}$ R_{MIC2}			163		kΩ
Recommended decoupling cap	C_{DECOUP}			0.33		uF
Input Capacitance	C_{MICIN}			10		pF
Programmable Gain Amplifier (PGA)						
Programmable Gain			-17.25		30	dB
Programmable Gain Step Size		Guaranteed Monotonic		0.75		dB
Mute Attenuation				TBD		dB
Automatic Level Control (ALC)						
Target Record Level			-28.5		-6	dB
Gain Hold Time (Note 1)	t_{HOLD}	MCLK = 12.288MHz (Note 3)	0, 2.67, 5.33, 10.67, … , 43691 (time doubles with each step)			ms
Gain Ramp-Up (Decay) Time (Note2)	t_{DCY}		24, 48, 96, … , 2458 (time doubles with each step)			ms
Gain Ramp-Down (Attack) Time (Note 2)	t_{ATK}		6, 12, 24, … , 6140 (time doubles with each step)			ms
LINE1/2 to Analogue to Digital Converter (ADC)						
Signal to Noise Ratio (Note 4, 5)		A-weighted, 0dB gain		95		dB
Total Harmonic Distortion (Note 6)		full-scale, 0dB gain		-82		dB
Channel Separation (Note 7)		1kHz input signal		90		dB
LINE1/2 to Voice Analogue to Digital Converter (ADC), fs = 8kHz						
Signal to Noise Ratio (Note 4, 5)		A-weighted, 0dB gain		82		dB
Total Harmonic Distortion (Note 6)		full-scale, 0dB gain		-74		dB
Channel Separation (Note 7)		1kHz input signal		90		dB
Digital to Analogue Converter (DAC) to Lineout (LOUT1/2, ROUT1/2, MONO1, MONO2,OUT3 with 10kΩ / 50pF load)						
Signal to Noise Ratio (A-weighted)	SNR	A-weighted	TBD	98		dB
Total Harmonic Distortion (Note 6)	THD	R_L = 10 kΩ full-scale signal		-84		dB

Test Conditions

DCVDD = 1.5V, AVDD = HPVDD = DBVDD = SPKRVDD = PLLVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voice Digital to Analogue Converter (DAC) to Lineout (LOUT1/2, ROUT1/2, MONO1, MONO2,OUT3 with 10kΩ / 50pF load), fs = 8kHz						
Signal to Noise Ratio (A-weighted)	SNR	A-weighted	TBD	82		dB
Input Resistance	$R_{LINE1/2}$	LINE1/2 input to output mixer, gain = +6dB	10			kΩ
	R_{RXP}		30			kΩ
	R_{RXN}		20			kΩ
Total Harmonic Distortion (Note 6)	THD	R_L = 10 kΩ full-scale signal		-74		dB
Tone Control						
Bass Boost			-6	0	+9	dB
Bass Boost Step Size				1.5dB		dB
Bass Filter Characteristic				2nd order		
Treble Boost			-6	0	+9	dB
Treble Boost Step Size				1.5dB		dB
Treble Filter Characteristic				2nd order		
Output Mixers (Left, Right and Mono mix)						
PGA gain range into mixer			-15		+6	dB
PGA gain step into mixer				3		dB
Analogue Outputs (L/ROUT1, L/ROUT2, MONO1)						
0dB full scale output voltage				AVDD/3.3		Vrms
Programmable Gain range		1kHz signal	-73		+6	dB
Programmable Gain step size		monotonic		1		dB
Mute Attenuation		1kHz, full scale signal		85		dB
Channel Separation				90		dB
Headphone Output (LOUT1/2, OUT3)						
Total Harmonic Distortion	THD	HPVDD=1.8V, R_L=32Ω Po = 5mW			0.013 -78	% dB
		HPVDD=1.8V, R_L=16Ω Po = 5mW			0.013 - 78	% dB
		HPVDD=3.3V, R_L=32Ω Po = 20mW			0.01 -80	% dB
		HPVDD=3.3V, R_L=16Ω Po = 20mW			0.01 -80	% dB
Signal to Noise Ratio (A-weighted)	SNR	HPVDD = 3.3V		90		dB
		HPVDD = 1.8V		90		dB
Speaker Output (L/ROUT2)						
Total Harmonic Distortion	THD	Po=180mW, RL=8Ω, SPKRVDD=3.3V		-50 0.3		dB %
		Po=400mW, RL=8Ω, SPKRVDD=3.3V		-40 1		dB %
Signal to Noise Ratio (A-weighted)	SNR	SPKRVDD=3.3V, RL=8Ω		90		dB
		SPKRVDD=2.5V, RL=8Ω		90		dB

Test Conditions

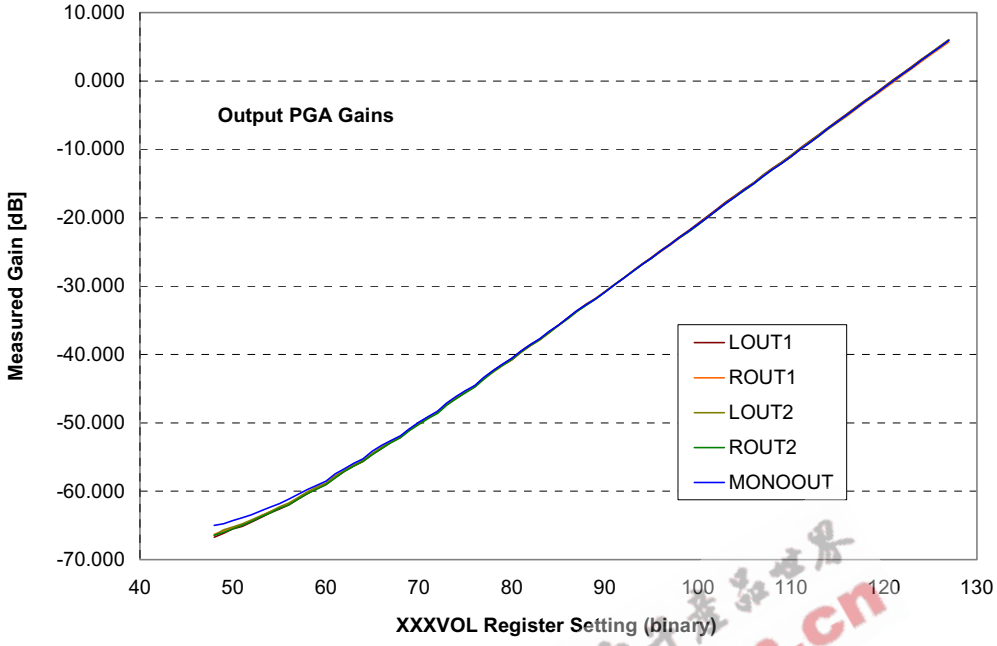
DCVDD = 1.5V, AVDD = HPVDD = DBVDD = SPKRVDD = PLLVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Bias						
Bias Voltage (MBVSEL=0)	$V_{MICBIAS}$		-3%	0.9*AVDD	+3*%	V
Bias Voltage (MBVSEL=1)	$V_{MICBIAS}$		-3%	0.75*AVDD	+3*%	V
Bias Current Source	$I_{MICBIAS}$				3	mA
Output Noise Voltage	Vn	1K to 20kHz		15		nV/√Hz
Digital Input / Output (excluding GPIO4)						
Input HIGH Level	V_{IH}		0.7×DBVDD			V
Input LOW Level	V_{IL}				0.3×DBVDD	V
Output HIGH Level	V_{OH}	I_{OL}=1mA	0.9×DBVDD			V
Output LOW Level	V_{OL}	I_{OH}=-1mA			0.1×DBVDD	V
GPIO4 Input						
Input HIGH Level	V_{IH}		1.4			V
Input LOW Level	V_{IL}				0.8	V
Pullup/pulldown resistance	R_{IN}			100		kΩ

TERMINOLOGY

1. Hold Time is the length of time between a signal detected being too quiet and beginning to ramp up the gain. It does not apply to ramping down the gain when the signal is too loud, which happens without a delay.
2. Ramp-up and Ramp-Down times are defined as the time it takes for the PGA to sweep across 90% of its gain range.
3. All hold, ramp-up and ramp-down times scale proportionally with MCLK
4. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
5. Dynamic range (dB) - DR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
6. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
7. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.

OUTPUT PGA'S LINEARITY



POWER CONSUMPTION

The power consumption of the WM8753L depends on the following factors.

Supply voltages: Reducing the supply voltages also reduces supply currents, and therefore results in significant power savings.

Operating mode: Power consumption is lower in mono modes than in stereo, as one ADC / DAC / PGA is switched OFF. It is also reduced when the device is used for playback only (ADC off) or for recording only (DAC off). Unused outputs should be switched off (for example, when line out is not used, do not enable the LINE outputs).

Headphone volume: At high volume, the power dissipated in the headphone itself is greater than the power consumption of the WM8753L. High headphone volume also increases the power consumption of the on-chip headphone drivers.

	AVDD (V)	IAVDD (mA)	DCVDD (V)	IDCVDD (mA)	DBVDD (V)	IDBVDD (mA)	HPVDD (V)	IHPVDD (mA)	SPKVDD (V)	ISPKVDD (mA)	PLLVDD (V)	IPLLVDD (mA)	Total Power (mW)
Off	3.3	0.018	1.8	0.007	3.3	0	3.3	0	3.3	0	3.3	0	0.07
	3.3	0.018	2.7	0.009	2.7	0	3.3	0	3.3	0	2.7	0	0.08
	1.8	0.007	1.8	0.007	1.8	0	1.8	0	3.3	0	1.8	0	0.03
Off with temp sensor disabled	3.3	0	1.8	0.007	3.3	0	3.3	0	3.3	0	3.3	0	0.01
	3.3	0	2.7	0.009	2.7	0	3.3	0	3.3	0	2.7	0	0.02
	1.8	0	1.8	0.007	1.8	0	1.8	0	3.3	0	1.8	0	0.01
Standby (500k VMID, no clocks, temp sensor off)	3.3	0.004	1.8	0.007	3.3	0	3.3	0	3.3	0	3.3	0	0.03
	3.3	0.004	2.7	0.009	2.7	0	3.3	0	3.3	0	2.7	0	0.04
	1.8	0.002	1.8	0.007	1.8	0	1.8	0	3.3	0	1.8	0	0.02
Stereo 16R HP playback 44.100k, MCLK=13MHz, PLL enabled, quiescent	3.3	4.38	1.8	2.9	3.3	1.54	3.3	0	3.3	0.007	3.3	1	28.08
	3.3	4.38	1.8	2.9	1.8	0.8	3.3	0	3.3	0.007	3.3	1	24.44
	2.7	3.48	1.8	2.87	1.8	0.8	2.7	0.52	3.3	0.006	2.7	0.84	19.69
	1.8	2.22	1.5	2.35	1.8	0.8	1.8	0.31	3.3	0.004	1.8	0.64	10.68
Stereo 16R HP playback 44.100k, MCLK=13MHz, PLL enabled, 100mVrms	3.3	4.34	1.8	2.9	3.3	1.54	3.3	5.3	3.3	0.007	3.3	1	45.44
	3.3	4.33	1.8	2.9	1.8	0.8	3.3	5.44	3.3	0.007	3.3	1	42.22
	2.7	3.48	1.8	2.85	1.8	0.8	2.7	5.28	3.3	0.006	2.7	0.84	32.51
	1.8	2.22	1.5	2.36	1.8	0.8	1.8	5.33	3.3	0.004	1.8	0.64	19.74
Stereo 16R HP playback 44.100k, MCLK=256fs, quiescent	3.3	4.35	1.8	2.43	3.3	0.062	3.3	0.68	3.3	0.007	3.3	0.09	21.50
	3.3	4.33	1.8	2.42	1.8	0.004	3.3	0.68	3.3	0.007	3.3	0.09	21.22
	2.7	3.48	1.8	2.42	1.8	0.004	2.7	0.52	3.3	0.005	2.7	0.071	15.37
	1.8	2.23	1.5	1.97	1.8	0.004	1.8	0.31	3.3	0.004	1.8	0.044	7.63
Stereo 16R HP playback 44.100k, MCLK=256fs, 100mVrms	3.3	4.35	1.8	2.43	3.3	0.062	3.3	5.14	3.3	0.007	3.3	0.09	36.22
	3.3	4.33	1.8	2.42	1.8	0.004	3.3	5.45	3.3	0.007	3.3	0.09	36.96
	2.7	3.46	1.8	2.42	1.8	0.004	2.7	5.46	3.3	0.005	2.7	0.07	28.65
	1.8	2.23	1.5	1.97	1.8	0.004	1.8	5.18	3.3	0.004	1.8	0.044	16.39
Stereo 16R HP playback 44.100k, MCLK=256fs, 565mVrms = 20mW	3.3	4.35	1.8	2.43	3.3	0.062	3.3	29	3.3	0.007	3.3	0.09	114.95
Stereo 16R HP playback 44.100k, MCLK=256fs, 565mVrms = 20mW	3.3	4.34	1.8	2.46	1.8	0.004	3.3	29	3.3	0.007	3.3	0.09	114.78
Stereo 16R HP playback 44.100k, MCLK=256fs, 462mVrms = 13.3mW	2.7	3.48	1.8	2.46	1.8	0.004	2.7	19.5	3.3	0.005	2.7	0.071	66.69
Stereo 16R HP playback 44.100k, MCLK=256fs, 308mVrms = 5.9mW	1.8	2.25	1.5	2.03	1.8	0.004	1.8	8.8	3.3	0.004	1.8	0.044	23.03
PCM voice call (Right ADC, diff rec from mic2, VDAC playback to 16R, 64x OSR, 8kHz, MCLK=256fs)	3.3	5.18	1.8	0.63	3.3	0.094	3.3	5.27	3.3	0.007	3.3	0.016	36.01
	3.3	5.18	1.8	0.63	1.8	0.004	3.3	5.27	3.3	0.007	3.3	0.016	35.70
	2.7	4.4	1.8	0.63	1.8	0.004	2.7	5.26	3.3	0.006	2.7	0.013	27.28
	1.8	3.15	1.5	0.5	1.8	0.004	1.8	5	3.3	0.004	1.8	0.008	15.45

Table 1 Power Consumption Figures

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

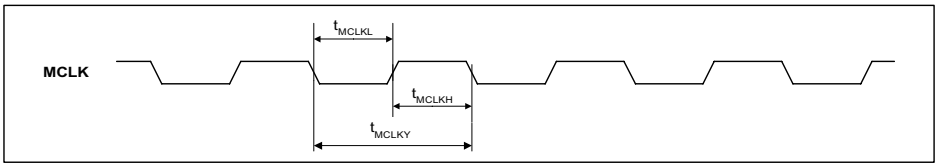


Figure 1 System Clock Timing Requirements

Test Conditions

CLKDIV2=0, DCVDD = 1.42V, DBVDD = AVDD = SPKRVDD = PLLVDD = 3.3V, DGND = AGND = PLLGND = 0V, T_A = +25°C, Slave Mode fs = 48kHz, MCLK = 384fs, 24-bit data, unless otherwise stated.

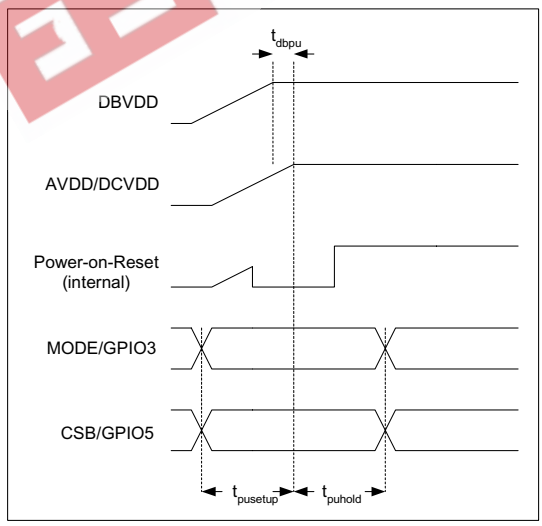
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
MCLK System clock cycle time	T_{MCLKY}	54			ns
MCLK duty cycle	T_{MCLKDS}	60:40		40:60	

Test Conditions

CLKDIV2=1, DCVDD = 1.42V, DBVDD = AVDD = SPKRVDD = PLLVDD = 3.3V, DGND = AGND = PLLGND = 0V, T_A = +25°C, Slave Mode fs = 48kHz, MCLK = 384fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
MCLK System clock pulse width high	T_{MCLKL}	10			ns
MCLK System clock pulse width low	T_{MCLKH}	10			ns
MCLK System clock cycle time	T_{MCLKY}	27			ns

MODE/GPIO3 AND CSB/GPIO5 LATCH ON POWERUP TIMING



Test Conditions

DCVDD = 1.42V, DBVDD = AVDD = SPKRVDD = PLLVDD = 3.3V, DGND = AGND = PLLGND = 0V, T_A = +25°C, Slave Mode fs = 48kHz, MCLK = 384fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
MODE/GPIO3 and CSB/GPIO5 to AVDD and DCVDD power-up setup time	$t_{pusetup}$	100			us
AVDD and DCVDD to MODE/GPIO3 and CSB/GPIO5 hold time	t_{puhold}	1			ms
DBVDD powerup to DCVDD or AVDD powerup	t_{dbpu}	0			us

Note:

1. DBVDD must be supplied before or at same time as either DCVDD or AVDD to ensure MODE and CSB are defined internally when power on reset is released

AUDIO INTERFACE TIMING – MASTER MODE

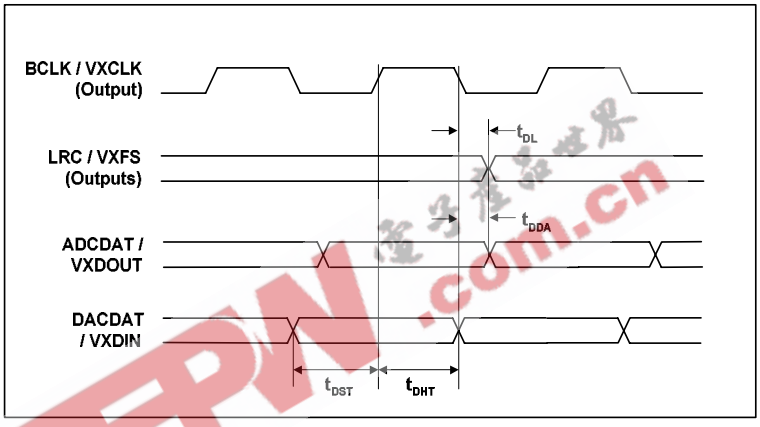


Figure 2 Digital Audio Data Timing – Master Mode (see Control Interface)

Test Conditions

DCVDD = 1.42V, DBVDD = AVDD = HPVDD = SPKRVDD = PLLVDD = 3.3V, DGND = AGND = PLLGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
LRC / VXFS propagation delay from BCLK / VXCLK falling edge	t_{DL}			10	ns
ADCDAT / VXDOUT propagation delay from BCLK / VXCLK falling edge	t_{DDA}			10	ns
DACDAT / VXDIN setup time to BCLK / VXCLK rising edge	t_{DST}	10			ns
DACDAT / VXDIN hold time from BCLK / VXCLK rising edge	t_{DHT}	10			ns

AUDIO INTERFACE TIMING – SLAVE MODE

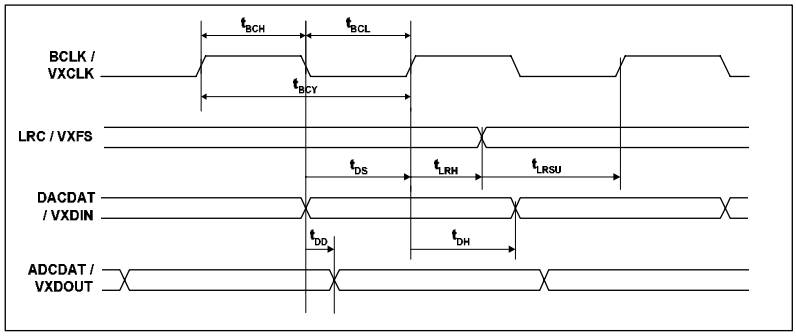


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

DCVDD = 1.42V, DBVDD = AVDD = HPVDD = SPKRVDD = PLLVDD = 3.3V, DGND = AGND = PLLGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK / VXCLK cycle time	t_{BCY}	50			ns
BCLK / VXCLK pulse width high	t_{BCH}	20			ns
BCLK / VXCLK pulse width low	t_{BCL}	20			ns
LRC / VXFS set-up time to BCLK / VXCLK rising edge	t_{LRSU}	10			ns
LRC / VXFS hold time from BCLK / VXCLK rising edge	t_{LRH}	10			ns
DACDAT / VXDIN hold time from BCLK / VXCLK rising edge	t_{DH}	10			ns
ADCDAT / VXDOUT propagation delay from BCLK / VXCLK falling edge	t_{DD}			10	ns

Note:

1. BCLK / VXCLK period should always be greater than or equal to MCLK / VXCLK period.

CONTROL INTERFACE TIMING – 3-WIRE MODE

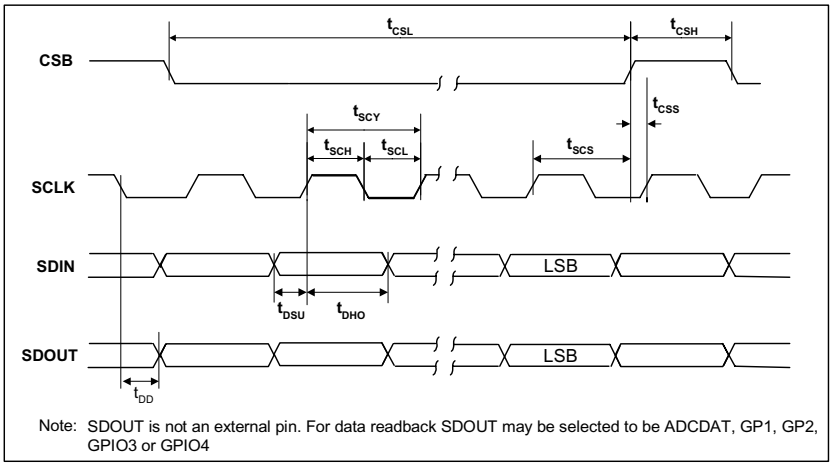


Figure 4 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

DCVDD = 1.42V, DBVDD = AVDD = HPVDD = SPKRVDD = PLLVDD = 3.3V, DGND = AGND = PLLGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	t_{SCS}	80			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SCLK to SDIN hold time	t_{DHO}	40			ns
CSB pulse width low	t_{CSL}	40			ns
CSB pulse width high	t_{CSH}	40			ns
CSB rising to SCLK rising	t_{CSS}	40			ns
SCLK falling to SDOUT propagation delay	t_{DD}			10	ns
Pulse width of spikes that will be suppressed	t_{ps}	5			ns

CONTROL INTERFACE TIMING – 2-WIRE MODE

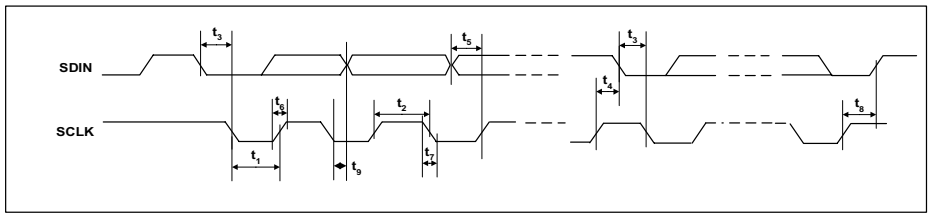


Figure 5 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD = 1.42V, DBVDD = AVDD = HPVDD = SPKRVDD = PLLVDD = 3.3V, DGND = AGND = PLLGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency		0		526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

INTERNAL POWER ON RESET CIRCUIT

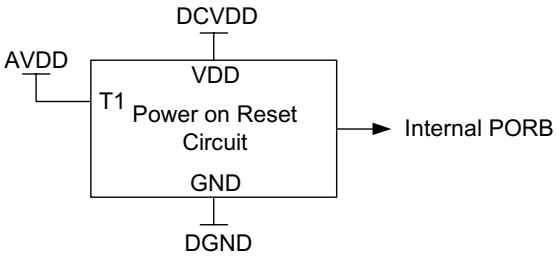


Figure 6 Internal Power on Reset Circuit Schematic

The WM8750 includes an internal Power-On-Reset Circuit, as shown in Figure 6, which is used to reset the digital logic into a default state after power up. The power on reset circuit is powered from DCVDD and monitors DCVDD and AVDD. It asserts PORB low if DCVDD or AVDD are below a minimum threshold.

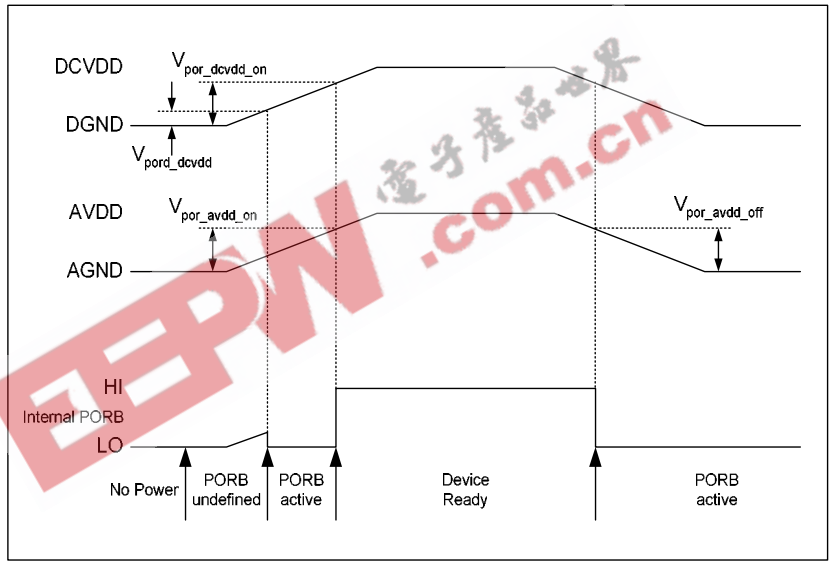


Figure 7 Typical Power-Up Sequence

Figure 7 shows a typical power-up sequence. When DCVDD and AVDD rise above the minimum thresholds, Vpord_dcvdd and Vpord_avdd, there is enough voltage for the circuit to guarantee the Power on Reset is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When DCVDD rises to Vpor_dcvdd_on and AVDD rises to Vpor_avdd_on, PORB is released high and all registers are in their default state and writes to the control interface may take place. If DCVDD and AVDD rise at different rates then PORB will only be released when DCVDD and AVDD have both exceeded the Vpor_dcvdd_on and Vpor_avdd_on thresholds.

On power down, PORB is asserted low whenever DCVDD drops below the minimum threshold Vpor_dcvdd_off or AVDD drops below the minimum threshold Vpor_avdd_off.

SYMBOL	MIN	TYP	MAX	UNIT
V_{pord_dcvdd}	0.4	0.6	0.8	V
$V_{por\_dcvdd\_on}$	0.9	1.26	1.6	V
$V_{por\_avdd\_on}$	0.5	0.7	0.9	V
$V_{por\_avdd\_off}$	0.4	0.6	0.8	V

Table 2 Typical POR Operation (typical values, not tested)

DEVICE DESCRIPTION

INTRODUCTION

The WM8753L is a low power audio CODEC combining a high quality stereo audio DAC with a high quality stereo ADC and mono DAC. The stereo ADC may be configured for operation as a mono or stereo voice ADC to operate with the mono DAC as a voice CODEC. Alternatively the ADC may be configured as a hi-fi ADC for high quality record function. In voice mode the ADC filters are optimised for voice record function. Applications for such a combined device include MP3 playing 'smart-phones' and Bluetooth connected high quality stereo headsets. The mono voice CODEC might be used either for the usual voice CODEC function, or perhaps as an additional CODEC for support of Bluetooth links from such MP3 phones. Alternatively, if not required for such functions, the ADC of the CODEC may be reconfigured so it is clocked off the I^2S audio data interface domain, and its output sent over the Hi-Fi audio interface as well as the voice audio interface, so it might be used as a recording ADC in an I^2S based audio system.

FEATURES

The chip offers great flexibility in use, and so can support many different modes of operation as follows:

LINE INPUTS

The device includes two pairs of stereo analogue inputs that can be switched internally. LINE1 and LINE2 can be used as either a pair of mono line level inputs, or as a single stereo pair. They may also be used as differential input or be mixed together. A further two inputs, RXP and RXN, can be used as a single differential input or mixed together. The output from these inputs can be played back in stereo form to the headphones, or mono form to the transmit mono output. The mono output supports both single ended and differential output, using a pair of output pins. If not required, the differential output buffer may be powered down.

MICROPHONE INPUTS

Two microphone preamplifiers are provided, allowing for a pair of external microphones to be differentially connected, with user defined gain using internal resistors, offering gain range from +12dB to +30dB. Alternatively, three microphones can be connected to one microphone preamplifier, with the second preamplifier disabled, and the microphone required is then selected. A microphone bias is output from the chip which can be used to bias all microphones. The signal routing can be configured to allow manual adjustment of mic levels, or indeed to allow the ALC loop to control the level of mic signal that is transmitted.

PGA AND ALC OPERATION

A programmable gain amplifier is provided in the input path to the ADC. This may be used manually or in conjunction with a mixed analog/digital automatic level control (ALC) which keeps the recording volume constant.

HI-FI DAC

The hi-fi DAC provides high quality audio playback suitable for all portable audio hi-fi type applications, including MP3 players and portable disc players of all types.

VOICE CODEC

The on-chip stereo ADC and mono DAC are of a high quality using a multi-bit high-order oversampling architecture to deliver optimum performance with low power consumption. Various sample rates are supported, from the 8ks/s rate typically used in voice CODECs, up to the 48ks/s rate used in high quality audio applications. The ADC digital filters may be switched for voice mode to filters with steeper roll-off.

OUTPUT MIXERS

Flexible mixing is provided on the outputs of the device; a stereo mixer is provided for the stereo headphone or line outputs, and an additional mono mixer for the mono output to the transmit side of the equipment. Gain adjustment capability, and signal switching is provided to allow for all possible signal combinations; eg. Sidetone, transmission of stereo music playback along with voice, whilst at the same time as listening to music, and received phone call if so desired. The output buffers can be configured in several ways, allowing support of up to three sets of external transducers; ie stereo headphone, BTL speaker, and BTL earpiece may be connected simultaneously. (thermal implications should be considered before simultaneous full power operation of all outputs is attempted!)

Alternatively, if a speaker output is not required, the LOUT2 and ROUT2 pins might be used as a stereo speaker or headphone driver, (disable output invert buffer on ROUT2). In that case either two sets of headphones might be driven, or the LOUT2 and ROUT2 pins used as a line output driver.

The Earpiece may be driven in BTL mode, with the ROUT1 signal inverted into the OUT3 pin, or alternatively OUT3 may be either the mono version of ROUT1 and LOUT1, or simply a buffered version of the chip midrail reference voltage. This voltage may then be used as a headphone 'pseudo ground' allowing removal of the large AC coupling capacitors often used in the output path.

AUDIO INTERFACES

The WM8753L has a pair of audio interfaces, to support the Hi-Fi DAC and the PCM CODEC.
The Hi-Fi DAC is supported with a 4 wire standard audio DAC interface which supports a number of audio data formats including I^2S, DSP Mode (a burst mode in which frame sync plus 2 data packed words are transmitted), MSB-First, left justified and MSB-First, right justified, and can operate in master or slave modes.

The PCM CODEC is connected via standard PCM type interface, comprising a frame sync, FS, a bitclk VXCLK, (typically 16 clocks per frame), and a pair of data lines for DAC input and ADC output data. A master clock for the PCM CODEC (typically 256fs or 2.048MHz when running at 8ks/s) may also be supplied as an input, if the system controller can provide this, to PCMCLK input pin. In the event of the system controller not being able to provide this clock, it may be generated in the WM8753L using PLL2. Note that the MCLK input to the chip must be present for PLL2 to operate, as it is a digital PLL type of circuit and uses this high speed master clock.

In the event of the PCM CODEC not being required, (temporarily or otherwise) the ADC output data may be sent over the hi-fi audio interface using the ADCDAT line. In this case the ADC may be configured to run at the same sample rate as the hi-fi DAC and use the same clock signals (BCLK and LRC). It may also be configured to run at a different sample rate and instead use the FS and VXCLK as the ADC data frame sync and clock. Both interfaces may be configured to run in Master mode when LRC, BCLK, FS and VXCLK are outputs from the WM8753L. A mixed Master-Slave mode is also supported allowing BCLK / VXCLK to be outputs from the WM8753L and LRC / FS to be inputs.

CONTROL INTERFACES

To allow full software control over all its features, the WM8753L offers a choice of 2 or 3 wire MPU control interface. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs.

Selection between the modes is via the MODE/GPIO3 pin. In 2 wire mode only slave operation is supported and the address of the device may be selected between two values using the CSB/GPIO5 pin. The interface mode and 2-wire address select are set on power-up by the sampling of the MODE/GPIO3 and CSB/GPIO5 pins by the power-on reset. This allows these pins to be used as GPIO pins after powerup.

CLOCKING SCHEMES

WM8753L offers the normal audio DAC clocking scheme operation, where 256 or 384fs or higher MCLK is provided to the DAC. Similarly the PCM CODEC can be operated in normal PCM type mode where a 256fs clock is sent along with the PCM frame clock and data.

However, a pair of PLLs are also included which may be used to generate these clocks in the event that they are not available from the system controller. The first PLL1 uses an input clock, typically the Rf reference clock used in most mobile systems, to generate high quality audio clocks. The second PLL2 can use this same reference clock. If these PLLs are not required for generation of these clocks, they can be reconfigured to generate alternative clocks which may then be output and used elsewhere in the system. The WM8753L can also generate standard audio clock rates from a 12 or 24MHz USB clock without the use of the PLLs.

POWER CONTROL

The design of the WM8753L has given much attention to power consumption without compromising performance. It operates at very low voltages, and includes the ability to power off any unused parts of the circuitry under software control, and includes standby and power off modes.

OPERATION SCENARIOS

Flexibility in the design of the WM8753L allows for a wide range of operational scenarios, some of which are proposed below:

Telephony with MP3 playback: The voice CODEC may be used as standard voice CODEC, and the stereo DAC used for MP3 type playback. The user may choose to transmit the mono version of the MP3 playback to the Tx side of the phone conversation as required. Recording of the phone conversation would then require to be supported in the digital domain, after the voice CODEC. (digital Tx and Rx sides of the conversation would need to be digitally summed as required).

Telephony with recording: In many smart-phone applications the voice CODEC for voice conversion will be included in the cellphone base-band chipset. In such cases the analog (often differential) mic input and speaker outputs from this voice CODEC will be routed to the WM8753L line or mic inputs, and mono outputs. The WM8753L will then provide the buffers to connect to the system transducers (speakers, mics, headphones etc.) and also the stereo hi-fi DAC and mixers to allow MP3 type playback. The ADC may then be used for recording the phone conversation, both Tx and Rx parts, and the extra DAC might be used for generation of confirmation tones or ringtones as required.

Bluetooth Hi-Fi stereo headset; In Bluetooth headsets a mono PCM CODEC is required for the standard telephony quality voice channel. But for the support of compressed hi-fi quality stereo, a hi-fi quality stereo DAC is required. In this case WM8753L can supply both these needs. The BTL speaker driver could be recommitted as either stereo headphone driver, or stereo speaker driver, and perhaps the other headphone output re-used as stereo line output.

Analog FM tuner support: An analog stereo FM tuner might be connected to the Line inputs of WM8753, and the stereo signal listened to via headphones, or transmitted over the 'phone.

INPUT SIGNAL PATH

The WM8753L has a combination of analogue inputs, microphone preamps, mixers and switches allowing flexibility in the configuration of the input to left and right ADCs and to analogue bypass paths into the Left, Right and Mono output Mixers. The input to the ADC may be routed through a PGA whose gain is controlled either by the user or by the on-chip ALC function (see Automatic Level Control). The ADCs may be powered off independently and a single ADC may be used for left and right ADC input mono mixing.

SIGNAL INPUTS

The WM8753L has three sets of high impedance, low capacitance AC coupled differential inputs as well as two high impedance, low capacitance AC coupled mono line inputs. Two of the differential inputs (MIC1N/MIC1N and MIC2N/MIC2N) have a microphone pre-amp and selectable gain of +12dB to +30dB in 6dB steps. RXN and RXP are a differential line input and can also be configured as a stereo to mono mix input. In addition there are two mono LINE inputs (LINE1 and LINE2) which can be used as a single stereo input.

The LINE1 and LINE2 inputs may be configured as a differential input or a stereo to mono mix using the Line input mixer under the control of register bits LMSEL. The LMSEL bits also allow either one of the inputs to be enabled and the other disabled. The Line mixer output may then be routed to the ALC mixer by setting LINEALC and/or to the output Mono mixer via the bypass path. The Line mixer has -6dB of gain so that a 0dB signal on LINE1 and LINE2 will sum to give a 0dB signal at the mixer output.

There is an analogue input to analogue output bypass path into the Left, Right and Mono output mixers. The Left bypass path may be selected to be either the output of the RX mixer or the LINE1 input under the control of LM. The Right bypass path may be selected to be either the output of the RX mixer or the LINE2 input under the control of RM. The Mono bypass path may be selected to be either the output of the Line mixer or the RX mixer under the control of MM.

RXN and RXP are inputs to a mixer controlled by the RXMSEL register bits. By default this is a differential input (RXP-RXN). The RX mixer can also be configured as a stereo to mono mix input (RXP+RXN). Alternatively RXP or RXN can be individually selected as mono inputs with the other input disabled. The RX mixer has -6dB of gain so that a 0dB signal on RXP and RXN will sum to give a 0dB signal at the mixer output.

In addition there is a Sidetone path from the Mic Mux to the left, right and mono mixers. This Sidetone path may be selected to be the output from the left or right ADC input PGA, the Mic1 preamp or the Mic2 preamp under the control of MICMUX[1:0].

The Left ADC input is selected using LADCSEL[1:0]. It can be selected to be i) a direct analogue input from LINE1 or the output of the RX mixer block; ii) through the input PGA and ALC mixer; iii) DC measurement input from LINE1. For direct analogue input the input may be selected from either LINE1 or the RX mixer using LM. The ALC mixer may be used to mix MIC1, MIC2, LINE and RX differential inputs, selected using MIC1ALC, MIC2ALC, LINEALC and RXALC.

The Right ADC input is selected using RADCSEL[1:0]. It can be selected to be i) a direct analogue input from LINE2 or the RX mixer input; ii) through the input PGA from the MIC2 preamp; iii) Record mixer output. For direct analogue input the input may be selected from either LINE2 or the RX mixer using RM. The Record mixer may be used to mix the output from the left, right and mono output mixers, e.g. for recording a phone call. The inputs to the Record mixer are selected using LSEL, RSEL and MSEL and have independent input gain control from -15dB to +6dB.

The input to the Left ADC PGA via the external dc blocking capacitor is from the output of the ALC mixer, which allows the mixing of the output from the Line mixer, the RX mixer, the Mic1 preamp and the Mic2 preamp under the control of LINEALC, RXALC, MIC1ALC and MIC2ALC.

The signal inputs are biased internally to the reference voltage VREF. Whenever the analogue inputs are muted or the device placed into standby mode, the inputs are kept biased to VREF using special anti-thump circuitry. This reduces any audible clicks that may otherwise be heard when changing inputs.

DC MEASUREMENT

For DC measurements (for example, battery voltage monitoring), the input signal at the LINE1 input can be taken directly into the left ADC, bypassing the PGA. The ADC output then becomes unsigned relative to AVDD, instead of being a signed (two's complement) number relative to VREF. The input range for dc measurement is AGND to AVDD. The ADC high pass filter should be disabled when measuring DC voltages.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R46 (2Eh) ADC input Mode	[3:2]	RADCSEL[1:0]	00	Right ADC Input Select 00 : PGA 01 : LINE2 or RXP-RXN 10 : Left + Right + Mono output Mix 11 : unused
	[1:0]	LADCSEL[1:0]	00	Left ADC Input Select 00 : PGA 01 : LINE1 or RXP-RXN 10 : LINE1 DC measurement 11 : unused

Table 3 ADC Input Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R47 (2Fh) Input Control (1)	[4:3]	LMSEL[1:0]	00	Line Mix Select: 00: LINE1 + LINE2 01: LINE1 – LINE2 10: LINE1 (LINE2 disconnected) 11: LINE2 (LINE1 disconnected)
	2	MM	0	Mono Mux Select 0 : Line Mix Output 1: Rx Mix output (RXP +/– RXN)
	1	RM	0	Right Mux Select 0 : LINE2 1 : Rx Mix output (RXP +/– RXN)
	0	LM	0	Left Mux Select 0 : LINE1 1 : Rx Mix output (RXP +/– RXN)

Table 4 Input and Bypass Mux Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R48 (30h) Input Control (2)	[7:6]	RXMSEL[1:0]	00	Differential input, Rx, mixer 00: RXP – RXN 01: RXP + RXN 10: RXP (RXN disconnected) 11: RXN (RXP disconnected)
	[5:4]	MICMUX[1:0]	00	Mic Mux Sidetone Select 00 : Sidetone = Left PGA output 01 : Sidetone = Mic 1 preamp output 10 : Sidetone = Mic 2 preamp output 11 : Sidetone = Right PGA output
	3	LINEALC	0	ALC Mix input select Line Mix 0 : Line Mix not selected into ALC Mix 1 : Line Mix selected into ALC Mix
	2	MIC2ALC	0	ALC Mix input select MIC2 0 : MIC2 not selected into ALC Mix 1 : MIC2 selected into ALC Mix
	1	MIC1ALC	0	ALC Mix input select MIC1 0 : MIC1 not selected into ALC Mix 1 : MIC1 selected into ALC Mix
	0	RXALC	0	ALC Mix input select RX 0 : RX not selected into ALC Mix 1 : RX selected into ALC Mix

Table 5 ALC Mix and Mic Mux Input Select

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) Record Mix (1)	7	RSEL	0	Record Mixer Select Right Mix 0 : Right Mix not selected into Record mixer 1 : Right mix selected into Record mixer
	6:4	RRECVOL [2:0]	101 (-9dB)	Right mixer signal to Record mixer Volume 000 = +6dB … (3dB steps) 111 = -15dB
	3	LSEL	0	Record Mixer Select Left Mix 0 : Left Mix not selected into Record mixer 1 : Left mix selected into Record mixer
	2:0	LRECVOL[2:0]	101 (-9dB)	Left mixer signal to Record mixer Volume 000 = +6dB … (3dB steps) 111 = -15dB
R33 (21h) Record Mix (2)	3	MSEL	0	Record Mixer Select Mono Mix 0 : Mono Mix not selected into Record mixer 1 : Mono mix selected into Record mixer
	2:0	MRECVOL [2:0]	101 (-9dB)	Mono mixer signal to Record mixer Volume 000 = +6dB … (3dB steps) 111 = -15dB

Table 6 Record Mixer Input Select and Gain Control

MONO MIXING

The stereo ADC can operate as a stereo or mono device, or the two channels can be mixed to mono, either in the analogue domain (in the front end of the ADC) or in the digital domain (after the ADC). MONOMIX selects the mode of operation. For analogue mono mix either the left or right channel ADC can be used, allowing the unused ADC to be powered off or used for a dc measurement conversion. The user also has the flexibility to select the data output from the audio interface using DATSEL. The default is for left and right channel ADC data to be output, but the interface may also be configured so that e.g. left channel ADC data is output as both left and right data for when an analogue mono mix is selected.

Note:

If DC measurement is selected this overrides the MONOMIX selection.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R46 (2Eh) ADC input Mode	5:4	MONOMIX[1:0]	00	00: Stereo 01: Analogue Mono Mix (using left ADC) 10: Analogue Mono Mix (using right ADC) 11: Digital Mono Mix

Table 7 Mono Mixing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) Additional Control (1)	8:7	DATSEL [1:0]	00	00: left data = left ADC; right data = right ADC 01: left data = left ADC; right data = left ADC 10: left data = right ADC; right data = right ADC 11: left data = right ADC; right data = left ADC

Table 8 ADC Data Output Configuration

MICROPHONE INPUTS

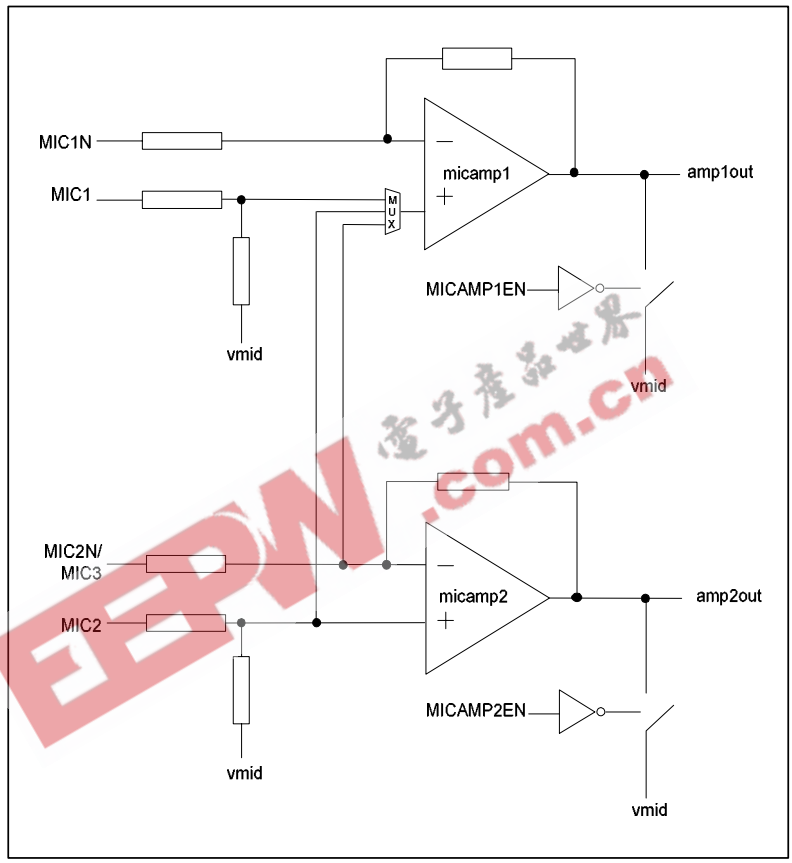


Figure 8 Internal Microphone Input Circuit

There are two microphone pre-amplifiers which can be configured in a variety of ways to accommodate up to 3 single ended or 2 differential microphone inputs. The microphone input circuit is shown in Figure 8.

Each microphone preamplifier has a separate enable bit, MICAMP1EN and MICAMP2EN. The gain for each preamp can be set independently using MIC1BOOST and MIC2BOOST.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 (15h)	8	MICAMP1EN	0	Microphone amplifier 1 enable 0 = Mic1 amp disabled 1 = Mic1 amp enabled
	7	MICAMP2EN	0	Microphone amplifier 2 enable 0 = Mic2 amp disabled 1 = Mic2 amp enabled

Table 9 Mic Preamp Enables

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R47 (2Fh) Mic Input Boost	[8:7]	MIC2BOOST[1:0]	00	MIC2 Preamp Gain Control 00 : +12dB 01 : +18dB 10 : +24dB 11 : +30dB
	[6:5]	MIC1BOOST[1:0]	00	MIC1 Preamp Gain Control 00 = +12dB 01 = +18dB 10 = +24dB 11 = +30dB

Table 10 MIC Preamp Gain Control

The suggested configuration for the external microphone circuit is shown in Figure 9.

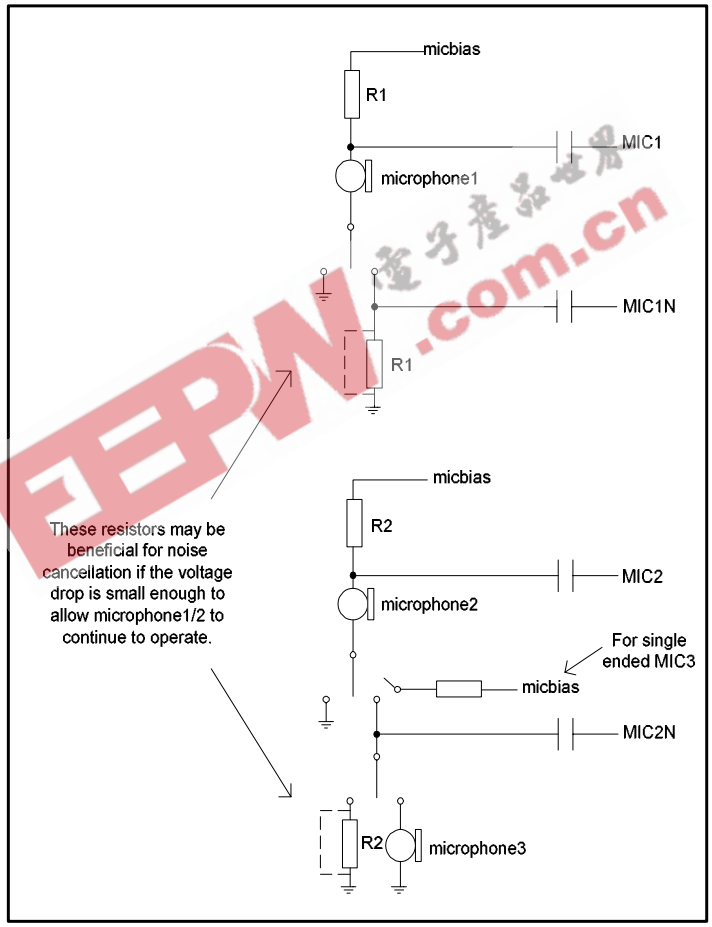


Figure 9 Suggested External Microphone Input Configuration

DIFFERENTIAL OPERATION

It is possible to connect up to two mics differentially. Microphone1 is connected between the MIC1 and MIC1N inputs and microphone2 is connected between the MIC2 and MIC2N inputs. It should be noted that in differential mode, with mic inputs routed to the ADCs, an extra invert occurs in the MIC1 (left ADC) path due to the extra mixer. This can be compensated for by inverting the left ADC signal back again using ADCPOL.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) ADC control	[6:5]	ADCPOL[1:0]	00	00 = Polarity not inverted 01 = L polarity invert 10 = R polarity invert 11 = L and R polarity invert

Table 11 ADC Polarity Control

SINGLE ENDED OPERATION

It is possible to connect up to three microphones single endedly. Microphone1 is connected to the MIC1 input , microphone2 to the MIC2 input, microphone3 to the MIC2N input and MIC1N is connected to Vref. The gains, MIC1BOOST and MIC2BOOST, should be set to be identical and micamp2 must be disabled. Any of the three microphones can then be selected as the output from micamp1 using MICSEL.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R51 (33h) Mic Select	[7:6]	MICSEL[1:0]	00	Microphone selected 00 : MIC1 01 : MIC2 10 : MIC3 11 : unused

Table 12 MIC Select Control

MICROPHONE BIASING CIRCUIT

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. Refer to the Applications Information section for recommended external components. The MICBIAS voltage can be altered via the MBVSEL register bit. When MBVSEL=0, MICBIAS=0.9*AVDD and when MBVSEL=1, MICBIAS=0.75*AVDD. The output can be enabled or disabled using the MICB control bit (see also the "Power Management" section).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R20 (14h) Power Management (1)	5	MICB	0	Microphone Bias Enable 0 = OFF (high impedance output) 1 = ON

Table 13 Microphone Bias Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R51 (33h) Mic bias comp control	8	MBVSEL	0	Microphone Bias Voltage Control 0 = 0.9 * AVDD 1 = 0.75 * AVDD

Table 14 Microphone Bias Voltage Control

The internal MICBIAS circuitry is shown in Figure 10. Note that the maximum source current capability for MICBIAS is 3mA. The external biasing resistors therefore must be large enough to limit the MICBIAS current to 3mA.

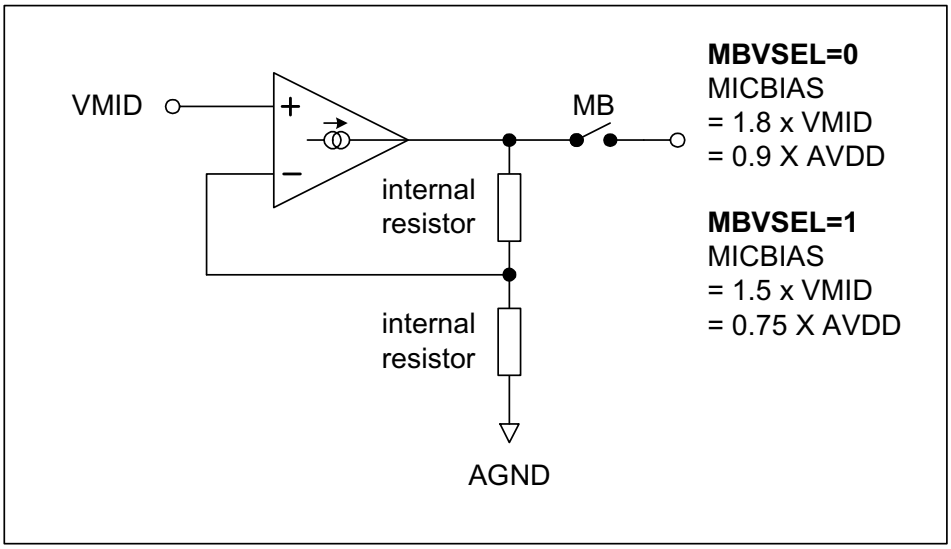


Figure 10 Microphone Bias Schematic

MICBIAS CURRENT DETECT

The WM8753L includes a microphone bias current detect circuit which allows the user to set thresholds for the microphone bias current, above which an interrupt will be triggered. There are two separate interrupt bits, MICDET to allow the user to e.g. distinguish between one or two microphones connected to the WM8753L, and MICSHT to detect a shorted microphone (mic button press). The thresholds for the microphone bias current are set by MBTHRESH[2:0], for MICDET, and MBSCTHRESH[1:0] for MICSHT. Thresholds for each code are shown in Table 15. The circuit is enabled by setting MBCEN.

See the GPIO and Interrupt Controller sections for details on the interrupt and status readback for the microphone bias current detect.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R51 (33h)	5:4	MBSCTHRESH	00	Microphone Bias, Shorted Current Threshold Select 00: 500uA 01: 1000uA 10: 1600uA 11: 2300uA These values are for 3.3V supply and scale with supply voltage.
	3:1	MBTHRESH	000	Microphone Bias, Current Threshold Select 000:250uA 001:410uA ….160uA steps up to 111:1370uA These values are for 3.3V supply and scale with supply voltage.
	0	MBCEN	0	Mic Bias Current Comparator Circuit enable 0 : Comparator disabled 1 : Comparator enabled

Table 15 Mic Bias Current Comparator Circuit Control

PGA CONTROL

The PGA matches the input signal level to the ADC input range. The PGA gain is logarithmically adjustable from –17.25dB to +30dB in 0.75dB steps. Each PGA can be controlled either by the user or by the ALC function (see Automatic Level Control). When ALC is enabled for one or both channels, then writing to the corresponding PGA control register has no effect.

The gain is independently adjustable on both Right and Left Line Inputs. However, by setting the LRINBOTH or RLINBOTH bits whilst programming the PGA gain, both channels are simultaneously updated. This reduces the required number of software writes required. Setting the LZCEN and RZCEN bits enables a zero-cross detector which ensures that PGA gain changes only occur when the signal is at zero, eliminating any zipper noise. If zero cross is enabled a timeout is also available to update the gain if a zero cross does not occur. This function may be enabled by setting TOEN in register R18 (12h).

The inputs can also be muted in the analogue domain under software control. The software control registers are shown in Table 16

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R49 (31h) Left Channel PGA	8	LIVU	0	Left Volume Update 0 = Store LINVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LINVOL, right = intermediate latch)
	7	LINMUTE	1	Left Channel Input Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: LIVU must be set to un-mute.
	6	LZCEN	0	Left Channel Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	5:0	LINVOL [5:0]	010111 (0dB)	Left Channel Input Volume Control 111111 = +30dB 111110 = +29.25dB . . 0.75dB steps down to 000000 = -17.25dB
R50 (32h) Right Channel PGA	8	RIVU	0	Right Volume Update 0 = Store RINVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (right = RINVOL, left = intermediate latch)
	7	RINMUTE	1	Right Channel Input Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: RIVU must be set to un-mute.
	6	RZCEN	0	Right Channel Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	5:0	RINVOL [5:0]	010111 (0dB)	Right Channel Input Volume Control 111111 = +30dB 111110 = +29.25dB . . 0.75dB steps down to 000000 = -17.25dB
R18 (12h) Additional Control	0	TOEN	0	Timeout Enable 0 : Timeout Disabled 1 : Timeout Enabled

Table 16 Input PGA Software Control

ANALOGUE TO DIGITAL CONVERTER (ADC)

The WM8753L uses a multi-bit, oversampled sigma-delta ADC for each channel. The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise. The ADC Full Scale input level is proportional to AVDD. With a 3.3V supply voltage, the full scale level is 1.0 Volts r.m.s. Any voltage greater than full scale may overload the ADC and cause distortion.

ADC DIGITAL FILTER

The ADC filters perform true 24 bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface. The digital filter path is illustrated in Figure 11.

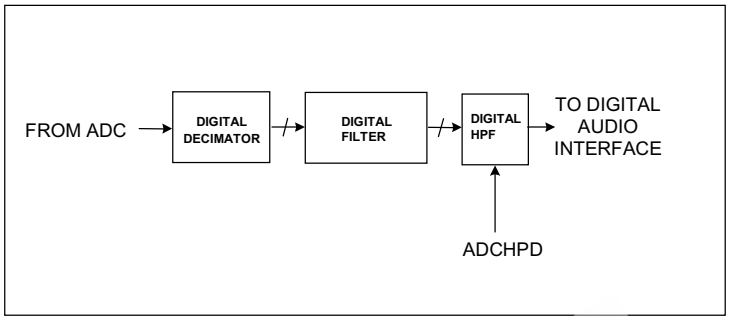


Figure 11 ADC Digital Filter

The characteristic of the digital decimation filter is selectable using control bit VXFILT for HiFi and voice modes of operation. In Voice mode the filter has a steeper roll-off and reduced stopband attenuation. The ADC digital filters also contain a digital high pass filter, selectable via software control. The cut-off frequency of the highpass filter is selectable to suit the mode of operation. For HiFi record mode the default cut-off of 3.4Hz (at fs=48kHz) is recommended and for voice record a cut-off of 100Hz or 200Hz (at fs=8kHz) may be selected The frequency response of the highpass filter will scale with sample rate so the 100Hz cut-off at 8KHz sample rate will scale to a 200Hz cut-off at 16kHz sample rate. The decimation and high-pass filter responses are detailed in the Digital Filter Characteristics section. When the high-pass filter is enabled the dc offset is continuously calculated and subtracted from the input signal. By setting HPOR, the last calculated dc offset value is stored and will continue to be subtracted from the input signal. If the DC offset is changed, the stored and subtracted value will not change unless HPOR is reset. This feature can be used for calibration purposes.

HPMODE	Cut-off (Hz)		
	fs=8kHz	fs=16kHz	fs=48kHz
00	0.6	1.1	3.7
01	41	82	246
10	82	164	492
11	170	340	1020

Table 17 Highpass Filter Cut-off Frequencies

The output data format can be programmed by the user to accommodate stereo or monophonic recording on both inputs. The polarity of the output signal can also be changed under software control. The software control is shown in Table 18.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) ADC Control	6:5	ADCPOL [1:0]	00	00 = Polarity not inverted 01 = L polarity invert 10 = R polarity invert 11 = L and R polarity invert
	4	VXFILT	0	ADC Filter Select 0 = HiFi Filter 1 = Voice FIlter
	3:2	HPMODE	00	ADC High pass Filter Cut-off Select 00 = 3.4Hz @ fs = 48kHz 01 = 82Hz @ fs = 16kHz (41Hz @ fs = 8kHz) 10 = 82Hz @ fs = 8kHz (164Hz @ fs = 16kHz) 11 = 170Hz @ fs = 8kHz (340Hz @ fs = 16kHz)
	1	HPOR	0	Store dc offset 1 = store offset 0 = clear offset
	0	ADCHPD	0	ADC High Pass Filter Enable (Digital) 1 = Disable High Pass Filter 0 = Enable High Pass Filter

Table 18 ADC Signal Path Control

DIGITAL ADC VOLUME CONTROL

The output of the ADCs can be digitally amplified or attenuated over a range from –97dB to +30dB in 0.5dB steps. The volume of each channel can be controlled separately. The gain for a given eight-bit code X is given by:

$0.5 \times (X-195)$ dB for $1 \leq X \leq 255$; MUTE for X = 0

The LAVU and RAVU control bits control the loading of digital volume control data. When LAVU or RAVU are set to 0, the LADCVOL or RADCVOL control data will be loaded into the respective control register, but will not actually change the digital gain setting. Both left and right gain settings are updated when either LAVU or RAVU are set to 1. This makes it possible to update the gain of both channels simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16(10h) Left ADC Digital Volume	7:0	LADCVOL [7:0]	11000011 (0dB)	Left ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -97dB 0000 0010 = -96.5dB ... 0.5dB steps up to 1111 1111 = +30dB
	8	LAVU	0	Left ADC Volume Update 0 = Store LADCVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LADCVOL, right = intermediate latch)
R17 (11h) Right ADC Digital Volume	7:0	RADCVOL [7:0]	11000011 (0dB)	Right ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -97dB 0000 0010 = -96.5dB ... 0.5dB steps up to 1111 1111 = +30dB
	8	RAVU	0	Right ADC Volume Update 0 = Store RADCVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = RADCVOL)

Table 19 ADC Digital Volume Control

AUTOMATIC LEVEL CONTROL (ALC)

The WM8753L has an automatic level control that aims to keep a constant recording volume irrespective of the input signal level. This is achieved by continuously adjusting the PGA gain so that the signal level at the ADC input remains constant. A digital peak detector monitors the ADC output and changes the PGA gain if necessary.

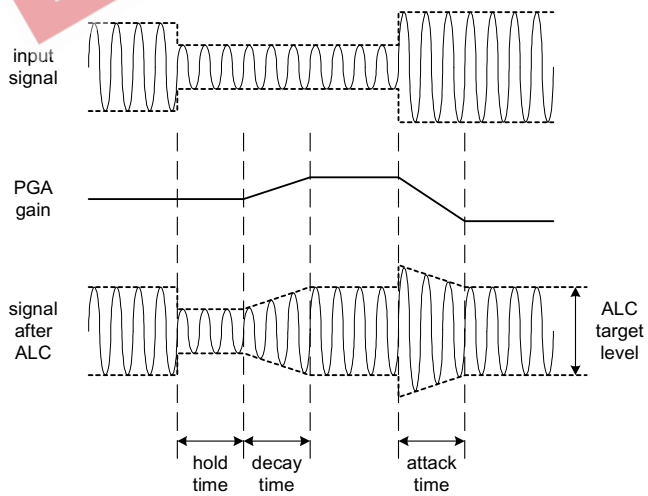


Figure 12 ALC Operation

The ALC function is enabled using the ALCSEL control bits. When enabled, the recording volume can be programmed between –6dB and –28.5dB (relative to ADC full scale) using the ALCL register bits. An upper limit for the PGA gain can be imposed by setting the MAXGAIN control bits.

HLD, DCY and ATK control the hold, decay and attack times, respectively:

Hold time is the time delay between the peak level detected being below target and the PGA gain beginning to ramp up. It can be programmed in power-of-two (2^n) steps, e.g. 2.67ms, 5.33ms, 10.67ms etc. up to 43.7s. Alternatively, the hold time can also be set to zero. The hold time only applies to gain ramp-up, there is no delay before ramping the gain down when the signal level is above target.

Decay (Gain Ramp-Up) Time is the time that it takes for the PGA gain to ramp up across 90% of its range (e.g. from –15B up to 27.75dB). The time it takes for the recording level to return to its target value therefore depends on both the decay time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the decay time. The decay time can be programmed in power-of-two (2^n) steps, from 24ms, 48ms, 96ms, etc. to 24.58s.

Attack (Gain Ramp-Down) Time is the time that it takes for the PGA gain to ramp down across 90% of its range (e.g. from 27.75dB down to -15B gain). The time it takes for the recording level to return to its target value therefore depends on both the attack time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the attack time. The attack time can be programmed in power-of-two (2^n) steps, from 6ms, 12ms, 24ms, etc. to 6.14s.

When operating in stereo, the peak detector takes the maximum of left and right channel peak values, and any new gain setting is applied to both left and right PGAs, so that the stereo image is preserved. However, the ALC function can also be enabled on one channel only. In this case, only one PGA is controlled by the ALC mechanism, while the other channel runs independently with its PGA gain set through the control register.

When one ADC channel is unused or used for DC measurement, the peak detector disregards that channel. The ALC function can also operate when the two ADC outputs are mixed to mono in the digital domain, but not if they are mixed to mono in the analogue domain, before entering the ADCs.

ALCSR is used to set the sample rate for the ALC when the ADC is in voice mode (SRMODE=1). When ALC is enabled in voice mode the ALCSR bits should be set to match the ADC sample rate as shown in Table 20.

ADC SAMPLE RATE	ALCSR [3:0]
8kHz	0110
11.025/12kHz	1000
16kHz	1010
22.05kHz	1010
32kHz	1100
48/44/1kHz	0000
88.2/96kHz	1110

Table 20 ADC Sample Rate

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 (0Ch) ALC Control 1	8:7	ALCSEL [1:0]	00 (OFF)	ALC function select 00 = ALC off (PGA gain set by register) 01 = Right channel only 10 = Left channel only 11 = Stereo (PGA registers unused)
	6:4	MAXGAIN [2:0]	111 (+30dB)	Set Maximum Gain of PGA 111 : +30dB 110 : +24dB ….(-6dB steps) 001 : -6dB 000 : -12dB
	3:0	ALCL [3:0]	1011 (-12dB)	ALC target – sets signal level at ADC input 0000 = -28.5dB FS 0001 = -27.0dB FS … (1.5dB steps) 1110 = -7.5dB FS 1111 = -6dB FS
R13 (0Dh) ALC Control 2	8	ALCZC	0 (zero cross off)	ALC uses zero cross detection circuit.
	7:4	ALCSR[3:0]	0000	ALC sample rate control (only used when in PCM mode, otherwise SR[4:0] bits control the sample rate)
	3:0	HLD [3:0]	0000 (0ms)	ALC hold time before gain is increased. 0000 = 0ms 0001 = 2.67ms 0010 = 5.33ms … (time doubles with every step) 1111 = 43.691s
R14 (0Eh) ALC Control 3	7:4	DCY [3:0]	0011 (192ms)	ALC decay (gain ramp-up) time 0000 = 24ms 0001 = 48ms 0010 = 96ms … (time doubles with every step) 1010 or higher = 24.58s
	3:0	ATK [3:0]	0010 (24ms)	ALC attack (gain ramp-down) time 0000 = 6ms 0001 = 12ms 0010 = 24ms … (time doubles with every step) 1010 or higher = 6.14s

Table 21 ALC Control

PEAK LIMITER

To prevent clipping when a large signal occurs just after a period of quiet, the ALC circuit includes a limiter function. If the ADC input signal exceeds 87.5% of full scale (–1.16dB), the PGA gain is ramped down at the maximum attack rate (as when ATK = 0000), until the signal level falls below 87.5% of full scale. This function is automatically enabled whenever the ALC is enabled.

Note:

1. If ATK = 0000, then the limiter makes no difference to the operation of the ALC. It is designed to prevent clipping when long attack times are used.

NOISE GATE

When the signal is very quiet and consists mainly of noise, the ALC function may cause “noise pumping”, i.e. loud hissing noise during silence periods. The WM8753L has a noise gate function that prevents noise pumping by comparing the signal level at the LINPUT1/2/3 and/or RINPUT1/2/3 pins against a noise gate threshold, NGTH. The noise gate cuts in when:

Signal level at ADC [dB] < NGTH [dB] + PGA gain [dB] + Mic Boost gain [dB]

This is equivalent to:

Signal level at input pin [dB] < NGTH [dB]

The ADC output can then either be muted or alternatively, the PGA gain can be held constant (preventing it from ramping up as it normally would when the signal is quiet).

The table below summarises the noise gate control register. The NGTH control bits set the noise gate threshold with respect to the ADC full-scale range. The threshold is adjusted in 1.5dB steps. Levels at the extremes of the range may cause inappropriate operation, so care should be taken with set–up of the function. Note that the noise gate only works in conjunction with the ALC function, and always operates on the same channel(s) as the ALC (left, right, both, or none).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R15 (0Fh) Noise Gate Control	7:3	NGTH [4:0]	00000	Noise gate threshold 00000 -76.5dBfs 00001 -75dBfs … 1.5 dB steps 11110 -31.5dBfs 11111 -30dBfs
	1	NGG	0	Noise gate type 0 = PGA gain held constant 1 = mute ADC output
	0	NGAT	0	Noise gate function enable 1 = enable 0 = disable

Table 22 Noise Gate Control

3D STEREO ENHANCEMENT

The WM8753L has a digital 3D enhancement option to artificially increase the separation between the left and right channels. This effect can be used for recording or playback, but not for both simultaneously. Selection of 3D for record or playback is controlled by register bit MODE3D. Switching the 3D filter from record to playback or from playback to record may only be done when ADC and DAC are disabled. The WM8753L control interface will only allow MODE3D to be changed when ADC and DAC are disabled (ie ADCL = 0, ADCR = 0, DACL = 0 and DACR = 0).

The 3D enhancement function is activated by the 3DEN bit, and has two programmable parameters. The DEPTH3D setting controls the degree of stereo expansion. Additionally, one of four filter characteristics can be selected for the 3D processing, using the 3DFILT control bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R19 (13h) 3D enhance	7	MODE3D	0	Playback/Record 3D select 0 = 3D selected for Record 1 = 3D selected for Playback
	6	3DUC	0	Upper Cut-off frequency 0 = High (2.2kHz at 48kHz sampling) 1 = Low (1.5kHz at 48kHz sampling)
	5	3DLC	0	Lower Cut-off frequency 0 = Low (200Hz at 48kHz sampling) 1 = High (500Hz at 48kHz sampling)
	4:1	DEPTH3D[3:0]	0000	Stereo depth 0000: 0% (minimum 3D effect) 0001: 6.67% .... 1110: 93.3% 1111: 100% (maximum 3D effect)
	0	3DEN	0	3D function enable 1: enabled 0: disabled

Table 23 3D Stereo Enhancement Function

When 3D enhancement is enabled (and/or the tone control for playback) it may be necessary to attenuate the signal by 6dB to avoid limiting. This is a user selectable function, enabled by setting ADCDIV2 for the record path and DACDIV2 for the playback path.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 (012h) ADC and DAC control	2	ADCDIV2	0	ADC 6dB attenuate enable 0 = disabled (0dB) 1 = -6dB enabled
	1	DACDIV2	0	DAC 6dB attenuate enable 0 = disabled (0dB) 1 = -6dB enabled

Table 24 ADC and DAC 6dB Attenuation Select

OUTPUT SIGNAL PATH

The WM8753L output signal paths consist of digital filters, a stereo Hi-Fi DAC, Voice DAC, analogue mixers and output drivers. The digital filters and DACs are enabled when the WM8753L is in 'playback only' or 'record and playback' mode. The mixers and output drivers can be separately enabled by individual control bits (see Analogue Outputs). Thus it is possible to utilise the analogue mixing and amplification provided by the WM8753L, irrespective of whether the DACs are running or not.

The WM8753L Hi-Fi DAC receives digital input data on the DACDAT pin. The digital filter block processes the data to provide the following functions:

- Digital volume control
- Graphic equaliser and Dynamic Bass Boost
- Sigma-Delta Modulation
- Two high performance sigma-delta audio DACs convert the digital data into two analogue signals (left and right).

The WM8753L Voice DAC receives digital input data on the VXDIN pin which is processed and up-sampled by the digital filters and then sigma delta modulated to provide the analogue voice signal.

The analogue output from the stereo Hi-Fi DAC and the Voice DAC can then be mixed with each other and the analogue signals from the analogue inputs. The mix is fed to the output drivers, LOUT1/ROUT1, LOUT2/ROUT2, OUT3, OUT4, MONO1 and MONO2.

- LOUT1/ROUT1: can drive a 16Ω or 32Ω stereo headphone or stereo line output.
- OUT3: can drive a 16Ω or 32Ω headphone or line output or buffered Vmid
- LOUT2/ROUT2: can drive a 16Ω or 32Ω stereo headphone or stereo line output, or an 8Ω mono speaker.
- MONO1 and MONO2: can drive a mono line output or other load down to 10kΩ
- OUT4: can drive a 16Ω or 32Ω headphone or line output or buffered Vmid.

DIGITAL HI-FI DAC VOLUME CONTROL

The signal volume from each Hi-Fi DAC can be controlled digitally. The gain and attenuation range is –127dB to 0dB in 0.5dB steps. The level of attenuation for an eight-bit code X is given by:

$0.5 \times (X-255)$ dB for $1 \leq X \leq 255$; MUTE for $X = 0$

The LDVU and RDVU control bits control the loading of digital volume control data. When LDVU or RDVU are set to 0, the LDACVOL or RDACVOL control data is loaded into an intermediate register, but the actual gain does not change. Both left and right gain settings are updated simultaneously when either LDVU or RDVU are set to 1.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Left Channel Digital Volume	8	LDVU	0	Left DAC Volume Update 0 = Store LDACVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LDACVOL, right = intermediate latch)
	7:0	LDACVOL [7:0]	11111111 (0dB)	Left DAC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB
R9 (09h) Right Channel Digital Volume	8	RDVU	0	Left DAC Volume Update 0 = Store RDACVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = RDACVOL)
	7:0	RDACVOL [7:0]	11111111 (0dB)	Right DAC Digital Volume Control similar to LDACVOL

Table 25 Digital Volume Control

GRAPHIC EQUALISER

The WM8753L has a digital graphic equaliser and adaptive bass boost function. This function operates on digital audio data before it is passed to the audio DACs. Bass enhancement can take two different forms:

- Linear bass control: bass signals are amplified or attenuated by a user programmable gain. This is independent of signal volume, and very high bass gains on loud signals may lead to signal clipping.
- Adaptive bass boost: The bass volume is amplified by a variable gain. When the bass volume is low, it is boosted more than when the bass volume is high. This method is recommended because it prevents clipping, and usually sounds more pleasant to the human ear.

Treble control applies a user programmable gain, without any adaptive boost function. Bass and treble control are completely independent with separately programmable gains and filter characteristics.

The selectable cut-offs scale with sample frequency to give the following cut-off frequencies at different sample rates

BC[2:0]	CUT-OFF AT FS=8KHZ	CUT-OFF AT FS=16KHZ	CUT-OFF AT FS=48KHZ
000	22Hz	44Hz	130Hz
001	33.3Hz	66.7Hz	200Hz
010	50Hz	100Hz	300Hz
011	66.7Hz	133.3Hz	400Hz
100	100Hz	200Hz	600Hz
101	200Hz	400Hz	1200Hz

Table 26 Bass Filter Cut-off Frequencies for Different Frequencies

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) Bass Control	7	BB	0	Bass Boost 0 = Linear bass control 1 = Adaptive bass boost
	6:4	BC[2:0]	000	Bass Filter Characteristic – cut-off: 000 = 130Hz at fs = 48kHz 001 = 200Hz at fs = 48kHz 010 = 100Hz at fs = 16kHz 011 = 400Hz at fs = 48kHz 100 = 100Hz at fs = 8kHz 101 = 200Hz at fs = 8kHz
	3:0	BASS [3:0]	1111 (Disabled)	Bass Intensity
				Code / BB=0 / BB=1
				0000 / +9dB / 15 (max)
				0001 / +9dB / 14
				0010 / +7.5dB / 13
				0011 / +6dB / 12
				0100 / +4.5dB / 11
				0101 / +3dB / 10
				0110 / +1.5dB / 9
				0111 / 0dB / 8
				1000 / -1.5dB / 7
				1001 / -3dB / 6
				1010 / -4.5dB / 5
				1011 / -6dB / 4
				1100 / -6dB / 3
				1101 / -6dB / 2
				1110 / -6dB / 1
				1111 / Bypass (OFF)
R11 (0Bh) Treble Control	6	TC	0	Treble Filter Characteristic 0 = High Cutoff (8kHz at 48kHz sampling) 1 = Low Cutoff (4kHz at 48kHz sampling)
	3:0	TRBL [3:0]	1111 (Disabled)	Treble Intensity 0000 or 0001 = +9dB 0010 = +7.5dB … (1.5dB steps) 1011 to 1110 = -6dB 1111 = Disable

Table 27 Graphic Equaliser

HI-FI DIGITAL TO ANALOGUE CONVERTER (DAC)

After passing through the graphic equaliser filters, digital 'de-emphasis' can be applied to the audio data if necessary (e.g. when the data comes from a CD with pre-emphasis used in the recording). De-emphasis filtering is available for sample rates of 48kHz, 44.1kHz and 32kHz.

The WM8753L also has a Soft Mute function, which gradually attenuates the volume of the digital signal to zero. When removed, the gain will ramp back up to the digital gain setting. This function is enabled by default. To play back an audio signal, it must first be disabled by setting the DACMU bit to zero.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (01h) DAC Control	2:1	DEEMP [1:0]	00	De-emphasis Control 11 = 48kHz sample rate 10 = 44.1kHz sample rate 01 = 32kHz sample rate 00 = No De-emphasis
	3	DACMU	1	Digital Soft Mute 1 = mute 0 = no mute (signal active)

Table 28 HiFi DAC Control

The digital audio data is converted to oversampled bit streams in the on-chip, true 24-bit digital interpolation filters. The bitstream data enters two multi-bit, sigma-delta DACs, which convert them to high quality analogue audio signals. The multi-bit DAC architecture reduces high frequency noise and sensitivity to clock jitter. It also uses a Dynamic Element Matching technique for high linearity and low distortion.

In normal operation, the left and right channel digital audio data is converted to analogue in two separate DACs. There is also a mono-mix mode where the two audio channels are mixed together digitally, controlled by the DMONOMIX register bits which allow the digital mono mix to be applied to left, right or both DAC channels. If only one DAC channel is being used for the mono mix the other can be powered down.

The DAC output defaults to non-inverted. Setting DACINV will invert the DAC output phase on both left and right channels.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (01h) DAC Control	5:4	DMONOMIX [1:0]	00	DAC Mono Mix 00: stereo 01: mono ((L+R)/2) into DACL, '0' into DACR 10: mono ((L+R)/2) into DACR, '0' into DACL 11: mono ((L+R)/2) into DACL and DACR
	6	DACINV	0	DAC Phase Invert 0 : non-inverted 1 : inverted

Table 29 HiFi DAC Mono Mix and Phase Invert Select

OUTPUT MIXERS

The WM8753L provides the option to mix the Hi-FI DAC output signals and Voice DAC output signal with analogue line-in signals from the bypass and sidetone paths. The level of the mixed-in signals can be controlled with PGAs (Programmable Gain Amplifiers). The Mono mixer has a gain of -6dB to allow two signals with input amplitude of 0dB to be mixed together without clipping. This may be compensated for using the output PGAs if required.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R47 (2Fh) Input Control (1)	[4:3]	LMSEL[1:0]	00	Line Mix Select: 00: LINE1 + LINE2 01: LINE1 – LINE2 10: LINE1 (LINE2 disconnected) 11: LINE2 (LINE1 disconnected)
	2	MM	0	Mono Mux Select 0 : Line Mix Output 1: Rx Mix output (RXP +/– RXN)
	1	RM	0	Right Mux Select 0 : LINE2 1 : Rx Mix output (RXP +/– RXN)
	0	LM	0	Left Mux Select 0 : LINE1 1 : Rx Mix output (RXP +/– RXN)

Table 30 Analogue Input to Output Mixer Bypass Signal Selection (same as Table 4)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R48 (30h) Input Control (2)	[7:6]	RXMSEL[1:0]	00	Differential input, Rx, mixer 00: RXP – RXN 01: RXP + RXN 10: RXP (RXN disconnected) 11: RXN (RXP disconnected)
	[5:4]	MICMUX[1:0]	00	Mic Mux Sidetone Select 00 : Sidetone = Left PGA output 01 : Sidetone = Mic1 preamp output 10 : Sidetone = Mic 2 preamp output 11 : Sidetone = Right PGA output
	3	LINEALC	0	ALC Mix input select Line Mix 0 : Line Mix not selected into ALC Mix 1 : Line Mix selected into ALC Mix
	2	MIC2ALC	0	ALC Mix input select MIC2 0 : MIC2 not selected into ALC Mix 1 : MIC2 selected into ALC Mix
	1	MIC1ALC	0	ALC Mix input select MIC1 0 : MIC1 not selected into ALC Mix 1 : MIC1 selected into ALC Mix
	0	RXALC	0	ALC Mix input select RX 0 : RX not selected into ALC Mix 1 : RX selected into ALC Mix

Table 31 Analogue Input to Output Mixers Sidetone Signal Selection

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R34 (22h) Left Mixer Control (1)	8	LD2LO	0	Left DAC to Left Mixer 0 = Disable (Mute) 1 = Enable Path
	7	LM2LO	0	LM Signal to Left Mixer 0 = Disable (Mute) 1 = Enable Path
	6:4	LM2LOVOL [2:0]	101 (-9dB)	LM Signal to Left Mixer Volume 000 = +6dB … (3dB steps) 111 = -15dB
R35 (23h) Left Mixer Control (2)	8	VXD2LO	0	Voice DAC to Left Mixer 0 = Disable (Mute) 1 = Enable Path
	7	ST2LO	0	Sidetone Signal to Left Mixer 0 = Disable (Mute) 1 = Enable Path
	[6:4]	ST2LOVOL [2:0]	101 (-9dB)	Sidetone Signal to Left Mixer Volume 000 = +6dB … (3dB steps) 111 = -15dB
	[2:0]	VXD2LOVOL	101 (-6dB)	Voice DAC Signal to Left Mixer Volume 000 = +9dB … (3dB steps) 111 = -12dB

Table 32 Left Output Mixer Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R36 (24h) Right Mixer Control (1)	8	RD2RO	0	Right DAC to Right Mixer 0 = Disable (Mute) 1 = Enable Path
	7	RM2RO	0	RM Signal to Right Mixer 0 = Disable (Mute) 1 = Enable Path
	[6:4]	RM2ROVOL [2:0]	101 (-9dB)	RM Signal to Right Mixer Volume 000 = +6dB … (3dB steps) 111 = -15dB
R37 (25h) Right Mixer Control (2)	8	VXD2RO	0	Voice DAC to Right Mixer 0 = Disable (Mute) 1 = Enable Path
	7	ST2RO	0	Sidetone Signal to Right Mixer 0 = Disable (Mute) 1 = Enable Path
	[6:4]	ST2ROVOL [2:0]	101 (-9dB)	Sidetone Signal to Right Mixer Volume 000 = +6dB … (3dB steps) 111 = -15dB
	[2:0]	VXD2ROVOL [2:0]	101 (-6dB)	Voice DAC Signal to Right Mixer Volume 000 = +9dB … (3dB steps) 111 = -12dB

Table 33 Right Output Mixer Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R38 (26h) Mono Mixer Control (1)	8	LD2MO	0	Left DAC to Mono Mixer 0 = Disable (Mute) 1 = Enable Path
	7	MM2MO	0	MM Signal to Mono Mixer 0 = Disable (Mute) 1 = Enable Path
	[6:4]	MM2MOVOL [2:0]	101 (-9dB)	MM Signal to Mono Mixer Volume 000 = +6dB … (3dB steps) 111 = -15dB
R39 (27h) Mono Mixer Control (2)	8	RD2MO	0	Right DAC to Mono Mixer 0 = Disable (Mute) 1 = Enable Path
	7	ST2MO	0	Sidetone Signal to Mono Mixer 0 = Disable (Mute) 1 = Enable Path
	[6:4]	ST2MOVOL [2:0]	101 (-9dB)	Sidetone Signal to Mono Mixer Volume 000 = +6dB … (3dB steps) 111 = -15dB
	3	VXD2MO	0	Voice DAC to Mono Mixer 0 = Disable (Mute) 1 = Enable Path
	[2:0]	VXD2MOVOL [2:0]	101 (-6dB)	Voice Signal to Mono Mixer Volume 000 = +9dB … (3dB steps) 111 = -12dB

Table 34 Mono Output Mixer Control

ANALOGUE OUTPUTS

LOUT1/ROUT1 OUTPUTS

The LOUT1 and ROUT1 pins can drive a 16Ω or 32Ω headphone or a line output (see Headphone Output and Line Output sections, respectively). The signal volume on LOUT1 and ROUT1 can be independently adjusted under software control by writing to LOUT1VOL and ROUT1VOL, respectively. Note that gains over 0dB may cause clipping if the signal is large. Any gain setting below 0101111 (-73dB) mutes the output driver. The corresponding output pin remains at the same DC level (the reference voltage on the VREF pin), so that no click noise is produced when muting or un-muting.

A zero cross detect on the analogue output may also be enabled when changing the gain setting to minimize audible clicks and zipper noise as the gain updates. If zero cross is enabled a timeout is also available to update the gain if a zero cross does not occur. This function may be enabled by setting TOEN in register R18 (12h).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 (28h) LOUT1 Volume	8	LO1VU	0	Left Volume Update 0 = Store LOUT1VOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LOUT1VOL, right = intermediate latch)
	7	LO1ZC	0	Left zero cross enable 1 = Change gain on zero cross only 0 = Change gain immediately
	6:0	LOUT1VOL [6:0]	1111001 (0dB)	LOUT1 Volume 1111111 = +6dB … (1.0 dB steps) 0110000 = -73dB 0101111 to 0000000 = Analogue MUTE
R41 (29h) ROUT1 Volume	8	RO1VU	0	Right Volume Update 0 = Store ROUT1VOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = ROUT1VOL)
	7	RO1ZC	0	Left zero cross enable 1 = Change gain on zero cross only 0 = Change gain immediately
	6:0	ROUT1VOL [6:0]	1111001	ROUT1 Volume Similar to LOUT1VOL

Table 35 LOUT1/ROUT1 Volume Control

LOUT2/ROUT2 OUTPUTS

The LOUT2 and ROUT2 output pins are essentially similar to LOUT1 and ROUT1, but they are independently controlled and can also drive an 8Ω mono speaker (see Speaker Output section). For speaker drive, the ROUT2 signal must be inverted (ROUT2INV = 1), so that the left and right channel are mixed to mono in the speaker [L–(-R) = L+R].

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R42 (2Ah) LOUT2 Volume	6:0	LOUT2VOL [6:0]	1111001 (0dB)	Same as LOUT1VOL
	7	LO2ZC	0	Left zero cross enable 1 = Change gain on zero cross only 0 = Change gain immediately
	8	LO2VU	0	Same as LO1VU
R43 (2Bh) ROUT2 Volume	6:0	ROUT2VOL [6:0]	1111001 (0dB)	Same as ROUT1VOL
	7	RO2ZC	0	Left zero cross enable 1 = Change gain on zero cross only 0 = Change gain immediately
	8	RO2VU	0	Same as RO1VU
R45 (2Dh) Output Control	2	ROUT2INV	0	ROUT2 Invert 0 = No Inversion (0° phase shift) 1 = Signal inverted (180° phase shift)

Table 36 LOUT2/ROUT2 Volume Control

MONO1 OUTPUT

The MONO1 pin can drive a mono line output. The signal volume on MONO1 can be adjusted under software control by writing to MONO1VOL.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R44 (2Ch) MONOOUT Volume	6:0	MONO1VOL [6:0]	1111001 (0dB)	MONO1 Volume 1111111 = +6dB … (1.0 dB steps) 0110000 = -73dB 0101111 to 0000000 = Analogue MUTE
	7	MOZC	0	MONO1 zero cross enable 1 = Change gain on zero cross only 0 = Change gain immediately

Table 37 MONO1 Volume Control

MONO2

The MONO2 pin can drive a mono line output and may be configured to output either an inverted MONO1 output, the output from the left or right mixer or a mono mix of the left and right mixer outputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R45 (2Dh) Output Control	8:7	MONO2SW[1:0]	00	MONO2 Output Select 00 = inverted MONO1 01 = Left Mix / 2 10 = Right Mix / 2 11 = (Left Mix + Right Mix) / 2

Table 38 MONO2 Output Select

OUT3 OUTPUT

The OUT3 pin can drive a 16Ω or 32Ω headphone or a line output or be used as a DC reference for a headphone output (see Headphone Output section). It can be selected to either drive out an inverted ROUT2 or mono mix of the left and right mixers for e.g. an earpiece drive between OUT3 and LOUT1 or differential output between OUT3 and MONOOUT. This output is enabled by setting bit OUT3.

OUT3SW[1:0] selects the mode of operation required.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R45 (2Dh) Output Control	1:0	OUT3SW [1:0]	00	OUT3 select 00 = VREF 01 = ROUT2 signal (volume controlled by ROUT2VOL) 10 = (Left Mixer + Right Mixer) / 2 11 = unused

Table 39 OUT3 Select

OUT4 OUTPUT

The OUT4 output can be used to output a buffered Vmid for driving a mono or stereo headset in capless mode, output the signal from the record mixer or drive out an inverted LOUT2 signal. The output mode is determined by OUT4SW[1:0]. This output is enabled by setting register bit OUT4 high.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R63 (3Fh) Additional Control	8:7	OUT4SW [1:0]	00	OUT4 Output select 00 = VREF 01 = Record Mixer 10 = LOUT2 signal (volume controlled by LOUT2VOL) 11 = unused

Table 40 OUT4SW Control of OUT4

ZERO CROSS TIMEOUT

A zero-cross timeout function is also provided so that if zero cross is enabled on the input or output pgas the gain will automatically update after a timeout period if a zero cross has not occurred. This is enabled by setting TOEN. The timeout period is dependent on the clock input to the digital and is equal to 2^{21} * input clock period. The timeout clock may be set to be derived from either the mclk or pcmclk using SLWCLK..

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 (12h) Additional Control	0	TOEN	0	Timeout clock enable 0 = timeout clock disabled 1 = timeout clock enabled
R52 (34h) Clock Control	0	SLWCLK	0	Timeout and Headphone switch clock source 0 = mclk 1 = pcm clk

Table 41 Timeout Clock Controls

ENABLING THE OUTPUTS

Each analogue output of the WM8753L can be separately enabled or disabled. The analogue mixer associated with each output is powered on or off along with the output pin. All outputs are disabled by default. To save power, unused outputs should remain disabled.

Outputs can be enabled at any time, except when VREF is disabled (VR=0), as this may cause pop noise (see “Power Management” and “Applications Information” sections)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R22 (16h) Power Management (3)	8	LOUT1	0	LOUT1 Enable
	7	ROUT1	0	ROUT1 Enable
	6	LOUT2	0	LOUT2 Enable
	5	ROUT2	0	ROUT2 Enable
	4	OUT3	0	OUT3 Enable
	3	OUT4	0	OUT4 Enable
	2	MONO1	0	MONO1 Enable
	1	MONO2	0	MONO2 Enable
Note: All “Enable” bits are 1 = ON, 0 = OFF				

Table 42 Analogue Output Control

Whenever an analogue output is disabled, it remains connected to VREF (pin 20) through a resistor. This helps to prevent pop noise when the output is re-enabled. The resistance between VREF and L/ROUT1, L/ROUT2 and MONO1 can be controlled using the VROI bit in register 27. The default is low (500Ω), so that any capacitors on the outputs can charge up quickly at start-up. If a high impedance is desired for disabled outputs, VROI can then be set to 1, increasing the resistance to about 90kΩ.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R45 (2Dh) Additional (1)	3	VROI	0	VREF to analogue output resistance 0: 500 Ω 1: 90 kΩ

Table 43 Disabled Outputs to VREF Resistance

HEADPHONE SWITCH

Pin 43 (GPIO4) can be used as a headphone switch control input to automatically disable the speaker output and enable the headphone output e.g. when a headphone is plugged into a jack socket. In this mode, enabled by setting HPSWEN, pin 43 switches between headphone and speaker outputs (e.g. when pin 43 is connected to a mechanical switch in the headphone socket to detect plug-in). The HPSWPOL bit reverses the polarity of pin 43. Note that the LOUT1, ROUT1, LOUT2 and ROUT2 bits in register 22 must also be set for headphone and speaker output (see Table 44 and Table 45). The GPIO4 pin has an internal pull-up/pull-down which can be enabled by setting register bits GPIO4M[1:0]. For cap-less headphone connections a pull-down should be used if VMID is greater than GPIO4 V_{IH}, otherwise a pull-up should be used. GPIO4 can also be used to generate an interrupt. See GPIO and Interrupt Controller Section. The GPIO4 input has a debounce circuit to remove glitches on the input caused by a jack insert in order to prevent the outputs being powered on and off. This debounce circuit is clocked from a slow clock with period = 2^{21} x input clock. The input clock can be selected to be either mclk or pcmclk using SLWCLK.

HPSWEN	HPSWPOL	GPIO4 (pin 43)	L/ROUT1 (reg. 22)	L/ROUT2 (reg. 22)	Headphone enabled	Speaker enabled
0	X	X	0	0	no	no
0	X	X	0	1	no	yes
0	X	X	1	0	yes	no
0	X	X	1	1	yes	yes
1	0	0	X	0	no	no
1	0	0	X	1	no	yes
1	0	1	0	X	no	no
1	0	1	1	X	yes	no
1	1	1	X	0	no	no
1	1	1	X	1	no	yes
1	1	0	0	X	no	no
1	1	0	1	X	yes	no

Table 44 Headphone Switch Operation

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R45 (2Dh) Output Control	6	HPSWEN	0	Headphone Switch Enable 0 : Headphone switch disabled 1 : Headphone switch enabled
	5	HPSWPOL	0	Headphone Switch Polarity 0 : GPIO4 high = headphone 1 : GPIO4 high = speaker
R52 (34h) Clock Control	0	GP2CLK2SEL	0	Timeout and Headphone switch clock source 0 = mclk 1 = pcm clk

Table 45 Headphone Switch

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R27 (1Bh) GPIO Control (1)	2:0	GPIO4M[2:0]	00	Configures GPIO4 pin: 000 = Input only. 001 = unused. 010 = input only with pull-down. 011 = Input only with pull-up. 100 = Drive low. 101 = Drive high. 110 = SDOUT from control interface 111 = INT from interrupt controller

Table 46 GPIO4 Control

THERMAL SHUTDOWN

The speaker and headphone outputs can drive very large currents. To protect the WM8753L from overheating a thermal shutdown circuit is included. If the device temperature reaches approximately 150^0C and the thermal shutdown circuit is enabled (TSDEN = 1) then the speaker and headphone amplifiers (outputs OUT1L/R, OUT2L/R, OUT3 and OUT4) will be disabled if TSDADEN is set. The thermal shutdown may also be configured to generate an interrupt. See the GPIO and Interrupt Controller section for details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R45 (2Dh) Output Control	4	TSDEN	0	Thermal Shutdown Enable 1 : thermal shutdown disabled 0 : thermal shutdown enabled
R63 (3Fh) Additional Control	6	TSDADEN	0	Thermal Shutdown Control 0 : Thermal shutdown will not disable speaker and headphone outputs 1 : Thermal shutdown will automatically disable speaker and headphone outputs

Table 47 Thermal Shutdown

HEADPHONE OUTPUT

Analogue outputs LOUT1/ROUT1, LOUT2/ROUT2, and OUT3/OUT4, can drive a 16Ω or 32Ω headphone load, either through DC blocking capacitors, or DC coupled without any capacitor.

Headphone Output using DC blocking capacitors

DC Coupled Headphone Output (OUT3SW = 00 or OUT4SW=00)

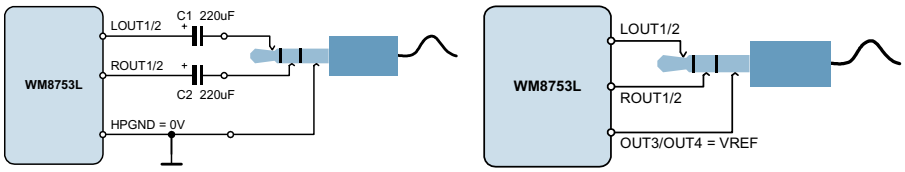


Figure 13 Recommended Headphone Output Configurations

When DC blocking capacitors are used, then their capacitance and the load resistance together determine the lower cut-off frequency, f_c. Increasing the capacitance lowers f_c, improving the bass response. Smaller capacitance values will diminish the bass response. Assuming a 16Ω load and C1, C2 = 220µF:

$f_c = 1 / 2\pi R_L C_1 = 1 / (2\pi \times 16\Omega \times 220\mu F) = 45$ Hz

In the DC coupled configuration, the headphone "ground" is connected to the OUT3 or OUT4 pin. OUT3 is enabled by setting OUT3 = 1 and OUT3SW = 00, while OUT4 is enabled by setting OUT4=1 and OUT4SW=00. As the OUT3 pin produces a DC voltage of AVDD/2 (=VREF), there is no DC offset between LOUT1/ROUT1 and OUT3, and therefore no DC blocking capacitors are required. This saves space and material cost in portable applications.

It is recommended to connect the DC coupled headphone outputs only to headphones, and not to the line input of another device. Although the built-in short circuit protection will prevent any damage to the headphone outputs, such a connection may be noisy, and may not function properly if the other device is grounded.

SPEAKER OUTPUT

LOUT2 and ROUT2 can differentially drive a mono 8Ω speaker as shown below.

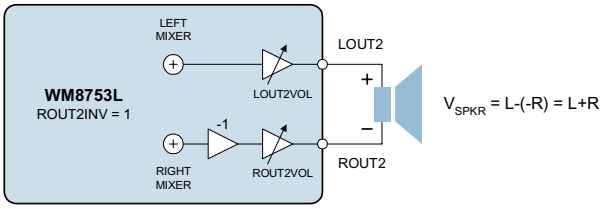


Figure 14 Speaker Output Connection

The right channel is inverted by setting the ROUT2INV bit, so that the signal across the loudspeaker is the sum of left and right channels.

Alternatively it is possible to drive 2 BTL stereo speakers, one between LOUT2 and OUT4, the other between ROUT2 and OUT3, but only to about 250mW/2 due to the limited drive capability of the OUT3/OUT4 outputs.

LINE OUTPUT

The analogue outputs, LOUT1/ROUT1 and LOUT2/ROUT2, can be used as line outputs. Additionally, OUT3 and MONO2 can be used as a stereo line-out by setting OUT3SW=11 (reg. 24) and ensuring the contents of registers 38 and 39 (mono-out mix) are the same as reg. 34 and 35 (left out mix). Recommended external components are shown below.

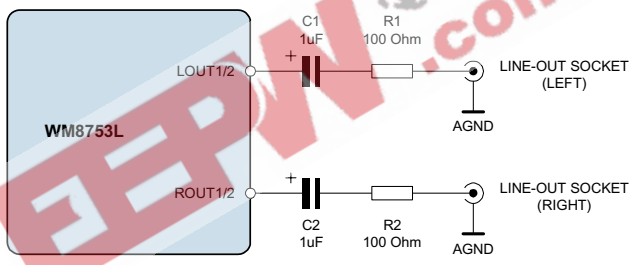


Figure 15 Recommended Circuit for Line Output

The DC blocking capacitors and the load resistance together determine the lower cut-off frequency, f_c. Assuming a 10 kΩ load and C1, C2 = 1µF:

$f_c = 1 / 2\pi (R_L+R_1) C_1 = 1 / (2\pi \times 10.1k\Omega \times 1\mu F) = 16$ Hz

Increasing the capacitance lowers f_c, improving the bass response. Smaller values of C1 and C2 will diminish the bass response. The function of R1 and R2 is to protect the line outputs from damage when used improperly.

INTERRUPT CONTROLLER

The WM8753L can generate an interrupt based on seven separate level-sensitive sources. Each source has programmable polarity and can be individually enabled. On detecting an enabled request with the correct polarity, a status latch for that source is set. If any of the status latches are set, the interrupt controller generates an internal INT signal that can be routed to one of the general purpose pins. The value of the status latches can be obtained over the control interface using the read/write mode. Each latch is cleared by disabling the source in question. Once cleared, the source can be re-enabled if desired. Figure 16 illustrates the operation of the interrupt controller circuit.

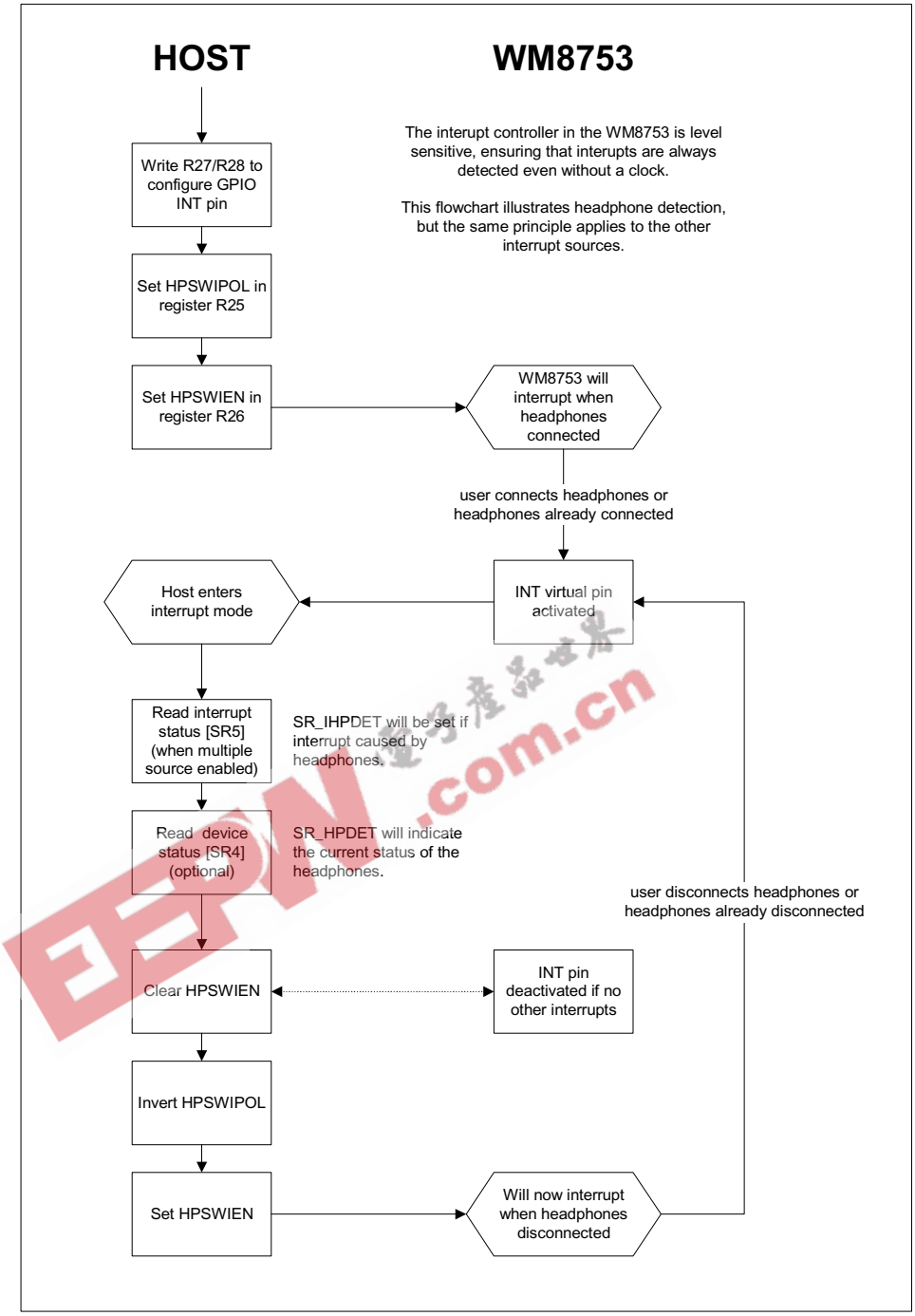


Figure 16 Interrupt Control Flowchart

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Interrupt Polarity	7	TSDIPOL	0	Controls polarity of thermal shutdown interrupts. 0 = Interrupt when thermal shutdown active. 1 = Interrupt when thermal shutdown inactive.
	6	HPSWIPOL	0	Controls polarity of Headphone interrupts. 0 = Interrupt when headphone connected. 1 = Interrupt when headphone disconnected.
	5	GPIO5IPOL	0	Controls polarity of GPIO5 interrupts. 0 = Interrupt when GPIO5 high. 1 = Interrupt when GPIO5 low.
	4	GPIO4IPOL	0	Controls polarity of GPIO4 interrupts. 0 = Interrupt when GPIO4 high 1 = Interrupt when GPIO4 low
	3	GPIO3IPOL	0	Controls polarity of GPIO3 interrupts. 0 = Interrupt when GPIO3 high 1 = Interrupt when GPIO3 low
	1	MICDETPOL	0	Controls polarity of microphone bias detect interrupt 0 = Interrupt when above threshold 1 = Interrupt when below threshold
	0	MICSHTPOL	0	Controls polarity of microphone bias short circuit interrupts. 0 = Interrupt when bias over current 1 = Interrupt when bias normal
R26 (1Ah) Interrupt Mask	7	TSDIEN	0	Controls thermal shutdown interrupt. 1 = Enable interrupt. 0 = Disable interrupt.
	6	HPSWIEN	0	Controls headphone interrupt. 1 = Enable interrupt. 0 = Disable interrupt.
	5	GPIO5IEN	0	Controls GPIO5 interrupt. 1 = Enable interrupt. 0 = Disable interrupt.
	4	GPIO4IEN	0	Controls GPIO4 interrupt. 1 = Enable interrupt. 0 = Disable interrupt.
	3	GPIO3IEN	0	Controls GPIO3 interrupt. 1 = Enable interrupt. 0 = Disable interrupt.
	1	MICDETEN	0	Controls Microphone Bias detect interrupt 1 = Enable interrupt. 0 = Disable interrupt.
	0	MICSHTEN	0	Controls microphone bias short circuit interrupt (button press). 1 = Enable interrupt. 0 = Disable interrupt.
R27 (1Bh) Interrupt Control (1)	8:7	INTCON	00	Controls INT signal from controller. 00 = Disabled (no interrupts). 01 = Open drain active low INT signal. 10 = Active high INT signal. 11 = Active low INT signal. Note that physical pin used for INT is controlled via GPIO Control register.

Table 48 Interrupt Control

GENERAL PURPOSE INPUT/OUTPUT

The WM8753L has four dual purpose input/output pins.

- GP1/CLK1: General purpose output 1, or PLL1 clock output.
- GP2/CLK2: General purpose output 2, or PLL2 clock output.
- GPIO3: General purpose input/output 3 and control interface mode selection input.
- GPIO4: General purpose input/output 4, or head phone detection input.
- GPIO5: General purpose input/output 5 and control interface chip/address select input.

Pin 44 (MODE/GPIO3) is sampled on powerup to determine the control interface mode (2-wire or 3-wire) of the WM8753L. After powerup pin 43 may be used as a GPIO, its use configurable using GPIO3M[2:0].

Pin 45 (CSB/GPIO5) is also sampled on powerup. If 2-wire interface control mode is the value on pin 45 on powerup is used to select the 2-wire address. After powerup, if 2-wire mode is selected, pin 44 may be used as a GPIO, its use configurable using GPIO5M[1:0]. If 3-wire control interface mode is selected pin 44 is always configured as an input and is used as the 3-wire interface latch signal.

Pin 43 (GPIO4) is a dedicated GPIO pin with TTL compatible input thresholds and CMOS output thresholds relative to DBVDD, making it ideal for headphone detection. It also features an optional pull-up/pull-down resistor. GPIO4M[2:0] is used to configure the GPIO4 pin.

Pins 13 and 14 (GP1/CLK1 and GP2/CLK2) are general purpose outputs and may be configured to either output the PLL clock outputs or may be used as general purpose outputs. They are configured using GP1M[2:0] and GP2M[2:0].

In 3-wire interface mode pin GPIO5/CSB cannot be used as a GPIO as it is used to latch the data. Setting GPIO5M to 01, 10 or 11 will prevent the device from being written to in 3-wire mode.

GP2/CLK2 may be configured to output a clock at 256 x the ADC or Hi-Fi DAC sample rate frequency (fs), e.g. if DAC sample rate is set to 8kHz (SR = 00110) output clock will be 256 x 8kHz = 2.048MHz.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R27 (1Bh) GPIO Control (1)	4:3	GPIO5M[1:0]	00	Configures GPIO5 pin. (2-wire interface mode only) 00 = Input only. 01 = INT from interrupt controller. 10 = Drive low. 11 = Drive high.
	2:0	GPIO4M[2:0]	000	Configures GPIO4 pin. 000 = Input only. 001 = unused. 010 = input only with pull-down. 011 = Input only with pull-up. 100 = Drive low. 101 = Drive high. 110 = SDOUT from control interface 111 = INT from interrupt controller
R28 (1Ch) GPIO Control (2)	8:6	GPIO3M[2:0]	000	Configures GPIO3 pin 000 = Input only. 001 to 011 Reserved. 100 = Drive low. 101 = Drive high. 110 = SDOUT from control interface. 111 = INT from interrupt controller.
	5:3	GP2M[2:0]	000	Configures GP2/CLK2 pin when GP2CLK2SEL=0 000 = Drive low. 001 = Drive high. 010 = SDOUT from control interface. 011 = INT from interrupt controller. 100 = ADC clock (=256 x fs) 101 = Hi-Fi DAC clock (=256 x fs) 110 = ADC clock divided by 2 111 = DAC clock divided by 2
	2:0	GP1M[2:0]	000	Configures GP1/CLK1 pin when GP1CLK1SEL=0 000 = Drive low. 001 = Drive high. 010 = SDOUT from control interface. 011 = INT from interrupt controller. 100 to 111 = reserved

Table 49 GPIO Control

Note:

GPIO5 must not be used in 3-wire interface mode. GPIO5 pin is shared with 3-wire interface CSB. Enabling GPIO5 as an output will prevent 3-wire writes to the WM8753L.

DIGITAL AUDIO INTERFACES

The WM8753L has two audio interfaces – a hi-fi audio interface and a voice audio interface. The hi-fi audio interface is used for the input of data to the hi-fi DAC and may also be used to output data from the stereo voice ADC. The voice audio interface is used for the input of data to the voice DAC and for output of data from the voice ADC.

HI-FI AUDIO INTERFACE

The Hi-Fi audio interface has four pins:

- ADCDAT: ADC data output
- DACDAT: DAC data input
- LRC: Data alignment clock
- BCLK: Bit clock, for synchronisation

The clock signals BCLK, and LRC can be outputs when the WM8753L operates as a master, or inputs when it is a slave (see Master and Salve Mode Operation, below).

Four different audio data formats are supported:

- Left justified
- Right justified
- I^2S
- DSP mode

All four of these modes are MSB first. They are described in Audio Data Formats, below. Refer to the Electrical Characteristic section for timing information.

VOICE AUDIO INTERFACE

The voice audio interface has four pins:

- VXDOUT: voice ADC data output
- VXDIN: voice DAC data input
- VXFS: data alignment clock or frame sync
- VXCLK: Bit clock, for synchronisation

The clock signals VXCLK, and VXFS can be outputs when the WM8753L operates as a master, or inputs when it is a slave (see Master and Slave Mode Operation, below). A mixed master/slave mode is also supported where BCLK and VXCLK are outputs from the WM8753L but DACLRC, ADCLRC and VXFS are inputs.

The same four audio modes are supported. The interface can also operate in mono mode where only the left or right channel data is transferred. The DATASEL bits can be used to configure which of the ADCs data is output.

MASTER AND SLAVE MODE OPERATION

The WM8753L audio interfaces may be individually configured as either master or slave interfaces. As a master Hi-Fi interface device the WM8753L generates BCLK and LRC and thus controls sequencing of the data transfer on ADCDAT and DACDAT. As a master voice interface device the WM8753L generates VXCLK and VXFS and thus controls sequencing of the data transfer on VXDIN and VXDOUT. In slave modes, the WM8753L responds with data to clocks it receives over the digital audio interfaces. These modes can be selected by writing to the MS and PMS bits. With the interface configured as a Master the LRC and VXFS outputs may be disabled and configured as inputs using LRCOE and VXFSOE for an external frame sync from the controller to be input. In this mode the generated LRC and VXFS must adhere to the timing requirements diagrams detailed in the Signal Timing Requirements section on page 8. Master, slave and mixed modes are illustrated below.

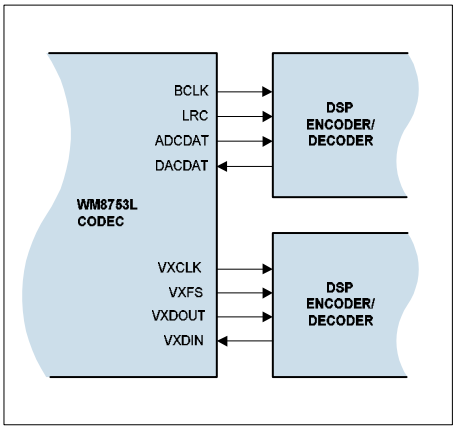


Figure 17a Master Mode

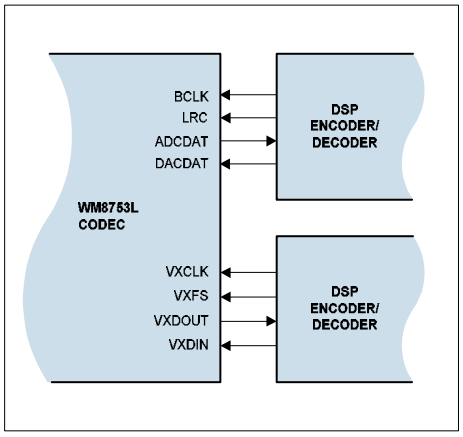


Figure 15b Slave Mode

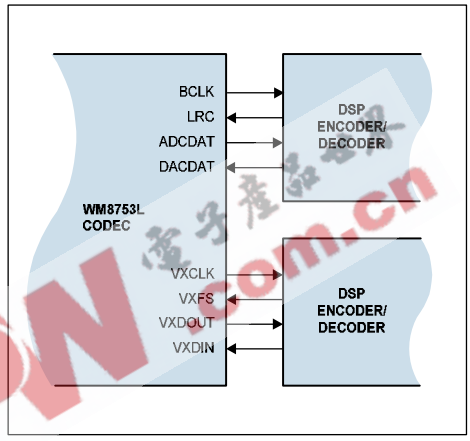


Figure 15c Mixed Mode

AUDIO DATA FORMATS – AUDIO INTERFACE AND VOICE INTERFACE

In Left Justified mode, the MSB is available on the first rising edge of BCLK following an LRC transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRC transition.

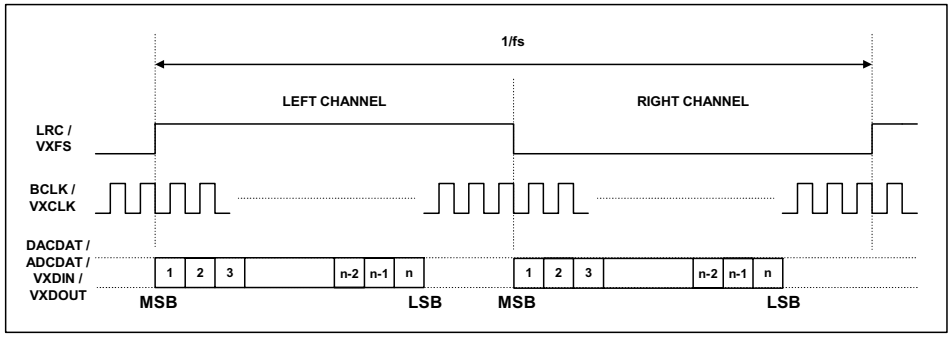


Figure 18 Left Justified Audio Interface (assuming n-bit word length)

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a LRC transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRC transition.

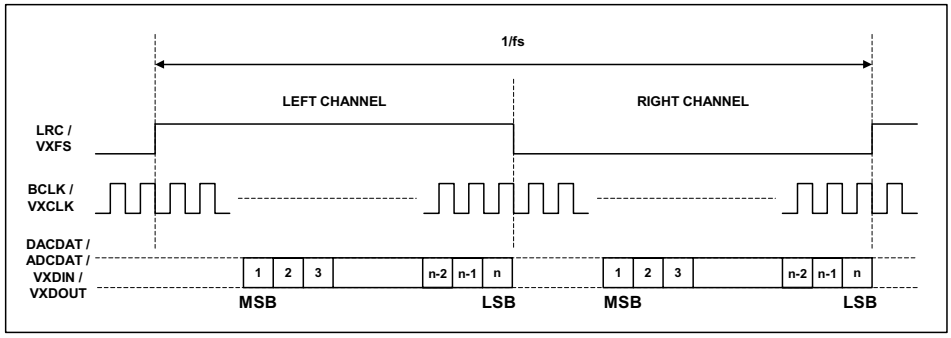


Figure 19 Right Justified Audio Interface (assuming n-bit word length)

In I^2S mode, the MSB is available on the second rising edge of BCLK following a LRC transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

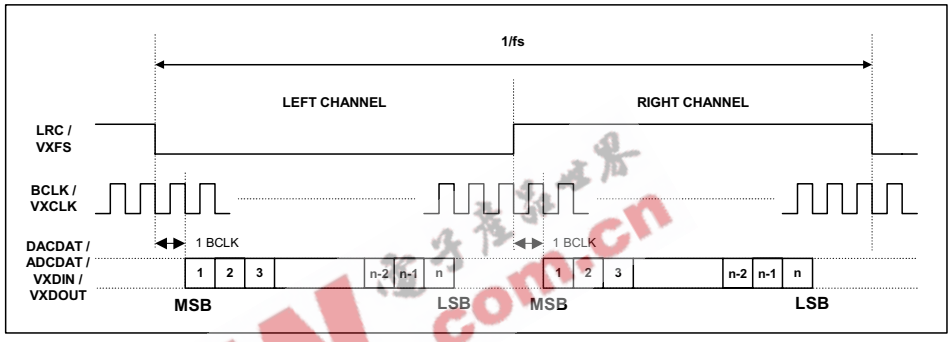


Figure 20 I^2S Justified Audio Interface (assuming n-bit word length)

DSP MODE

In DSP/PCM mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by LRP) following a rising edge of LRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRC output will resemble the frame pulse shown in Figure 21 and Figure 22. In device slave mode, Figure 23 and Figure 24, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

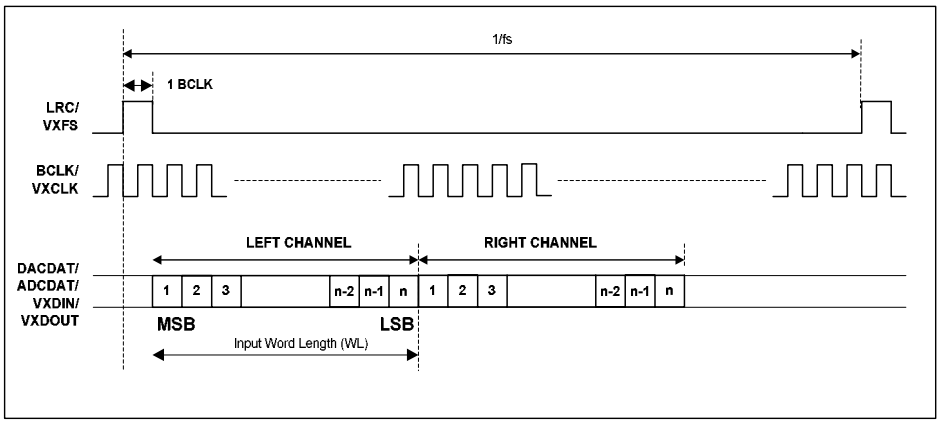


Figure 21 DSP/PCM Mode Audio Interface (mode A, LRP=0, Master)

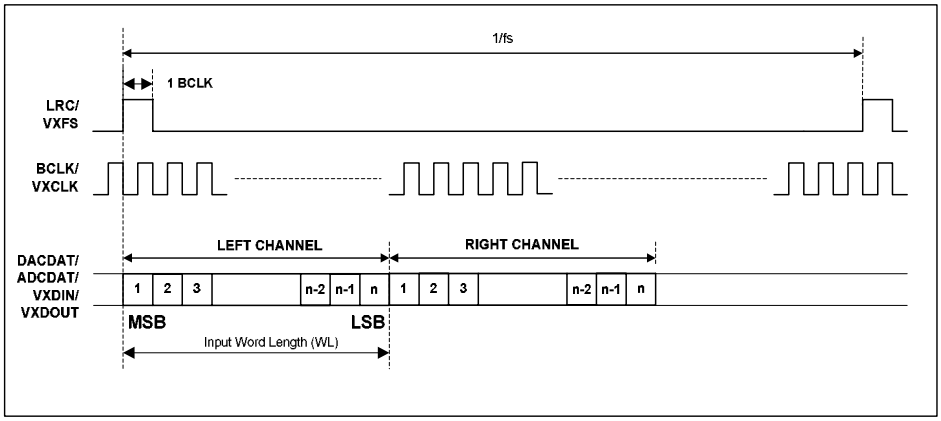


Figure 22 DSP/PCM Mode Audio Interface (mode B, LRP=1, Master)

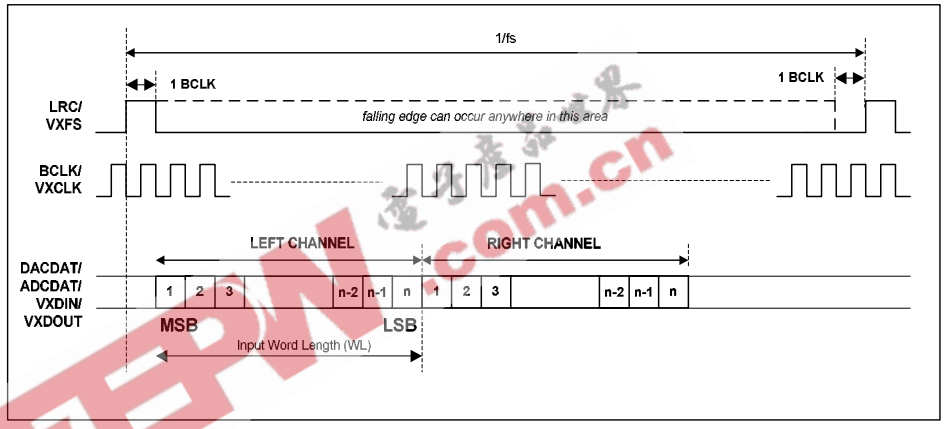


Figure 23 DSP/PCM Mode Audio Interface (mode A, LRP=0, Slave)

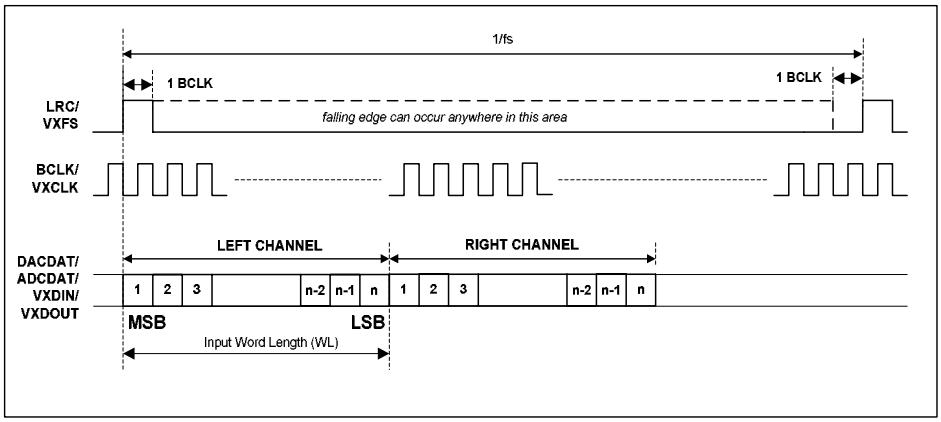


Figure 24 DSP/PCM Mode Audio Interface (mode B, LRP=0, Slave)

The Voice Interface may be configured for Mono mode, where only one channel of data is input or output. In this mode the interface should be configured for DSP mode. A short or long frame sync is supported and the MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of VXCLK.

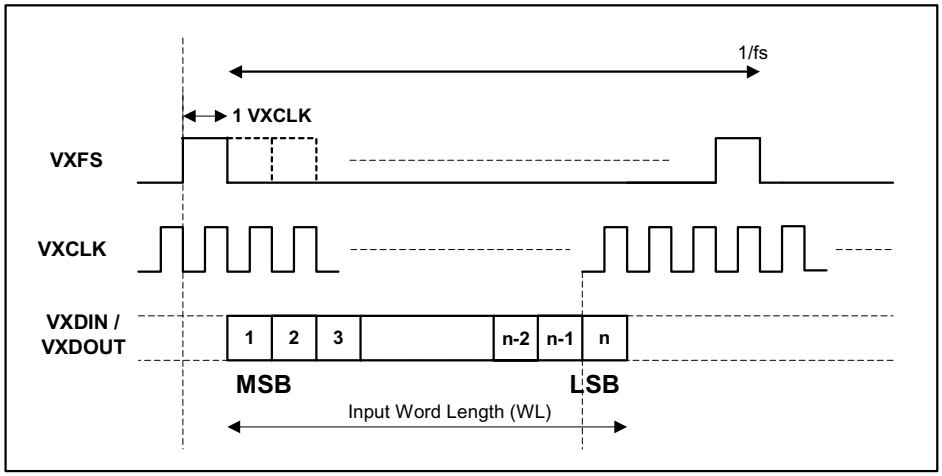


Figure 25 Voice Interface Mono Mode (mode A, PLRP=0)

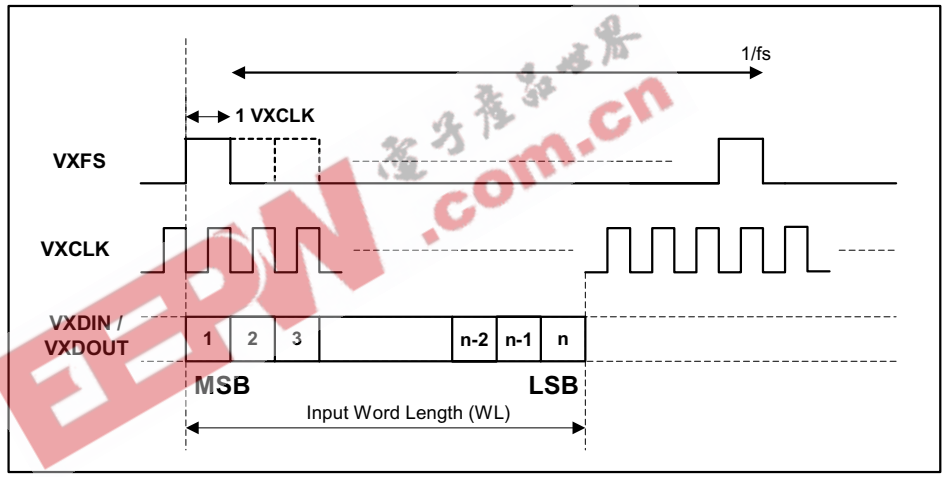


Figure 26 Voice Interface Mono Mode (mode B, PLRP=0)

AUDIO INTERFACES CONTROL

The register bits controlling audio format, word length and master / slave mode are summarised below. Each audio interface can be controlled individually.

MS selects hi-fi audio interface operation in master or slave mode. In Master mode BCLK, and LRC are outputs. The frequency of LRC is set by the sample rate control bits SR[4:0] and USB. In Slave mode BCLK, and LRC are inputs. PMS selects voice audio interface operation in master or slave mode. In master mode VXCLK and VXFS are outputs. The frequency of VXFS is set by PSR. In slave mode VXCLK and VXFS are inputs. The frequency of BCLK and VXCLK may also be selected by the user under the control of BMODE[2:0] and PBMODE[2:0]. BCLK and VXCLK are divided down versions of master clock and in some settings of BMODE and PBMODE this may result in short BCLK and VXCLK pulses at the end of a frame due to a non-integer ratio of BCLKs or VXCLKS to LRC and VXFS.

The WM8753 audio interfaces can be used together in the following modes, under the control of IFMODE[1:0]:

1. Voice CODEC operating over Voice interface, with HiFi DAC operating over HiFi interface.
2. Voice CODEC operating over HiFi interface, with HiFi DAC disabled.
3. Voice DAC disabled, with HiFi ADC and DAC over HiFi interface.
4. Voice DAC disabled, with HiFi ADC and DAC over HiFi interface, using VXFS as framing signal for ADC data, allowing different sample rates for ADC and DAC.

Additionally each interface can operate in a partial master mode, where the bit clock (BCLK or VXCLK) is generated by the WM8753L, but the framing signal (LRC or VXFS) is derived externally. This mode of operation is selected by selecting Master Mode (by setting MS and/or PMS) and then setting LRCOE and/or VXFSOE to '0' to select LRC and/or VXFS as inputs. In Slave mode (MS and PMS = 0) LRC and VXFS are always inputs.

The HiFi DAC audio interface setup is controlled using WL[1:0], FORMAT[1:0] and BCLKINV. The Voice DAC and ADC audio interface setup is controlled using PWL[1:0], PFORMAT[1:0] and VXCLKINV. This allows flexibility in configuring the Voice DAC and ADC separately from the HiFi DAC. Table 50, Table 51 and Table 52 show the configuration for the different interface modes.

1. For Voice CODEC and HiFi DAC mode (IFMODE[1:0] = 00) where the Voice DAC and ADC use the Voice interface the wordlength and format for the voice DAC and ADC are set by PWL[1:0] and PFORMAT[1:0]. The wordlength and format for the HiFi DAC using the HiFi interface are set by WL[1:0] and FORMAT[1:0].
2. For Voice CODEC on HiFi interface mode (IFMODE[1:0] = 01) where the Voice DAC and ADC use the HiFi interface the wordlength and format for the voice DAC and ADC are set by PWL[1:0] and PFORMAT[1:0].
3. For HiFi CODEC mode (IFMODE[1:0]=10) when the DAC and ADC both use the HiFi interface, the wordlength and format for the HiFi DAC are set by WL[1:0] and FORMAT[1:0] and the wordlength and format for the ADC are set by PWL[1:0] and PFORMAT[1:0]. In this mode ADC and DAC share the same BCLK and LRC but the format and wordlength for the ADC and DAC can be configured differently.
4. For HiFi CODEC mode with ADC and DAC at different sample rates (IFMODE[1:0]=11) when the DAC uses LRC and BCLK and the ADC uses VXFA and BCLK , the wordlength and format for the HiFi DAC are set by WL[1:0] and FORMAT[1:0] and the wordlength and format for the ADC are set by PWL[1:0] and PFORMAT[1:0]. In this mode ADC and DAC share the same BCLK but the format and wordlength for the ADC and DAC can be configured differently.

ADC data is usually output on either ADCDAT or VXDOUT. Under the control of ADCDOP, ADC data can be output on ADCDAT and VXDOUT at the same time. The data on ADCDAT and VXDOUT will be synchronous to either LRC and BCLK or VXFS and VXCLK as set by IFMODE[1:0].

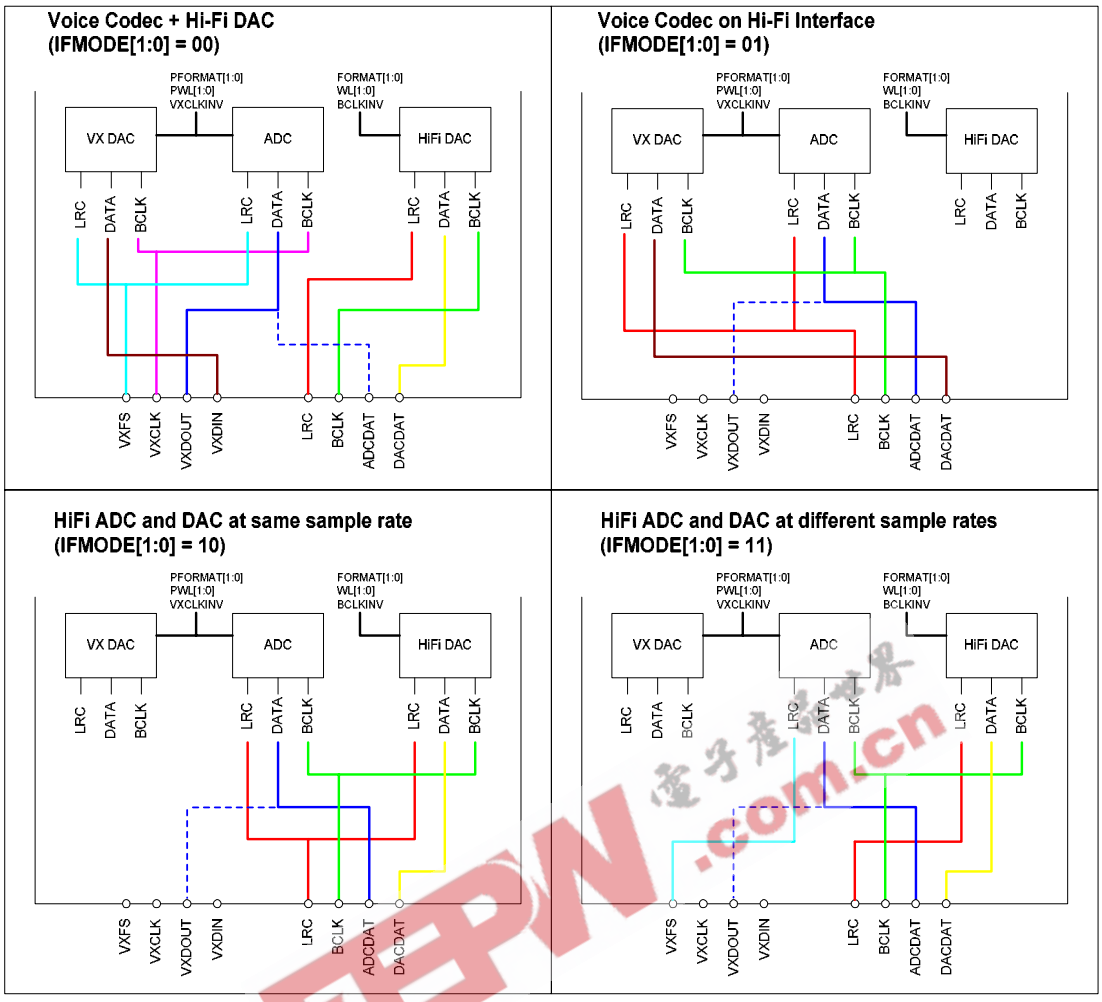


Figure 27 Audio Interface Configuration

IFMODE[1:0]	DAC DATA	DAC FRAME SYNC	DAC BIT CLK	DAC WORDLENGTH	DAC FORMAT
00	DACDAT	LRC	BCLK	WL[1:0]	FORMAT[1:0]
01	DACDAT	LRC	BCLK	WL[1:0]	FORMAT[1:0]
10	DACDAT	LRC	BCLK	WL[1:0]	FORMAT[1:0]
11	DACDAT	LRC	BCLK	WL[1:0]	FORMAT[1:0]

Table 50 Hi-FI DAC Audio Interface Configuration

IFMODE[1:0]	ADC DATA	ADC FRAME SYNC	ADC BIT CLK	ADC WORDLENGTH	ADC FORMAT
00	VXDOUT	VXFS	VXCLK	PWL[1:0]	PFORMAT[1:0]
01	ADCDAT	LRC	BCLK	PWL[1:0]	PFORMAT[1:0]
10	ADCDAT	LRC	BCLK	PWL[1:0]	PFORMAT[1:0]
11	ADCDAT	VXFS	BCLK	PWL[1:0]	PFORMAT[1:0]

Table 51 ADC Audio Interface Configuration

IFMODE[1:0]	VXDAC DATA	VXDAC FRAME SYNC	VXDAC BIT CLK	VXDAC WORDLENGTH	VXDAC FORMAT
00	VXDIN	VXFS	VXCLK	PWL[1:0]	PFORMAT[1:0]
01	DACDAT	LRC	BCLK	PWL[1:0]	PFORMAT[1:0]
10	-	-	-	-	-
11	-	-	-	-	-

Table 52 Voice DAC Audio Interface Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (04h) Digital Hi-Fi Audio Interface Format	7	BCLKINV	0	Hi-Fi DAC BCLK invert bit (for master and slave modes) 0 = BCLK not inverted 1 = BCLK inverted
	6	MS	0	Hi-Fi Interface Master / Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode
	5	LRSWAP	0	Hi-Fi DAC Left/Right channel swap 1 = swap left and right DAC data in audio interface 0 = output left and right data as normal
	4	LRP	0	Hi-Fi DAC right, left and I^2S modes – LRC polarity 1 = invert LRC polarity 0 = normal LRC polarity
				Hi-Fi DAC DSP Mode – mode A/B select 1 = MSB is available on 1st BCLK rising edge after LRC rising edge (mode B) 0 = MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A)
	3:2	WL[1:0]	10	Hi-Fi DAC Audio Data Word Length 11 = 32 bits (see Note) 10 = 24 bits 01 = 20 bits 00 = 16 bits
	1:0	FORMAT[1:0]	10	Hi-Fi DAC Audio Data Format Select 11 = DSP Mode 10 = I^2S Format 01 = Left justified 00 = Right justified

Table 53 Audio Data Format Control
Note: Right Justified mode does not support 32-bit data.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) Digital Audio Interface Control	8:6	PBMODE [2:0]	000	Voice Interface Master mode VXCLK rate select 000 : VXCLK = MCLK 001 : VXCLK = MCLK / 2 010 : VXCLK = MCLK / 4 011 : VXCLK = MCLK / 8 100 : VXCLK = MCLK / 16
	5:3	BMODE [2:0]	000	HiFi Interface Master mode BCLK rate select 000 : BCLK = MCLK 001 : BCLK = MCLK / 2 010 : BCLK = MCLK / 4 011 : BCLK = MCLK / 8 100 : BCLK = MCLK / 16

Table 54 BCLK and VXCLK Master Mode Rate Select

PMS selects Voice audio interface operation in master or slave mode. In Master mode VXCLK and VXFS are outputs. The frequency of FS is set by the sample rate control bits SRMODE and PSR. In Slave mode VXCLK and VXFS are inputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h) Digital Voice Audio Interface Format	8	ADCDOP	0	ADC data output to ADCDAT and VXDOUT enable 0 = ADC data output to ADCDAT or VXDOUT as selected by IFMODE[1:0] 1 = ADC data output to ADCDAT and VXDOUT
	7	VXCLKINV	0	VXCLK invert bit (for master and slave modes) 0 = VXCLK not inverted 1 = VXCLK inverted
	6	PMS	0	Voice Interface Master / Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode
	5	MONO	0	Mono ADC data only 1 = output left channel ADC data only 0 = output left and right ADC data
	4	PLRP	0	Vx DAC and ADC right, left and I^2S modes VXCLK polarity 1 = invert VXCLK polarity 0 = normal VXCLK polarity
				Vx DAC and ADC DSP Mode – mode A/B select 1 = MSB is available on 1st VXCLK rising edge after VXFS rising edge (mode B) 0 = MSB is available on 2nd VXCLK rising edge after VXFS rising edge (mode A)
	3:2	PWL[1:0]	10	Vx DAC and ADC Audio Data Word Length 11 = 32 bits (see Note) 10 = 24 bits 01 = 20 bits 00 = 16 bits
	1:0	PFORMAT[1:0]	10	Vx DAC and ADC Audio Data Format Select 11 = DSP Mode 10 = I^2S Format 01 = Left justified 00 = Right justified

Table 55 Audio Data Format Control

Note: Right Justified mode does not support 32-bit data.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) Digital Audio Interface Control	3:2	IFMODE [1:0]	00	Interface mode 00 = Voice CODEC + HiFi DAC. 01 = Voice CODEC on HiFi interface. 10 = HiFi over HiFi interface. 11 = HiFi over HiFi interface, using VXFS for ADC frame sync.
	1	VXFSOE	1	Configures direction of VXFS pin in master mode 0 = Pin is input 1 = Pin is output
	0	LRCOE	1	Configures direction of LRC pin in master mode 0 = Pin is input 1 = Pin is output

Table 56 Audio Interface Control

Control bits VXCLKTRI, BCLKTRI, VXDTRI and ADCDTRI configure the Hi-Fi and Voice interface pins BCLK, VXCLK, ADCDAT and VXDOUT as inputs or tristate. This allows the I^2S and PCM interfaces to be connected to an interface bus and all outputs onto the bus tristated or switched to inputs. The default state for all audio interface PMS is input or tristate.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) Digital Audio Interface Control	7	VXCLKTRI	0	VXCLK tristate 0 = VXCLK pin configured as input or output as set by PMS 1 = VXCLK pin tristated and used as input
	6	BCLKTRI	0	BCLK tristate 0 = BCLK pin configured as input or output as set by MS 1 = BCLK pin tristated and used as input
	5	VXDTRI	1	VXDOUT tristate 0 = VXDOUT pin enabled as output 1 = VXDOUT pin tristated
	4	ADCDTRI	1	ADCDAT tristate 0 = ADCDAT pin enabled as output 1 = ADCDAT pin tristated

Table 57 PCM and Hi-Fi Interface Tristate

CONTROL INTERFACE

SELECTION OF CONTROL MODE AND 2-WIRE MODE ADDRESS

The control interface can operate as either a 3-wire or 2-wire MPU interface. The MODE/GPIO3 pin is sampled at power-up, latched and used to select the interface format. After power-up MODE/GPIO3 is available for general purpose use. The CSB/GPIO5 pin is also sampled and latched on power-up and, if 2-wire mode is selected, the latched value selects the 2-wire mode address. For 3-wire mode CSB/GPIO5 is always an input. After power-up in 2-wire mode CSB/GPIO5 is available for general purpose use. See MODE/GPIO3 and CSB/GPIO5 LATCH on Power-up Timing Information on page 13.

The WM8753L is controlled by writing to registers through a serial control interface. A control word consists of 16 bits. The first 7 bits (B15 to B9) are address bits that select which control register is accessed. The remaining 9 bits (B8 to B0) are register bits, corresponding to the 9 bits in each control register.

MODE/GPIO3	INTERFACE FORMAT
Low	2 wire
High	3 wire

Table 58 Control Interface Mode Selection

3-WIRE SERIAL CONTROL MODE

In 3-wire mode, every rising edge of SCLK clocks in one data bit from the SDIN pin. A rising edge on GPIO5/CSB latches in a complete control word consisting of the last 16 bits.

In 3-wire mode readback is also available to allow read of a device ID register or interrupt status registers. Readback is enabled by setting READEN. The address of the register to be read back is selected by setting READSEL[2:0]. The readback data can be output on ADCDAT by setting RDDAT or on GPI/CLK1, GP2/CLK2, GPIO3 or GPIO4 by configuring the GPIO pins using control bits GP1M[1:0], GP2M[1:0], GP3M[2:0] and GP4M[2:0].

The SDOUT virtual pin will be tri-state when the CSB pin is high, allowing data from multiple sources to be connected to the same controller.

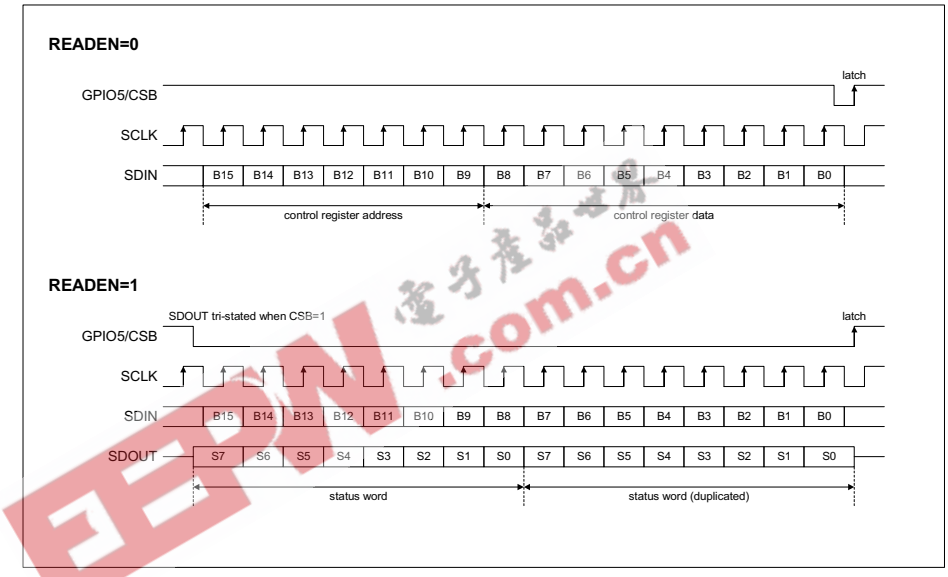


Figure 28 3-Wire Serial Control Interface

2-WIRE SERIAL CONTROL MODE

The WM8753L supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus, and each device has a unique 7-bit device address (this is not the same as the 7-bit address of each register in the WM8753L).

The WM8753L operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8753L, then the WM8753L responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is '1' when operating in write only mode, the WM8753L returns to the idle condition and wait for a new start condition and valid address.

During a write, once the WM8753L has acknowledged a correct address, the controller sends the first byte of control data (B15 to B8, i.e. the WM8753L register address plus the first bit of register data). The WM8753L then acknowledges the first data byte by pulling SDIN low for one clock pulse. The controller then sends the second byte of control data (B7 to B0, i.e. the remaining 8 bits of register data), and the WM8753L acknowledges again by pulling SDIN low.

Transfers are complete when there is a low to high transition on SDIN while SCLK is high. After a complete sequence the WM8753L returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device jumps to the idle condition.

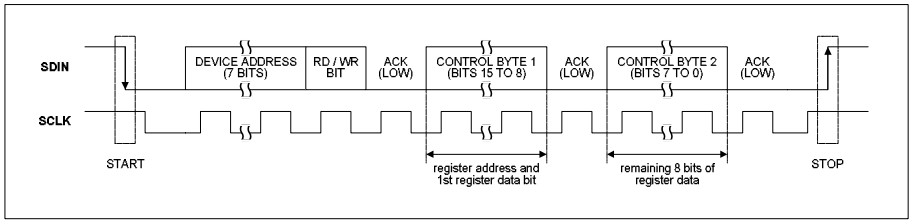


Figure 29 2-Wire Serial Control Interface

The WM8753L has two possible device addresses, which can be selected using the GPIO5/CSB pin. The pin is sampled at power-up and selects the device address. After power-up the pin is available for general purpose use in 2-wire interface mode.

GPIO5/CSB STATE	DEVICE ADDRESS
Low	0011010
High	0011011

Table 59 2-Wire MPU Interface

READ/WRITE OPERATION

The control interface of the WM8753L is a write only interface. However setting register bit READEN in 3-wire mode will allow a status word to be read from the device. A status word consists of 8 bits. Different status words are supported by the device, and are selected by changing the READSEL register bits. The supported words are listed in Table 60.

In 3-wire mode an additional pin is required for serial data output from the device. This data can be routed to the ADCDAT, GP1, GP2, GPIO3 or GPIO4 pins. The pin will be tri-state when the CSB pin is high, allowing data from multiple sources to be connected to the same controller.

In 3-wire mode, reads and write occur simultaneously (i.e. data is clocked in and out at the same time). Usually a read can be paired with a write, but if this is not possible it is recommended that reads be paired with a dummy write to register R0, which is unused.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) Read Control	4	RDDAT	0	Selects ADCDAT as SDOUT for 3-wire readback 0 = ADCDAT not selected for readback 1 = ADCDAT selected for readback
	3:1	READSEL	000	Read register select See table Table 61 below
	0	READEN	0	Control interface read enable 0 = Control interface is write only 1 = Control interface supports read and write.

Table 60 Control Interface Control

READSEL [3:1] VALUE	STATUS REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
000	SR0 (0h) Device ID high	7:0	SR_IDHI	87h	Indicates that device is an 8753L
001	SR1 (1h) Device ID low	7:0	SR_IDLO	53h	
010	SR2 (2h) Device revision	7:0	SR_REV	01h	Device revision
011	SR3 (3h) Device capabilities	7:0	SR_CAP	00h	Device capabilities.
100	SR4 (4h) Device status	7	SR_TSD	0	Thermal shutdown state. 1 = Thermal shutdown detected. 0 = Normal operation.
		6	SR_HPDET	0	Headphone or speaker detect state (see HPSWEN and HPSWPOL). 1 = Headphones connected 0 = Headphones disconnected
		5	SR_GPIO5	0	GPIO5 state. 0 = GPIO5 pin low 1 = GPIO5 pin high
		4	SR_GPIO4	0	GPIO4 state. 0 = GPIO4 pin low 1 = GPIO4 pin high
		3	SR_GPIO3	0	GPIO3 state. 0 = GPIO3 pin low 1 = GPIO3 pin high
		1	SR_IMICDET	0	Microphone bias threshold state 1 = above threshold 0 = below threshold
		0	SR_IMICSHT	0	Microphone bias short circuit state. 1 = Bias short circuit detected 0 = Bias current OK
101	SR5 (5h) Interrupt status	7	SR_ITSD	0	Thermal shutdown interrupt 1 = Interrupt. 0 = No interrupt.
		6	SR_IHPDET	0	Headphone detection interrupt. 1 = Interrupt. 0 = No interrupt.
		5	SR_IGPIO5	0	GPIO5 interrupt. 1 = Interrupt. 0 = No interrupt.
		4	SR_IGPIO4	0	GPIO4 interrupt. 1 = Interrupt. 0 = No interrupt.
		3	SR_IGPIO3	0	GPIO3 interrupt. 1 = Interrupt. 0 = No interrupt.
		1	SR_IMICDET	0	Microphone bias threshold interrupt
		0	SR_IMICSHT	0	Microphone bias short circuit interrupt

Table 61 Status Words

MASTER CLOCK AND PHASE LOCKED LOOP

The WM8753L has two on-chip phase-locked loop (PLL) circuits that can be used to:

- Generate master clocks for the WM8753L audio functions from another external clock, e.g. in telecoms applications.
- Generate a clock for another part of the system from an existing audio master clock.

The user must also select the clock for the HiFi DAC, ADC and Voice DAC. The ADC and Voice DAC are always clocked from the same clock source. The HiFi DAC may be clocked from the same or different clock source to the ADC and Voice DAC. For HiFi CODEC operation, when the ADC is selected for high quality record, the ADC and DAC must be clocked from the same clock source. The PLL and clock select circuit is shown below.

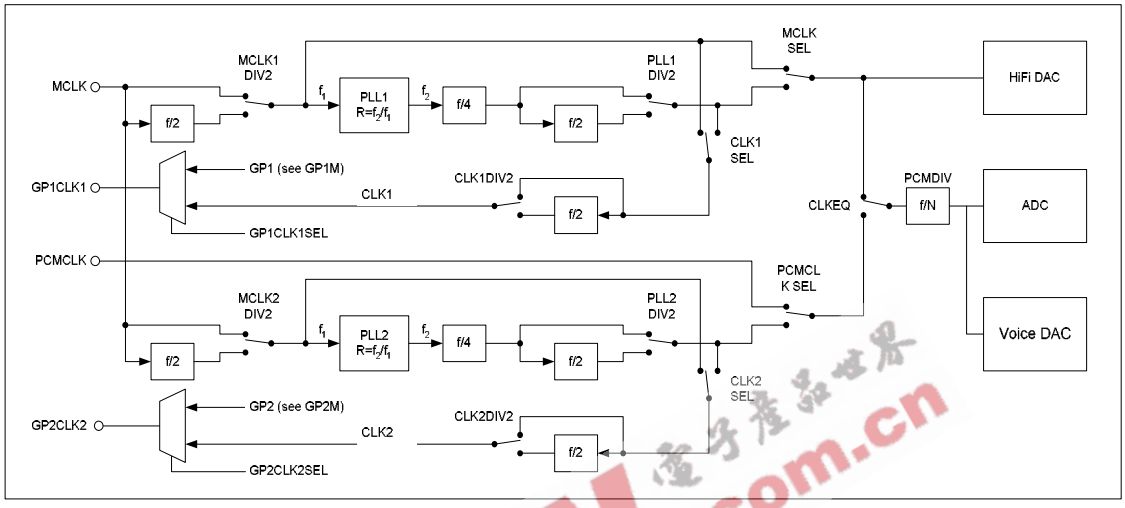


Figure 30 PLL and Clock Select Circuit

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R52 (34h) Clock Control	8:6	PCMDIV[2:0]	000	Control PCM clock divider 000 = divide by 1 (disable) 001 = Unused 010 = Divide by 3 011 = Divide by 5.5 100 = Divide by 2 101 = Divide by 4 110 = Divide by 6 111 = Divide by 8
	4	MCLKSEL	0	Select internal master clock for HiFi CODEC 0: from MCLK pin 1: from PLL1 (ensure PLL1EN=1)
	3	PCMCLKSEL	0	Select internal master clock for Voice CODEC 0: from PCMCLK pin 1: from PLL2 (ensure PLL2EN=1)
	2	CLKEQ	1	Select clock for Voice CODEC 0: PCMCLK or PLL2 clock 1: same as HiFi DAC (MCLK or PLL1 clock)
	1	GP1CLK1SEL	0	GP1CLK1 select 0 = GP1 output 1 = CLK1 output
	0	GP2CLK2SEL	0	GP2/CLK2 select 0 = GP2 output 1 = CLK2 output

R53 (35h) PLL1 Control (1)	5	CLK1SEL	0	CLKOUT1 select 0 : from MCLK pin 1 : from PLL1
	4	CLK1DIV2	0	CLKOUT1 Divide by 2 (see Note 1) 0 : Divide by 2 disabled 1 : Divide by 2 enabled
	3	MCLK1DIV2	0	MCLK Divide by 2 0 : Divide by 2 disabled 1 : Divide by 2 enabled
	2	PLL1DIV2	0	PLL1 Output Divide by 2 0 : Divide disabled 1 : Divide enabled
	1	PLL1RB	0	PLL1 reset 0 : PLL reset 1 : PLL active
	0	PLL1EN	0	PLL 1 Enable 0 : Disabled 1 : Enabled
R57 (39h) PLL2 Control (1)	5	CLK2SEL	0	CLKOUT2 select 0 : from MCLK pin 1 : from PLL2
	4	CLK2DIV2	0	CLKOUT2 Divide by 2 (see Note 1) 0 : Divide by 2 disabled 1 : Divide by 2 enabled
	3	MCLK2DIV2	0	MCLK Divide by 2 0 : Divide by 2 disabled 1 : Divide by 2 enabled
	2	PLL2DIV2	0	PLL2 Output Divide by 2 0 : Divide disabled 1 : Divide enabled
	1	PLL2RB	0	PLL2 reset 0 : PLL reset 1 : PLL active
	0	PLL2EN	0	PLL2 Enable 0 : Disabled 1 : Enabled

Table 62 PLL and Clocking Control

Note:

1. PLL1RB must be set to '1' before CLK1DIV2 will function

   PLL2RB must be set to '1' before CLK2DIV2 will function

The PLL frequency ratio R = f_2/f_1 (see

Figure **30**) can be set using K and N:

N = int R

K = int (2^{22} (R-N))

Example:

mclk=12MHz, required clock = 12.288MHz.

R should be chosen to ensure 5 < N < 13. There is a divide by 4 and a selectable divide by 2 after the PLL which should be set to meet this requirement. Enabling the divide by 2 sets the required f_2 = 8 x 12.288MHz = 98.304MHz.

R = 98.304 / 12 = 8.192

N = int R = 8

k = int (2^{22} x (8.192 – 8)) = 805306 = C49BAh

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R54 (36h) PLL1 Control (2)	8:5	PLL1N	0100	Integer (N) part of PLL1 input/output frequency ratio. Use values greater than 5 and less than 13.
	3:0	PLL1K [21:18]	0011	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 22-digit binary number).
R55 (37h) PLL1 Control (3)	8:0	PLL1K [17:9]	024h	
R56 (38h) PLL1 Control (4)	8:0	PLL1K [8:0]	1BAh	

Table 63 PLL1 Frequency Ratio Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R58 (3Ah) PLL2 Control (2)	8:5	PLL2N	0100	Integer (N) part of PLL2 input/output frequency ratio. Use values greater than 5 and less than 13.
	3:0	PLL2K [21:18]	0011	Fractional (K) part of PLL2 input/output frequency ratio (treat as one 22-digit binary number)
R59 (3Bh) PLL2 Control (2)	8:0	PLL2K [17:9]	024h	
R60 (3Ch) PLL2 Control (3)	8:0	PLL2K [8:0]	1BAh	

Table 64 PLL2 Frequency Ratio Control

The PLL performs best when f_2 is around 90MHz. Its stability peaks at N=8. Some example settings are shown below.

MCLK (MHz) (F1)	DESIRED OUTPUT (MHz)	F2 (MHz)	MCLK DIV2	PLL OUT DIV2	CLK OUT DIV2	R	N (Hex)	K (Hex)
11.91	11.2896	90.3168	0	1	0	7.5833	7	25545F
11.91	12.288	98.304	0	1	0	8.2539	8	103FF8
12	11.2896	90.3168	0	1	0	7.5264	7	21B08A
12	12.288	98.304	0	1	0	8.192	8	C49BA
13	11.2896	90.3168	0	1	0	6.9474	6	3CA2F5
13	12.288	98.304	0	1	0	7.5618	7	23F54A
14.4	11.2896	90.3168	0	1	0	6.272	6	116873
14.4	12.288	98.304	0	1	0	6.8267	6	34E81B
19.2	11.2896	90.3168	1	1	0	9.408	9	1A1CAC
19.2	12.288	98.304	1	1	0	10.24	A	F5C29
19.68	11.2896	90.3168	1	1	0	9.1785	9	B6D25
19.68	12.288	98.304	1	1	0	9.9902	9	3F6028
19.8	11.2896	90.3168	1	1	0	9.1229	9	7DDBE
19.8	12.288	98.304	1	1	0	9.9297	9	3B8028
24	11.2896	90.3168	1	1	0	7.5264	7	21B08A
24	12.288	98.304	1	1	0	8.192	8	C49BA
26	11.2896	90.3168	1	1	0	6.9474	6	3CA2F5
26	12.288	98.304	1	1	0	7.5618	7	23F54A
27	11.2896	90.3168	1	1	0	6.6901	6	2C2B25
27	12.288	98.304	1	1	0	7.2818	7	1208A6

Table 65 PLL Frequency Examples

AUDIO SAMPLE RATES

The WM8753L has two modes of operation for the HiFi DAC, ADC and voice DAC sample rates, selectable using control bit SRMODE:

HiFi ADC and DAC at different sample rates Mode (IFMODE [1:0] = 11) SRMODE=0. HiFi DAC and stereo ADC used for high quality playback and record. The Voice DAC is unused. Sample rate control is via control bits SR[4:0] and USB.

Voice CODEC + HiFi DAC Mode (IFMODE [1:0] =00) SRMODE = 1. HiFi DAC is used for high quality playback; Stereo (or mono) ADC and voice DAC are used for voice record and playback. HiFi DAC Sample rate is controlled by SR[4:0] and USB. Voice CODEC sample rate is controlled by PSR.

In either mode of operation the ADCs and DACs may be powered off if not required to allow e.g. HiFi DAC playback only, with ADCs disabled. The HiFi DAC sample rate is always controlled by SR[4:0] and USB.

HIFI CODEC MODE

In this mode the Voice DAC is unused and the stereo ADC is used for HiFi record.The WM8753L may be configured to run from a clock generated by the on-chip PLL or may be driven from an external clock connected to the MCLK pin. The WM8753L supports a wide range of master clock frequencies on the MCLK pin, and can generate many commonly used audio sample rates directly from the master clock. In HiFi CODEC Mode the ADC and DAC do not need to run at the same sample rate; several different combinations are possible.

There are two clocking modes:

- 'Normal' mode supports master clocks of $128f_s$, $192f_s$, $256f_s$, $384f_s$, and their multiples (Note: f_s refers to the ADC or DAC sample rate, whichever is faster)
- USB mode supports 12MHz or 24MHz master clocks. This mode is intended for use in systems with a USB interface, and eliminates the need for the internal PLL to generate the clock frequency for the audio CODEC.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) Sample Rate Control (1)	8	SRMODE	0	ADC Sample rate mode 0 – ADC sample rate selected by SR[4:0] and USB 1 – ADC sample rate selected by PSR
	[5:1]	SR [4:0]	00000	Sample Rate Control
	0	USB	0	Clocking Mode Select 1 = USB Mode 0 = 'Normal' Mode

Table 66 Clocking and Sample Rate Control

The clocking of the WM8753L Hi-Fi CODEC is controlled using the MCLK1DIV2, USB, and SR control bits. SR allows the user to change the ADC and DAC sample rates without changing the master clock frequency. Setting the MCLK1DIV2 bit divides MCLK by two internally. The USB bit selects between 'Normal' and USB mode. Each value of SR[4:0] selects one combination of MCLK division ratios and hence one combination of sample rates (see next page). Since all sample rates are generated by dividing MCLK, their accuracy depends on the accuracy of MCLK. If MCLK changes, the sample rates change proportionately.

Note that some sample rates (e.g. 44.1kHz in USB mode) are approximated, i.e. they differ from their target value by a very small amount. This is not audible, as the maximum deviation is only 0.27% (8.0214kHz instead of 8kHz in USB mode). By comparison, a half-tone step corresponds to a 5.9% change in pitch.

MCLK CLKDIV2=0	MCLK CLKDIV2=1	ADC SAMPLE RATE	DAC SAMPLE RATE	USB	SR [4:0]	FILTER TYPE
'Normal' Clock Mode ('*' indicates backward compatibility with WM8731)						
12.288MHz	24.576MHz	8 kHz (MCLK/1536)	8 kHz (MCLK/1536)	0	00110 *	1
		8 kHz (MCLK/1536)	48 kHz (MCLK/256)	0	00100 *	1
		12 kHz (MCLK/1024)	12 kHz (MCLK/1024)	0	01000	1
		16 kHz (MCLK/768)	16 kHz (MCLK/768)	0	01010	1
		24 kHz (MCLK/512)	24 kHz (MCLK/512)	0	11100	1
		32 kHz (MCLK/384)	32 kHz (MCLK/384)	0	01100 *	1
		48 kHz (MCLK/256)	8 kHz (MCLK/1536)	0	00010 *	1
		48 kHz (MCLK/256)	48 kHz (MCLK/256)	0	00000 *	1
		96 kHz (MCLK/128)	96 kHz (MCLK/128)	0	01110 *	3
11.2896MHz	22.5792MHz	8.0182 kHz (MCLK/1408)	8.0182 kHz (MCLK/1408)	0	10110 *	1
		8.0182 kHz (MCLK/1408)	44.1 kHz (MCLK/256)	0	10100 *	1
		11.025 kHz (MCLK/1024)	11.025 kHz (MCLK/1024)	0	11000	1
		22.05 kHz (MCLK/512)	22.05 kHz (MCLK/512)	0	11010	1
		44.1 kHz (MCLK/256)	8.0182 kHz (MCLK/1408)	0	10010 *	1
		44.1 kHz (MCLK/256)	44.1 kHz (MCLK/256)	0	10000 *	1
		88.2 kHz (MCLK/128)	88.2 kHz (MCLK/128)	0	11110 *	3
18.432MHz	36.864MHz	8 kHz (MCLK/2304)	8 kHz (MCLK/2304)	0	00111 *	1
		8 kHz (MCLK/2304)	48 kHz (MCLK/384)	0	00101 *	1
		12 kHz (MCLK/1536)	12 kHz (MCLK/1536)	0	01001	1
		16kHz (MCLK/1152)	16 kHz (MCLK/1152)	0	01011	1
		24kHz (MCLK/768)	24 kHz (MCLK/768)	0	11101	1
		32 kHz (MCLK/576)	32 kHz (MCLK/576)	0	01101 *	1
		48 kHz (MCLK/384)	48 kHz (MCLK/384)	0	00001 *	1
		48 kHz (MCLK/384)	8 kHz (MCLK/2304)	0	00011 *	1
		96 kHz (MCLK/192)	96 kHz (MCLK/192)	0	01111 *	3
16.9344MHz	33.8688MHz	8.0182 kHz (MCLK/2112)	8.0182 kHz (MCLK/2112)	0	10111 *	1
		8.0182 kHz (MCLK/2112)	44.1 kHz (MCLK/384)	0	10101 *	1
		11.025 kHz (MCLK/1536)	11.025 kHz (MCLK/1536)	0	11001	1
		22.05 kHz (MCLK/768)	22.05 kHz (MCLK/768)	0	11011	1
		44.1 kHz (MCLK/384)	8.0182 kHz (MCLK/2112)	0	10011 *	1
		44.1 kHz (MCLK/384)	44.1 kHz (MCLK/384)	0	10001 *	1
		88.2 kHz (MCLK/192)	88.2 kHz (MCLK/192)	0	11111 *	3
USB Mode ('*' indicates backward compatibility with WM8731)						
12.000MHz	24.000MHz	8 kHz (MCLK/1500)	8 kHz (MCLK/1500)	1	00110 *	0
		8 kHz (MCLK/1500)	48 kHz (MCLK/250)	1	00100 *	0
		8.0214 kHz (MCLK/1496)	8.0214kHz (MCLK/1496)	1	10111 *	1
		8.0214 kHz (MCLK/1496)	44.118 kHz (MCLK/272)	1	10101 *	1
		11.0259 kHz (MCLK/1088)	11.0259kHz (MCLK/1088)	1	11001	1
		12 kHz (MCLK/1000)	12 kHz (MCLK/1000)	1	01000	0
		16kHz (MCLK/750)	16kHz (MCLK/750)	1	01010	0
		22.0588kHz (MCLK/544)	22.0588kHz (MCLK/544)	1	11011	1
		24kHz (MCLK/500)	24kHz (MCLK/500)	1	11100	0
		32 kHz (MCLK/375)	32 kHz (MCLK/375)	1	01100 *	0
		44.118 kHz (MCLK/272)	8.0214kHz (MCLK/1496)	1	10011 *	1
		44.118 kHz (MCLK/272)	44.118 kHz (MCLK/272)	1	10001 *	1
		48 kHz (MCLK/250)	8 kHz (MCLK/1500)	1	00010 *	0
		48 kHz (MCLK/250)	48 kHz (MCLK/250)	1	00000 *	0
		88.235kHz (MCLK/136)	88.235kHz (MCLK/136)	1	11111 *	3
		96 kHz (MCLK/125)	96 kHz (MCLK/125)	1	01110 *	2

Table 67 Master Clock and Sample Rates

HIFI DAC + VOICE CODEC MODE

In this mode the stereo ADC and voice DAC are used for voice record and playback and the HiFi DAC is used for high quality playback. The HiFi DAC may be powered off for voice CODEC only operation. In this mode the sample rate for the HiFi DAC is controlled using SR[4:0] and USB, as detailed in the HIFI CODEC Mode section above. The Voice DAC and ADC sample rate is controlled by PSR. In this mode the Voice DAC and ADC sample rate is derived from the master clock selected for the voice DAC and ADC (see Figure 30). The Voice CODEC and HiFi DAC may operate at different sample rates from the same or separate master clocks. e.g. for HiFI DAC operation at fs=48kHz and voice CODEC operation at fs=8kHz with mclk = 12.288MHz. PCMDIV (reg52) should be set to divide mclk by 6 to provide a 2.048Mhz (= 256 x 8kHz) clock for the voice DAC and ADC.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) Sample Rate Control	8	SRMODE	0	ADC Sample rate mode 0 – ADC sample rate selected by SR[4:0] and USB 1 – ADC sample rate selected by PSR[1:0]
	7	PSR	0	Voice CODEC Sample Rate Control 0 – 256fs mode 1 – 384fs mode

Table 68 Clocking and Sample Rate Control

The clocking of the WM8753L voice CODEC is controlled using the PSR control bits. If MCLK changes, the sample rates change proportionately.

POWER SUPPLIES

The WM8753L can use up to four separate power supplies:

- AVDD and AGND: Analogue supply, powers all analogue functions except the headphone drivers. AVDD can range from 1.8V to 3.6V and has the most significant impact on overall power consumption (except for power consumed in the headphone). A large AVDD slightly improves audio quality.
- HPVDD, SPKRVDD and HP/SPKRGND: Headphone and Speaker supplies, power the headphone and speaker drivers. HPVDD and SPKRVDD can range from 1.8V to 3.6V. HPVDD and SPKRVDD are normally tied to AVDD, but it requires separate layout and decoupling capacitors to curb harmonic distortion. With a larger HPVDD and SPKRVDD, louder headphone and speaker outputs can be achieved with lower distortion. If HPVDD and /or SPKRVDD are lower than AVDD, the output signal may be clipped.
- PLLVDD and PLLGND. PLL supplies, power the two on-chip PLLs. PLLVDD can range from 1.8V to 3.6V.
- DCVDD: Digital core supply, powers all digital functions except the audio and control interfaces. DCVDD can range from 1.42V to 3.6V, and has no effect on audio quality. The return path for DCVDD is DGND, which is shared with DBVDD.
- DBVDD: Digital buffer supply, powers the audio and control interface buffers. This makes it possible to run the digital core at very low voltages, saving power, while interfacing to other digital devices using a higher voltage. DBVDD draws much less power than DCVDD, and has no effect on audio quality. DBVDD can range from 1.8V to 3.6V. The return path for DBVDD is DGND, which is shared with DCVDD.

It is possible to use the same supply voltage on all four. However, digital and analogue supplies should be routed and decoupled separately to keep digital switching noise out of the analogue signal paths.

POWER MANAGEMENT

The WM8753L has three control registers that allow users to select which functions are active. For minimum power consumption, unused functions should be disabled. To avoid any pop or click noise, it is important to enable or disable functions in the correct order (see Applications Information). VMIDSEL is the enable for the Vmid reference, which defaults to disabled and can be enabled as a 50kΩ potential divider or, for low power maintenance of Vref when all other blocks are disabled, as a 500kΩ potential divider.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R20 (14h) Power Management (1)	8:7	VMIDSEL	00	Vmid divider enable and select 00 – Vmid disabled (for OFF mode) 01 – 50kΩ divider enabled (for playback/record) 10 – 500kΩ divider enabled (for low-power standby) 11 – 5kΩ divider enabled (for fast start-up)
	6	VREF	0	VREF enable (necessary for all other functions) 0=VREF is powered down 1=VREF is powered up
	5	MICB	0	MIC Bias enable 0=MICB is powered down 1=MICB is powered up
	4	VDAC	0	Voice DAC enable 0=VDAC is powered down 1= VDAC is powered up
	3	DACL	0	DAC Left enable 0=DACL is powered down 1= DACL is powered up
	2	DACR	0	DAC Right enable 0=DACR is powered down 1=DACR is powered up
	0	DIGENB	0	Disables MCLK into digital 0=MCLK is enabled 1= MCLK is disabled
R21 (15h) Power Management (2)	8	MICAMP1EN	0	Mic1 preamp enable 0=MICAMP1EN is powered down 1=MICAMP1EN is powered up
	7	MICAMP2EN	0	Mic2 preamp enable 0=MICAMP2EN is powered down 1=MICAMP2EN is powered up
	6	ALCMIX	0	ALC mixer enable 0=ALCMIX is powered down 1=ALCMIX is powered up
	5	PGAL	0	ADC left PGA enable 0=PGAL is powered down 1=PGAL is powered up
	4	PGAR	0	ADC right PGA enable 0=PGAR is powered down 1=PGAR is powered up
	3	ADCL	0	Left ADC enable 0=ADCL is powered down 1=ADCL is powered up
	2	ADCR	0	Right ADCR enable 0=ADCR is powered down 1=ADCR is powered up
	1	RXMIX	0	RX mixer enable 0=RXMIX is powered down 1=RXMIX is powered up

	0	LINEMIX	0	Line mixer enable 0=LINEMIX is powered down 1=LINEMIX is powered up
R22 (16h) Power Management (3)	8	LOUT1	0	LOUT1 enable 0=LOUT1 is powered down 1=LOUT1 is powered up
	7	ROUT1	0	ROUT1 enable 0=ROUT1 is powered down 1=ROUT1 is powered up
	6	LOUT2	0	LOUT2 enable 0=LOUT2 is powered down 1=LOUT2 is powered up
	5	ROUT2	0	ROUT2 enable 0=ROUT2 is powered down 1=ROUT2 is powered up
	4	OUT3	0	OUT3 enable 0=OUT3 is powered down 1=OUT3 is powered up
	3	OUT4	0	OUT4 enable 0=OUT4 is powered down 1=OUT4 is powered up
	2	MONO1	0	MONO1 enable 0=MONO1 is powered down 1=MONO1 is powered up
	1	MONO2	0	MONO2 enable 0=MONO2 is powered down 1=MONO2 is powered up
R23 (17h) Power Management (4)	3	RECMIX	0	Record Mixer Enable 0=RECMIX is powered down 1=RECMIX is powered up
	2	MONOMIX	0	Mono mixer enable 0=MONOMIX is powered down 1=MONOMIX is powered up
	1	RIGHTMIX	0	Right mixer enable 0=RIGHTMIX is powered down 1=RIGHTMIX is powered up
	0	LEFTMIX	0	Left mixer enable 0=LEFTMIX is powered down 1=LEFTMIX is powered up

Table 69 Power Management

SAVING POWER AT LOW SUPPLY VOLTAGES

The analogue supplies to the WM8753L can run from 1.8V to 3.6V. By default, all analogue circuitry on the device is optimized to run at 3.3V. This set-up is also good for all other supply voltages down to 1.8V. However, at lower voltages, it is possible to save power by reducing the internal bias currents used in the analogue circuitry. This is controlled as shown below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 (12h) Additional Control	7:6	VSEL [1:0]	11	Analogue Bias optimization 00: Lowest bias current, optimized for AVDD=1.8V 01: Low bias current, optimized for AVDD=2.5V 1X: Default bias current, optimized for AVDD=3.3V

SAVING POWER BY REDUCING OVERSAMPLING RATE

The default mode of operation of the ADC and DAC digital filters is in 64x oversampling mode. Under the control of ADCOSR and DACOSR the oversampling rate may be doubled. 64x oversampling results in a slight decrease in noise performance compared to 128x but lowers the power consumption of the device.

Important: ADC 64x mode is not available in USB mode (USB = 1). In USB mode ADCOSR must be set to '0'.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) Sample Rate Control (2)	2	VXDACOSR	1	Voice DAC oversample rate select 1 = 64x (lowest power) 0 = 128x (best SNR)
	1	ADCOSR	1	ADC oversample rate select 1 = 64x (lowest power) 0 = 128x (best SNR)
	0	DACOSR	1	DAC oversample rate select 1 = 64x (lowest power) 0 = 128x (best SNR)

Table 70 ADC and DAC Oversampling Rate Selection

SAVING POWER BY REDUCING BIAS CURRENTS

There are various biasing options within the WM8753L for increasing or reducing the bias current that is used by sections of the chip. The control of these is via the register bits MBIASBOOST, VDACBIASX0P5, MICBIASBST, BUFBIAS, IPBIASX0P5, ADCBIAS, OPBIASX0P5 and DMBIASX0P5 as shown in Figure 31. The performance of the chip may vary when the bias currents are changed from the default.

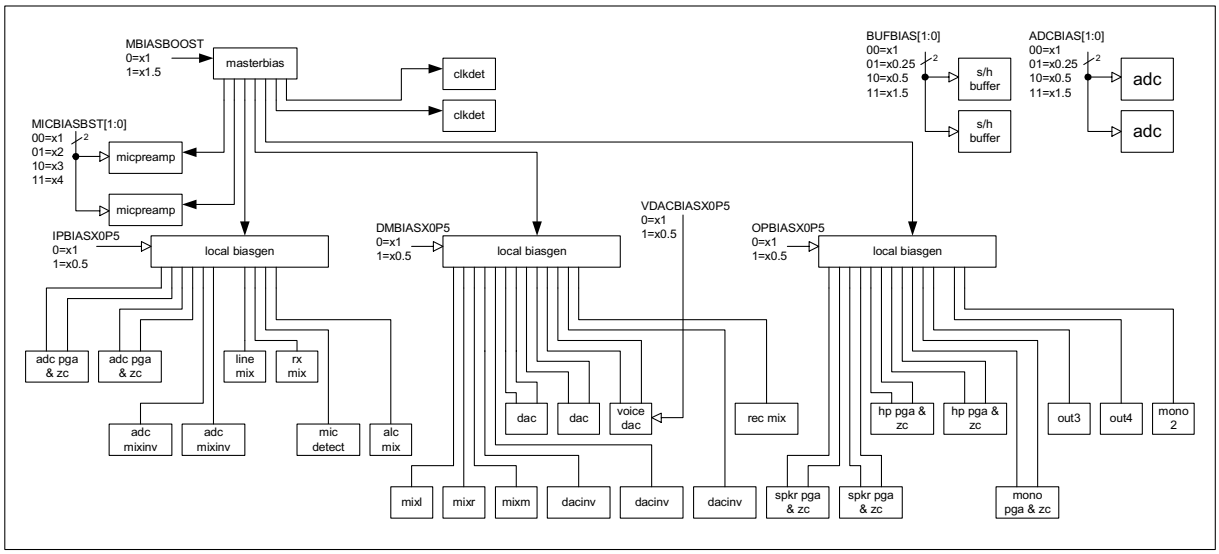


Figure 31 Bias Current Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R61 (3Dh) Bias control	8	VDACBIASX0P5	0	Voice DAC bias current reduce: 0 = 1x bias 1 = 0.5x bias (reduced power)
	7	MBIASBOOST	0	Master bias current boost 0 = 1x bias 1 = 1.5x bias (increased power)
	[6:5]	MICBIASBST [1:0]	00	Microphone preamplifier current boost: 00 = 1x bias 01 = 2x bias 10 = 3x bias 11 = 4x bias
	[4:3]	BUFBIAS[1:0]	00	ADC sample and hold buffer bias control: 00 = 1x bias 01 = 0.25x bias (lowest power) 10 = 0.5x bias (reduced power) 11 = 1.5x bias (increased power)
	2	IPBIASX0P5	0	ADC volume control (PGA) and ADCINV bias reduce: 0 = 1x bias 1 = 0.5x bias (reduced power)
	[1:0]	ADCBIAS[1:0]	00	ADC bias current reduce: 00 = 1x bias 01 = 0.25x bias (lowest power) 10 = 0.5x bias (reduced power) 11 = 1.5x bias (increased power)

Table 71 Bias Control Bits

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R63 (3Fh) Additional control	1	OPBIASX0P5	0	Analogue Output bias current control: 0 = 1x bias 1 = 0.5x bias (reduced power)
	0	DMBIAS0P5	0	DAC and Mixer bias current control: 0 = 1x bias 1 = 0.5x bias (reduced power)

Table 72 Additional Control Register – Bias Control Bits

REGISTER MAP

REGISTER	ADDRESS (Bit 15:9)	REMARKS	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R1 (01h)	0000001	DAC Control	0	0	DACINV	DMONOMIX[1:0]		DACMU	DEEMPH[1:0]		0	000001000
R2 (02h)	0000010	ADC Control	DATSEL[1:0]		ADCPOL[1:0]		VXFILT	HPMODE[1:0]		HPOR	ADCHPD	000000000
R3 (03h)	0000011	PCM Audio Interface	ADCDOP	VXCLKIN	PMS	MONO	PLRP	PWL[1:0]		PFORMAT[1:0]		000001010
R4 (04h)	0000100	Hi-Fi Audio Interface	0	BCLKINV	MS	LRSWAP	LRP	WL[1:0]		FORMAT[1:0]		000001010
R5 (05h)	0000101	Interface Control	0	VXCLKTRI	BCLKTRI	VXDTRI	ADCDTRI	IFMODE[1:0]		VXFSOE	LRCOE	000110011
R6 (06h)	0000110	Sample Rate Ctrl (1)	SRMODE	PSR	0	SR[4:0]					USB	000000000
R7 (07h)	0000111	Sample Rate Ctrl (2)	PBMODE[2:0]			BMODE[2:0]			VXDOSR	ADCOSR	DACOSR	000000111
R8 (08h)	0001000	Left DAC volume	LDVU	LDACVOL[7:0]								011111111
R9 (09h)	0001001	Right DAC volume	RDVU	RDACVOL[7:0]								011111111
R10 (0Ah)	0001010	Bass control	0	BB	BC[2:0]			BASS[3:0]				000001111
R11 (0Bh)	0001011	Treble control	0	0	TC	0	0	TRBL[3:0]				000001111
R12 (0Ch)	0001100	ALC1	ALCSEL[1:0]		MAXGAIN[2:0]			ALCL[3:0]				001111011
R13 (0Dh)	0001101	ALC2	ALCZC	ALCSR[3:0]				HLD[3:0]				000000000
R14 (0Eh)	0001110	ALC3	0	DCY[3:0]				ATK[3:0]				000110010
R15 (0Fh)	0001111	Noise Gate	0	NGTH[4:0]					0	NGG	NGAT	000000000
R16 (10h)	0010000	Left ADC volume	LAVU	LADCVOL[7:0]								011000011
R17 (11h)	0010001	Right ADC volume	RAVU	RADCVOL[7:0]								011000011
R18 (12h)	0010010	Additional control	0	VSEL[1:0]		0	0	0	ADCDIV2	DACDIV2	TOEN	011000000
R19 (13h)	0010011	3D Control	0	MODE3D	3DUC	3DLC	3DDEPTH[3:0]				3DEN	000000000
R20 (14h)	0010100	Pwr Mgmt (1)	VMIDSEL[1:0]		VREF	MICB	VDAC	DACL	DACR	0	DIGENB	000000000
R21 (15h)	0010101	Pwr Mgmt (2)	MICAMP1EN	MICAMP2E	ALCMIX	PGAL	PGAR	ADCL	ADCR	RXMIX	LINEMIX	000000000
R22 (16h)	0010110	Pwr Mgmt (3)	LOUT1	ROUT1	LOUT2	ROUT2	OUT3	OUT4	MONO1	MONO2	0	000000000
R23 (17h)	0010111	Pwr Mgmt (4)	0	0	0	0	0	RECMIX	MONOMIX	RIGHTMIX	LEFTMIX	000000000
R24 (18h)	0011000	ID register	0	0	0	0	RDDAT	READSEL[2:0]			READEN	000000000
R25 (19h)	0011001	Interupt Polarity	0	TSDIPOL	HPSW IPOL	GPIO5 IPOL	GPIO4 IPOL	GPIO3 IPOL	0	MICDET IPOL	MICSHT IPOL	000000000
R26 (1Ah)	0011010	Interupt Enable	0	TSDIEN	HPSWIEN	GPIO5 IEN	GPIO4 IEN	GPIO3 IEN	0	MICDET IEN	MICSHT IEN	000000000
R27 (1Bh)	0011011	GPIO Control (1)	INTCON[1:0]		0	0	GPIO5M[1:0]		GPIO4M[2:0]			000000000
R28 (1Ch)	0011100	GPIO Control (2)	GPIO3M[2:0]			GP2M[2:0]			GP1M[2:0]			000000000
R31 (1Fh)	0011111	Reset	writing 000000000 to this register resets all registers to their default state									not reset
R32 (20h)	0100000	Record Mix (1)	0	RSEL	RRECVOL[2:0]			LSEL	LRECVOL[2:0]			001010101
R33 (21h)	0100001	Record Mix (2)	0	0	0	0	0	MSEL	MRECVOL[2:0]			000000101
R34 (22h)	0100010	Left out Mix (1)	LD2LO	LM2LO	LM2LOVOL[2:0]			0	0	0	0	001010000
R35 (23h)	0100011	Left out Mix (2)	VXD2LO	ST2LO	ST2LOVOL[2:0]			0	VXD2LOVOL[2:0]			001010101
R36 (24h)	0100100	Right out Mix (1)	RD2RO	RM2RO	RM2ROVOL[2:0]			0	0	0	0	001010000
R37 (25h)	0100101	Right out Mix (2)	VXD2RO	ST2RO	ST2ROVOL[2:0]			0	VXD2ROVOL[2:0]			001010101
R38 (26h)	0100110	Mono out Mix (1)	LD2MO	MM2MO	MM2MOVOL[2:0]			0	0	0	0	001010000
R39 (27h)	0100111	Mono out Mix (2)	RD2MO	ST2MO	ST2MOVOL[2:0]			VXD2MO	VXD2MOVOL[2:0]			001010101
R40 (28h)	0101000	LOUT1 volume	LO1VU	LO1ZC	LOUT1VOL[6:0]							001111001
R41 (29h)	0101001	ROUT1 volume	RO1VU	RO1ZC	ROUT1VOL[6:0]							001111001
R42 (2Ah)	0101010	LOUT2 volume	LO2VU	LO2ZC	LOUT2VOL[6:0]							001111001
R43 (2Bh)	0101011	ROUT2 volume	RO2VU	RO2ZC	ROUT2VOL[6:0]							001111001
R44 (2Ch)	0101100	MONOOUT volume	0	MOZC	MONO1VOL[6:0]							001111001
R45 (2Dh)	0101101	Output Control	MONO2SW[1:0]		HPSWEN	HPSWPO	TSDEN	VROI	ROUT2IN	OUT3SW[1:0]		000000000

R46 (2Eh)	0101110	ADC input mode	0	0	0	MONOMIX[1:0]		RADCSEL[1:0]		LADCSEL[1:0]						000000000
R47 (2Fh)	0101111	Input Control (1)	MIC2BOOST[1:0]		MIC1BOOST[1:0]		LMSEL[1:0]		MM	RM	LM					000000000
R48 (30h)	0110000	Input Control (2)	0	RXMSEL[1:0]		MICMUX[1:0]		LINEALC	MIC2ALC	MIC1ALC	RXALC					000000000
R49 (31h)	0110001	Left Input volume	LIVU	LINMUTE	LIZC	LINVOL[5:0]										010010111
R50 (32h)	0110010	Right Input volume	RIVU	RINMUTE	RIZC	RINVOL[5:0]										010010111
R51 (33h)	0110011	Mic Bias comp control	MBVSEL	MICSEL[1:0]		MBSCTHRESH[1:0]		MBTHRESH[2:0]			MBCEN					000000000
R52 (34h)	0110100	Clock Control	PCMDIV[2:0]			SLWCLK	MCLK SEL	PCM CLKSEL	CLKEQ	GP1CLK1SEL	GP2CLK2SEL					000000100
R53 (35h)	0110101	PLL1 Control (1)	0	0	0	CLK1SEL	CLK1 DIV2	MCLK1 DIV2	PLL1 DIV2	PLL1RB	PLL1EN					000000000
R54 (36h)	0110110	PLL1 Control (2)	PLL1N[3:0]				0	PLL1K [21:18]								010000011
R55 (37h)	0110111	PLL1 Control (3)	PLL1K [17:9]													000100100
R56 (38h)	0111000	PLL1 Control (4)	PLL1K [8:0]													110111010
R57 (39h)	0111001	PLL2 Control (1)	0	0	0	CLK2SEL	CLK2 DIV2	MCLK2 DIV2	PLL2 DIV2	PLL2RB	PLL2EN					000000000
R58 (3Ah)	0111010	PLL2 Control (2)	PLL2N[3:0]				0	PLL2K [21:18]								010000011
R59 (3Bh)	0111011	PLL2 Control (3)	PLL2K [17:9]													000100100
R60 (3Ch)	0111100	PLL2 Control (4)	PLL2K [8:0]													110111010
R61 (3Dh)	0111101	Bias control	VDACBIAS X0P5	MBIAS BOOST	MICBIASBOOST[1:0]		BUFBIAS[1:0]		IPBIAS X0P5	ADCBIAS[1:0]						000000000
R63 (3Fh)	0111111	Additional Control	OUT4SW[1:0]		TSADEN	0	0	0	0	OPBIAS X0P5	DMBIAS XOP5					000000000

Table 73 Complete Register Map

DIGITAL FILTER CHARACTERISTICS

The ADC and DAC employ different digital filters. There are 4 types of digital filter, called Type 0, 1, 2 and 3. The performance of Types 0 and 1 is listed in the table below, the responses of all filters is shown in the proceeding pages.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter Type 0 (USB Mode, 250fs operation)					
Passband	+/- 0.05dB	0		0.416fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.05	dB
Stopband		0.584fs			
Stopband Attenuation	f > 0.584fs	-60			dB
Group Delay			17/fs		
ADC Filter Type 1 (USB mode, 272fs or Normal mode operation)					
Passband	+/- 0.05dB	0		0.4535fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.05	dB
Stopband		0.5465fs			
Stopband Attenuation	f > 0.5465fs	-60			dB
Group Delay			25/fs		
ADC High Pass Filter					
High Pass Filter Corner Frequency	-3dB		3.7		Hz
	-0.5dB		10.4		
	-0.1dB		21.6		
DAC Filter Type 0 (USB mode, 250fs operation)					
Passband	+/- 0.03dB	0		0.416fs	
	-6dB		0.5fs		
Passband Ripple				+/-0.03	dB
Stopband		0.584fs			
Stopband Attenuation	f > 0.584fs	-50			dB
Group Delay			15/fs		
DAC Filter Type 1 (USB mode, 272fs or Normal mode operation)					
Passband	+/- 0.03dB	0		0.4535fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.03	dB
Stopband		0.5465fs			
Stopband Attenuation	f > 0.5465fs	-50			dB
Group Delay			18/fs		

Table 74 HiFi Digital Filter Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voice ADC Filter					
Passband	+/- 0.3dB	0		0.414fs	
	-14dB		0.5fs		
Passband Ripple				+/- 0.3	dB
Stopband		0.53fs			
Stopband Attenuation	f > 0.53fs	-30			dB
Group Delay			7/fs		
Voice DAC Filter					
Passband	+/- 0.3dB	0		0.414fs	
	-14dB		0.5fs		
Passband Ripple				+/-0.3	dB
Stopband		0.53fs			
Stopband Attenuation	f > 0.53fs	-30			dB
Group Delay			7/fs		

Table 75 Voice CODEC Digital Filter Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC High Pass Filter (HPMODE[1:0] = 00) (256fs, fs=48kHz)					
High Pass Filter Corner Frequency	-3dB		3.7		Hz
	-0.5dB		10.4		
	-0.1dB		21.6		
ADC High Pass Filter (HPMODE[1:0] = 01) (256fs, fs=16kHz)					
High Pass Filter Corner Frequency	-3dB		82		Hz
	-0.5dB		203		
	-0.1dB		341		
ADC High Pass Filter (HPMODE[1:0] = 10) (256fs, fs=8kHz)					
High Pass Filter Corner Frequency	-3dB		82		Hz
	-0.5dB		185		
	-0.1dB		272		
ADC High Pass Filter (HPMODE[1:0] = 11) (256fs, fs=8kHz)					
High Pass Filter Corner Frequency	-3dB		170		Hz
	-0.5dB		321		
	-0.1dB		415		

Table 76 ADC Highpass Filter Characteristics

TERMINOLOGY

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

DAC FILTER RESPONSES

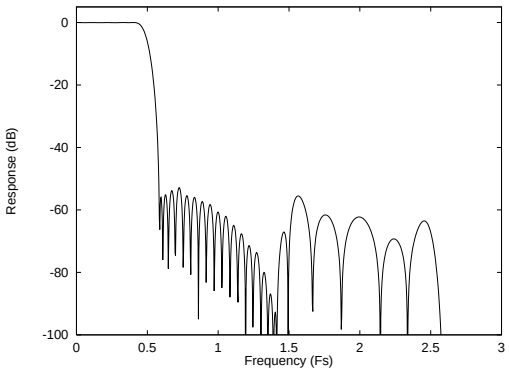


Figure 32 DAC Digital Filter Frequency Response – Type 0

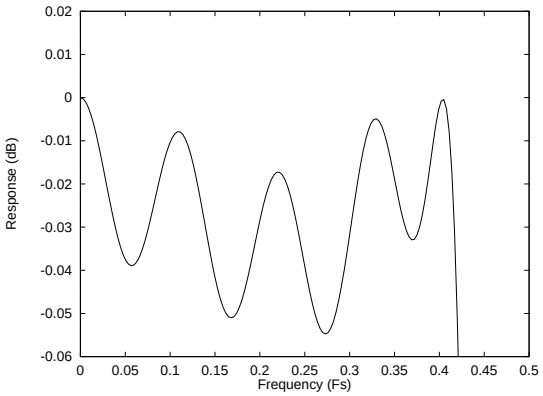


Figure 33 DAC Digital Filter Ripple – Type 0

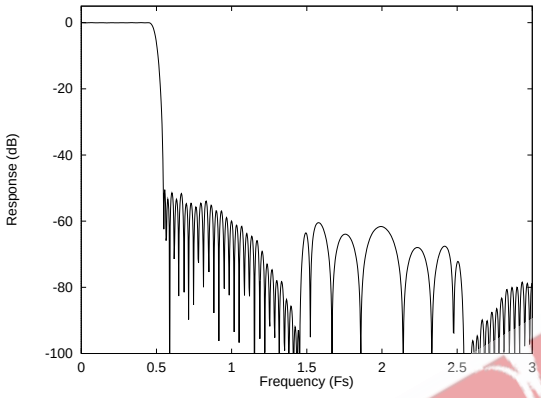


Figure 34 DAC Digital Filter Frequency Response – Type 1

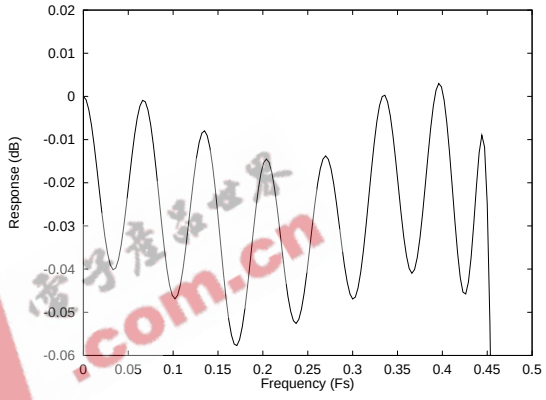


Figure 35 DAC Digital Filter Ripple – Type 1

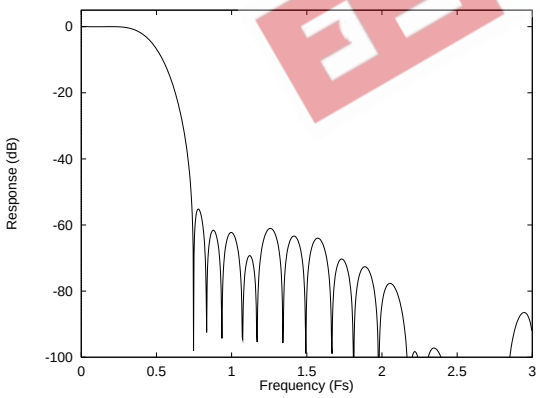


Figure 36 DAC Digital Filter Frequency Response – Type 2

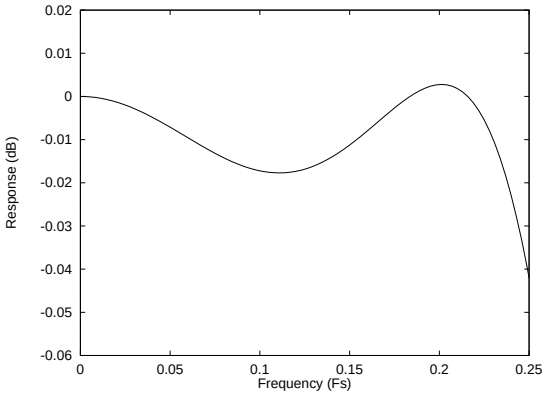


Figure 37 DAC Digital Filter Ripple – Type 2

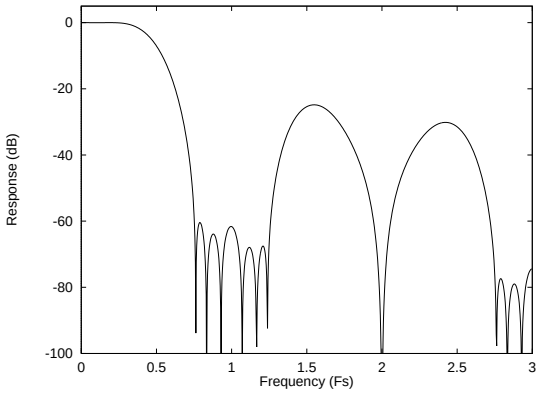


Figure 38 DAC Digital Filter Frequency Response – Type 3

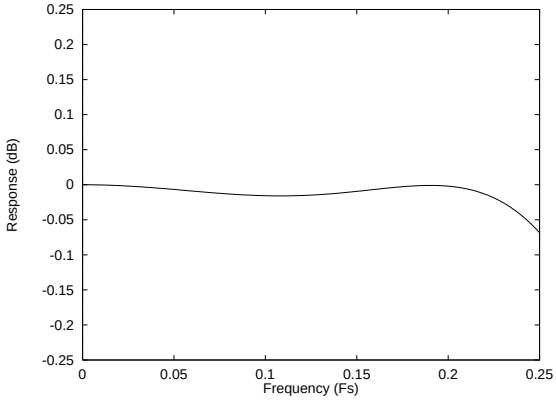


Figure 39 DAC Digital Filter Ripple – Type 3

ADC FILTER RESPONSES

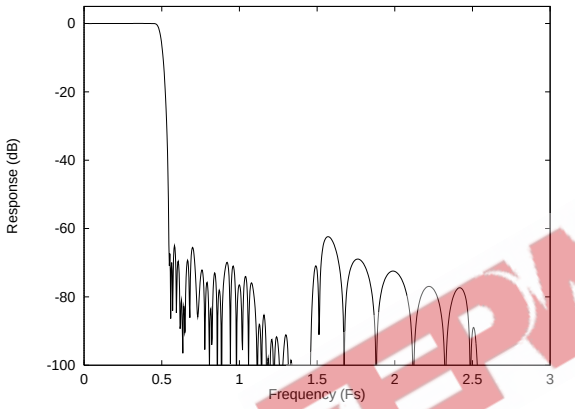


Figure 40 ADC Digital Filter Frequency Response – Type 0

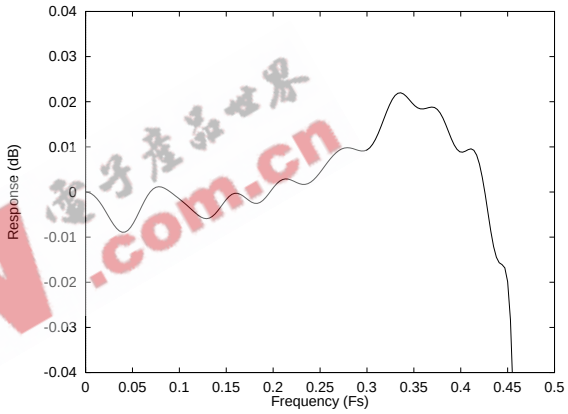


Figure 41 ADC Digital Filter Ripple – Type 0

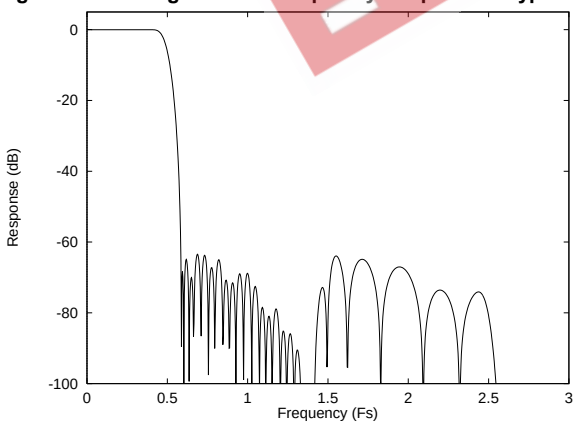


Figure 42 ADC Digital Filter Frequency Response – Type 1

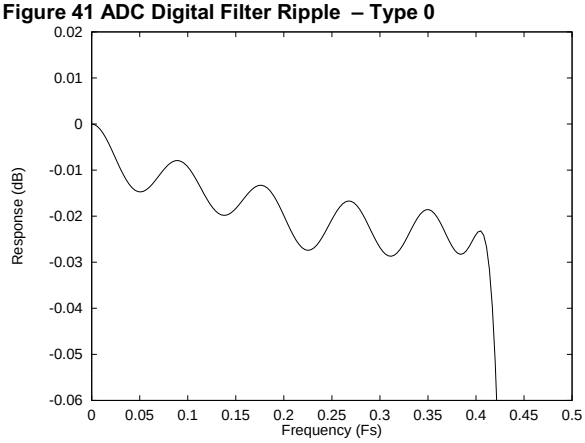


Figure 43 ADC Digital Filter Ripple – Type 1

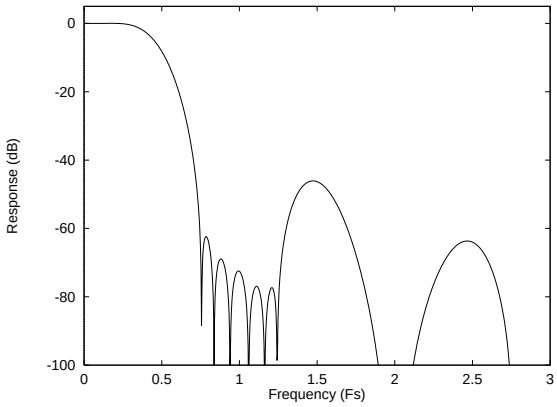


Figure 44 ADC Digital Filter Frequency Response – Type 2

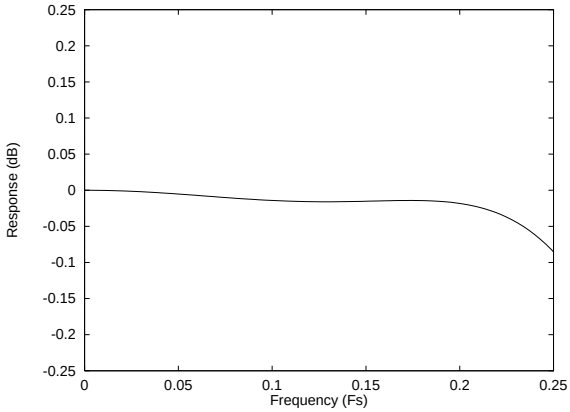


Figure 45 ADC Digital Filter Ripple – Type 2

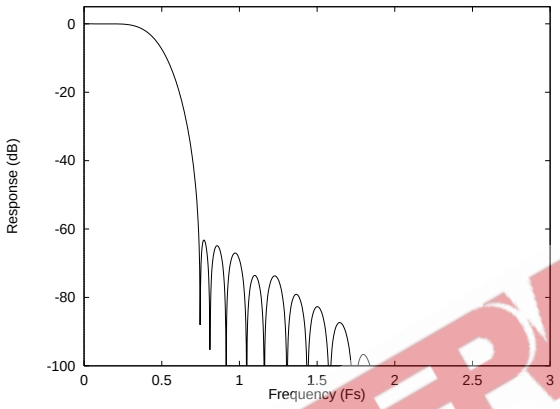


Figure 46 ADC Digital Filter Frequency Response – Type 3

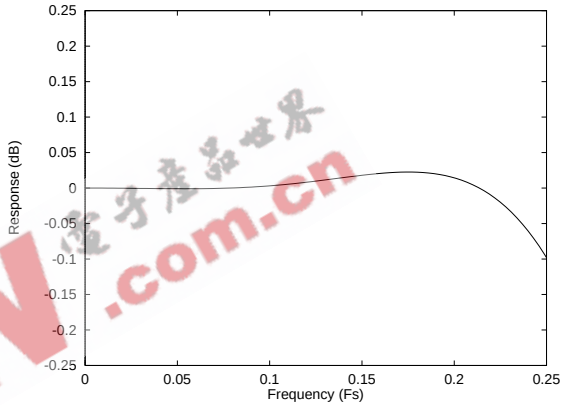


Figure 47 ADC Digital Filter Ripple – Type 3

VOICE FILTER RESPONSES

VOICE DAC FILTER RESPONSES

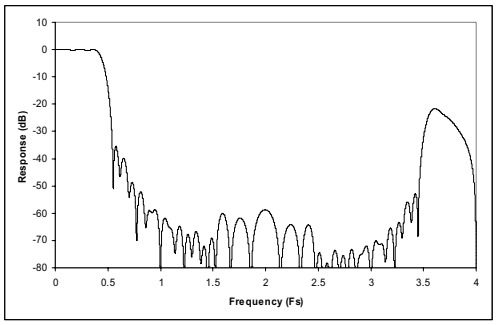


Figure 48 Voice DAC Digital Filter Frequency Response

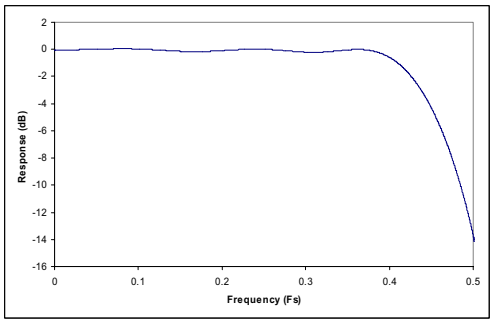


Figure 49 Voice DAC Digital Filter Frequency Response

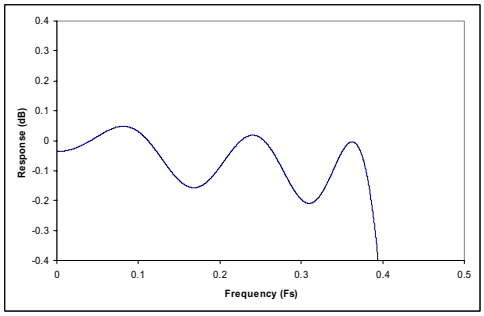


Figure 50 Voice DAC Digital Filter Ripple

VOICE ADC FILTER RESPONSES

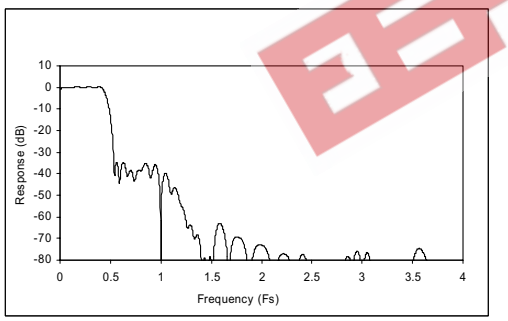


Figure 51 Voice ADC Digital Filter Frequency Response

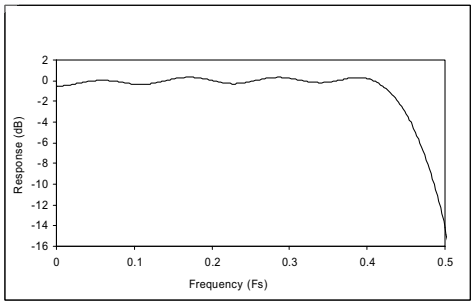


Figure 52 Voice ADC Digital Filter Frequency Response

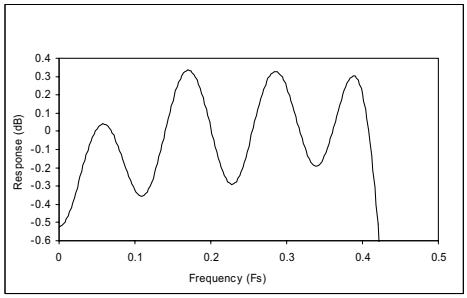


Figure 53 Voice ADC Digital Filter Ripple

DE-EMPHASIS FILTER RESPONSES

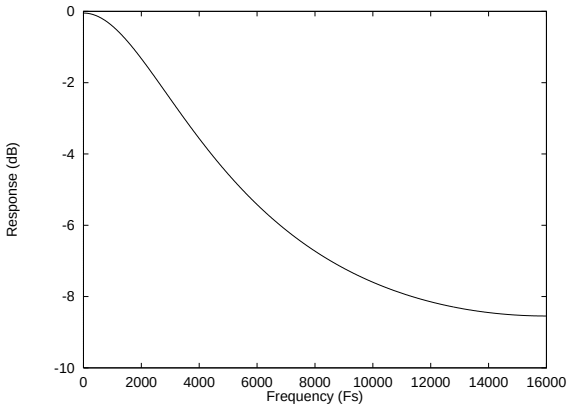


Figure 54 De-emphasis Frequency Response (32kHz)

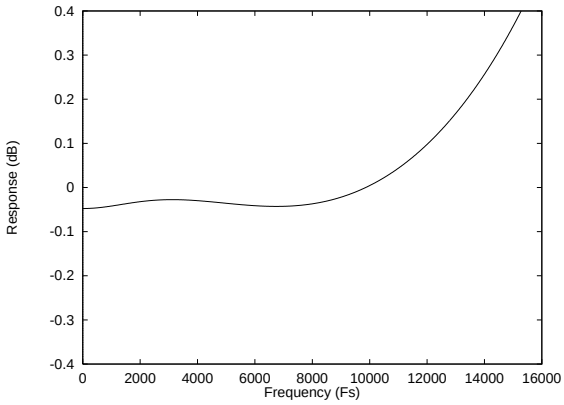


Figure 55 De-emphasis Error (32kHz)

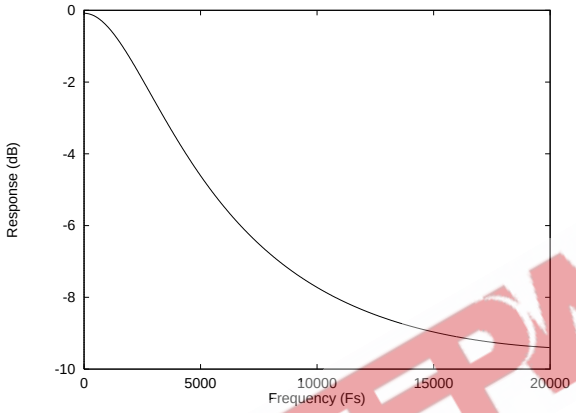


Figure 56 De-emphasis Frequency Response (44.1kHz)

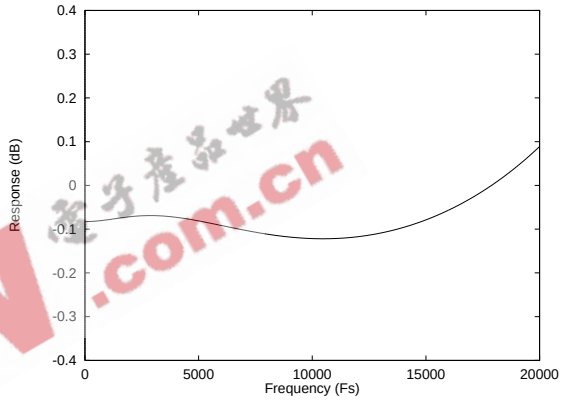


Figure 57 De-emphasis Error (44.1kHz)

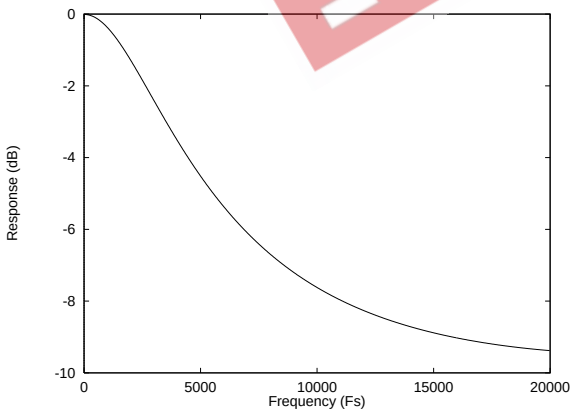


Figure 58 De-emphasis Frequency Response (48kHz)

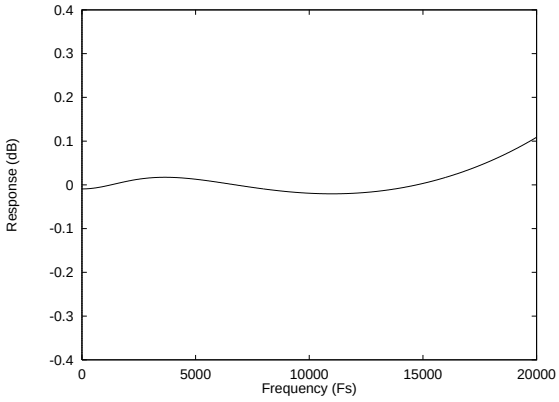


Figure 59 De-emphasis Error (48kHz)

HIGHPASS FILTER

The WM8753 has a selectable digital highpass filter in the ADC filter path to remove DC offsets.

HPMODE[1:0] = 00

The filter response is characterised by the following polynomial:

$$H(z) = \frac{1 - z^{-1}}{1 - 0.9995z^{-1}}$$

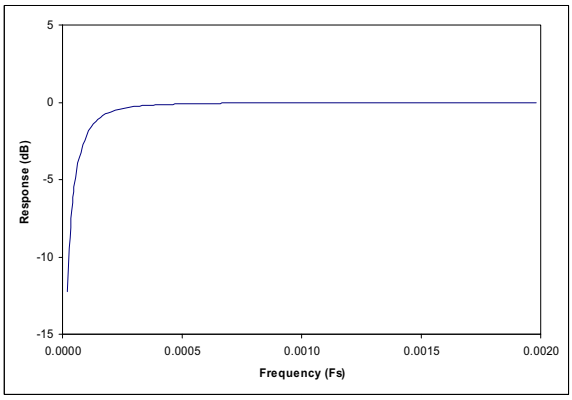


Figure 60 ADC Highpass Filter Response, HPMODE[1:0] = 00

HPMODE[1:0] = 01

The filter response is characterised by the following polynomial:

$$H(z) = \frac{1 - z^{-1}}{1 - 0.96875z^{-1}}$$

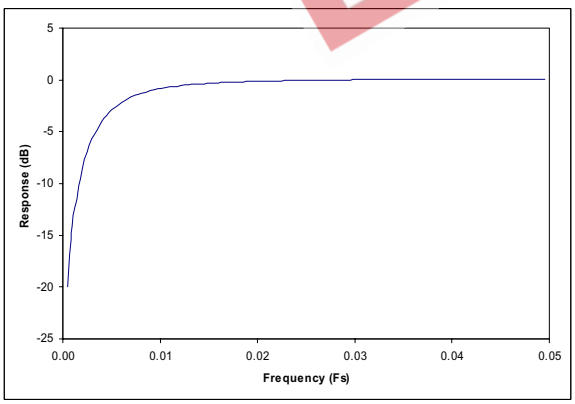


Figure 61 ADC Highpass Filter Response, HPMODE[1:0] = 01

HPMODE[1:0] = 10

The filter response is characterised by the following polynomial:

$$H(z) = \frac{1 - z^{-1}}{1 - 0.9375z^{-1}}$$

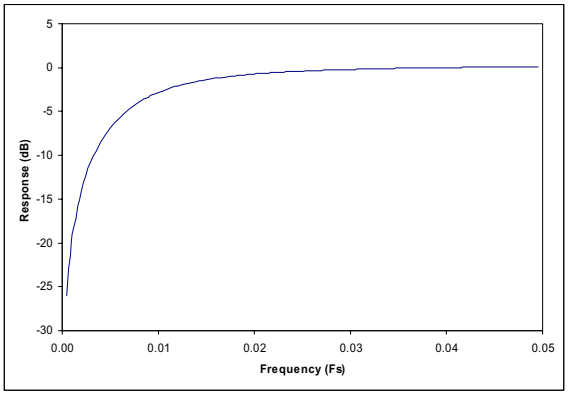


Figure 62 ADC Highpass Filter Response, HPMODE[1:0] = 10

HPMODE[1:0] = 11

The filter response is characterised by the following polynomial:

$$H(z) = \frac{1 - z^{-1}}{1 - 0.875z^{-1}}$$

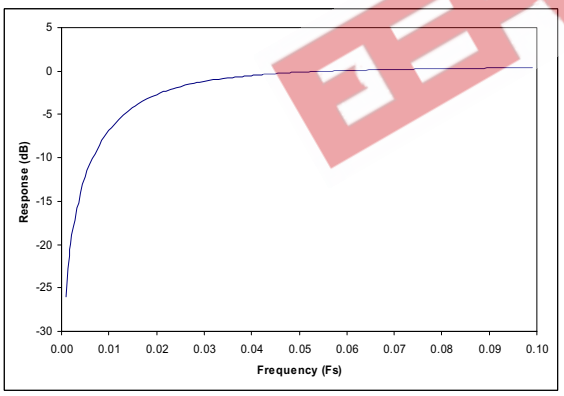


Figure 63 ADC Highpass Filter Response, HPMODE[1:0] = 11

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

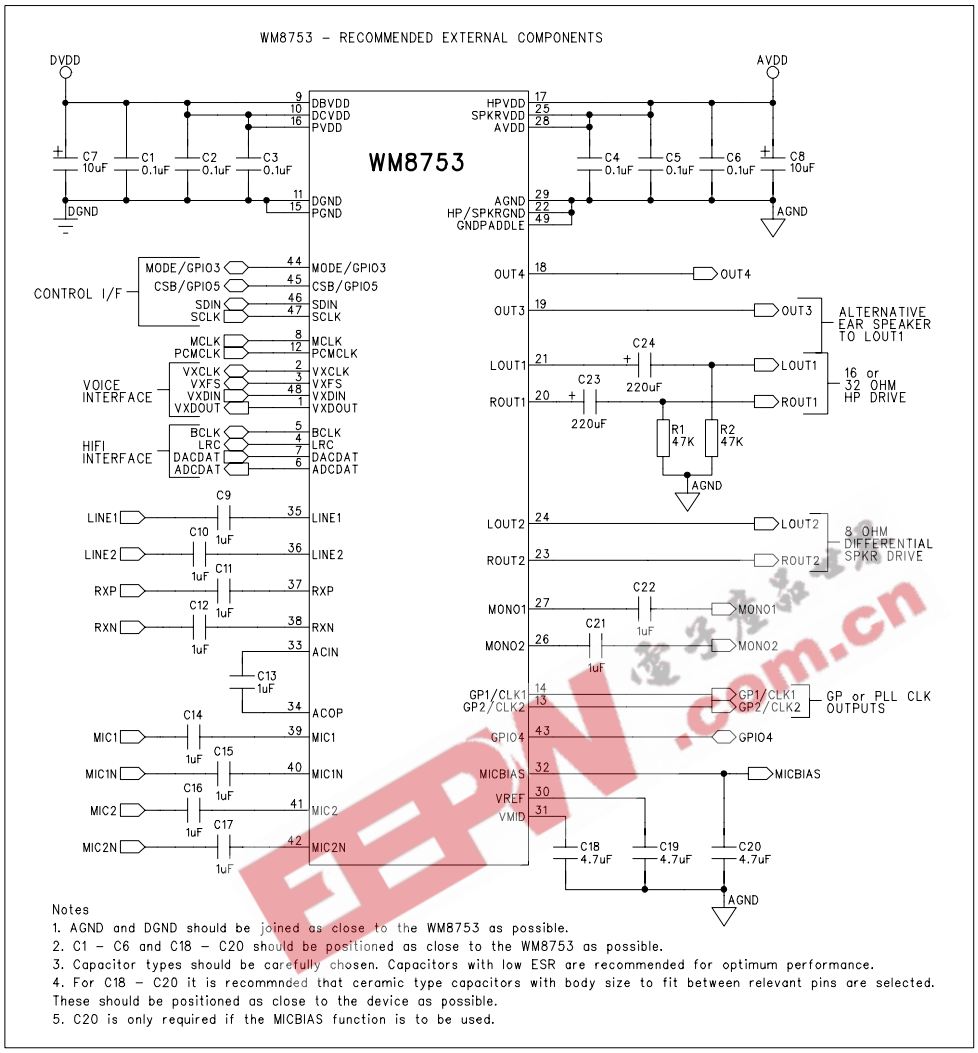


Figure 64 Recommended External Components Diagram

MINIMISING POP NOISE AT THE ANALOGUE OUTPUTS

To minimise any pop or click noise when the system is powered up or down, the following procedures are recommended.

POWER SUPPLIES

The ideal way to apply power to the WM8753 is to all supplies at the same time.

This is not always possible in many designs due to supplies being sourced from different voltage regulators or direct from batteries. In these situations, it is recommended that supplies are applied in the following order.

1. DCVDD, DBVDD and PVDD (if not at the same time, any order may be used)
2. AVDD
3. HPVDD and SPKRVDD (if not at the same time, any order may be used)

Supplies may be removed in any order. However, it is recommended that HPVDD and SPKRVDD supplies be removed last.

POWER UP

Switch on power supplies. By default the WM8753L is in Standby Mode, the DAC is digitally muted and the Audio Interface and Outputs are all OFF

Enable Vmid and VREF. Allow VREF to settle. The settling time depends on the value of the capacitor connected at VMID, and the size of the resistors selected using VMIDSEL (τ = RC).

Enable DACs, etc. as required.

Enable outputs as required.

Set DACMU = 0 to un-mute the audio DACs.

POWER DOWN (MINIMUM NOISE)

Set DACMU = 1 to mute the audio DACs.

Disable all Outputs.

Disable VREF and VMIDSEL.

Switch off the power supplies

POWER DOWN (QUICKEST MIDRAIL DISCHARGE)

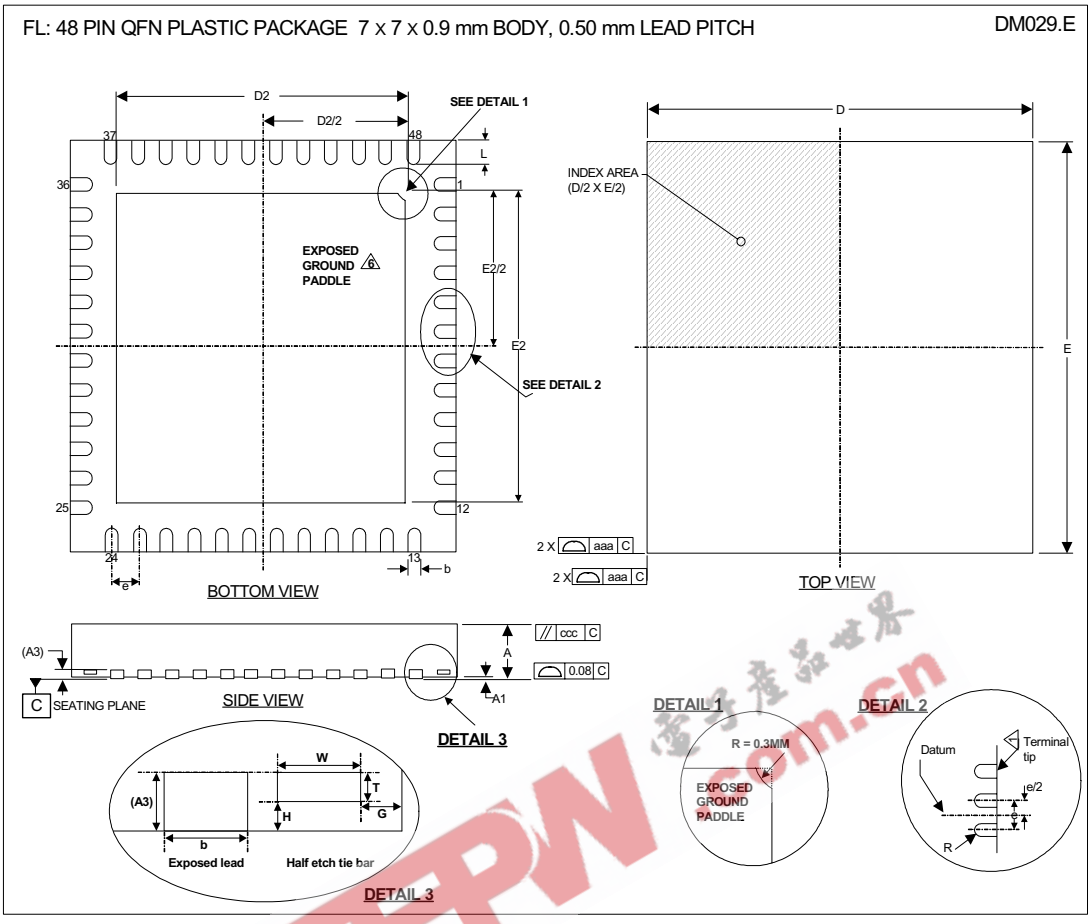
Set DACMU = 1 to mute the audio DACs.

Disable VREF and VMIDSEL.

Switch off the power supplies.

A choice of two power down sequences have been recommended. The first is completely noise free with the disadvantage that the mid-rail voltage can take some time to discharge due to the large amount of capacitance attached to the outputs. The second offers a quick discharge of the output capacitors but as the outputs have not been powered down it does allow for the small possibility that noise may be heard during power down.

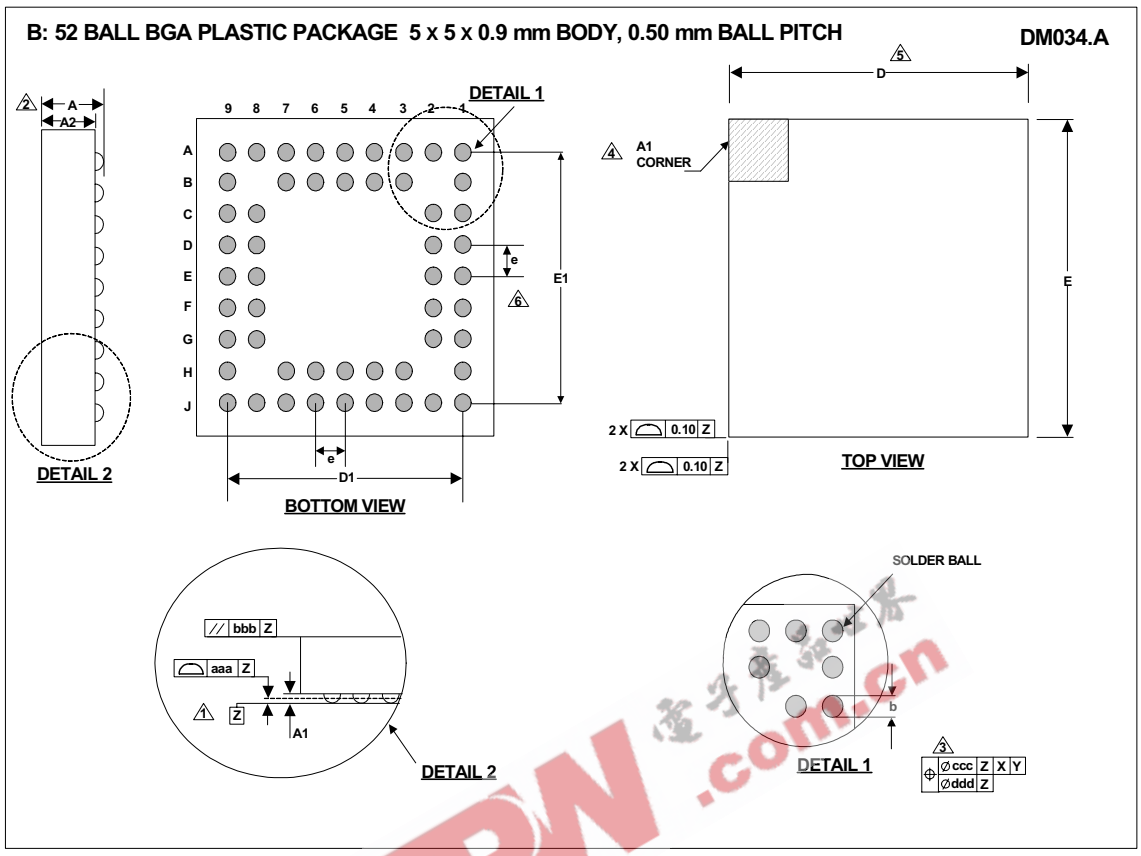
PACKAGE DIAGRAM – 48-LEAD QFN



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0	0.02	0.05	
A3		0.20 REF		
b	0.18	0.25	0.30	1
D		7.00 BSC		
D2	5.00	5.15	5.25	
E		7.00 BSC		
E2	5.00	5.15	5.25	
e		0.5 BSC		
G		0.213		
H		0.1		
L	0.30	0.4	0.50	
T		0.1		
W		0.2		
Tolerances of Form and Position				
aaa	0.15			
bbb	0.10			
ccc	0.10			
REF	JEDEC, MO-220, VARIATION VKKD-2			

NOTES:
1. DIMENSION b APPLIED TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.
2. ALL DIMENSIONS ARE IN MILLIMETRES
3. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-002.
4. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
5. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
6. REFER TO APPLICATION NOTE WAN_0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.

PACKAGE DIAGRAM - 52-BALL BGA



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.95	1.11	1.27	
A1	0.15	0.21	0.27	
A2	0.80	0.90	1.00	
b	0.25	0.30	0.35	
D		5.00 BSC		
D1		4.00 BSC		
E		5.00 BSC		
E1		4.00 BSC		
e		0.50 BSC		6
Tolerances of Form and Position				
aaa		0.80		
bbb		0.10		
ccc		0.15		
ddd		0.05		

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1'.
3. DIMENSION 'b' IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -Z-.
4. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
5. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
6. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
7. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.

IMPORTANT NOTICE

Wolfson Microelectronics plc (WM) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current. All products are sold subject to the WM terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

WM warrants performance of its products to the specifications applicable at the time of sale in accordance with WM's standard warranty. Testing and other quality control techniques are utilised to the extent WM deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

In order to minimise risks associated with customer applications, adequate design and operating safeguards must be used by the customer to minimise inherent or procedural hazards. Wolfson products are not authorised for use as critical components in life support devices or systems without the express written approval of an officer of the company. Life support devices or systems are devices or systems that are intended for surgical implant into the body, or support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided, can be reasonably expected to result in a significant injury to the user. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

WM assumes no liability for applications assistance or customer product design. WM does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of WM covering or relating to any combination, machine, or process in which such products or services might be or are used. WM's publication of information regarding any third party's products or services does not constitute WM's approval, license, warranty or endorsement thereof.

Reproduction of information from the WM web site or datasheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. Representation or reproduction of this information with alteration voids all warranties provided for an associated WM product or service, is an unfair and deceptive business practice, and WM is not responsible nor liable for any such use.

Resale of WM's products or services with statements different from or beyond the parameters stated by WM for that product or service voids all express and any implied warranties for the associated WM product or service, is an unfair and deceptive business practice, and WM is not responsible nor liable for any such use.

ADDRESS:

Wolfson Microelectronics plc
Westfield House
26 Westfield Road
Edinburgh
EH11 2QB
United Kingdom

Tel :: +44 (0)131 272 7000
Fax :: +44 (0)131 272 7001
Email :: sales@wolfsonmicro.com