

## Stereo Audio CODEC

### DESCRIPTION

The WM8734 is a low power stereo CODEC ideal for MD, CD-RW machines and DAT recording applications.

Stereo line inputs are provided, along with a mute function and programmable line level volume control.

Stereo 24-bit multi-bit sigma delta ADCs and DACs are used with oversampling digital interpolation and decimation filters.

Digital audio input word lengths from 16-32 bits and sampling rates from 8kHz to 96kHz are supported.

Stereo audio line level outputs are provided along with anti-thump mute and power up/down circuitry.

The device is controlled via a 2 or 3 wire serial interface. The interface provides access to all features including level controls, mutes, de-emphasis and power management facilities. The device is available in 20-lead SSOP or 28-lead, 5x5mm QFN packages.

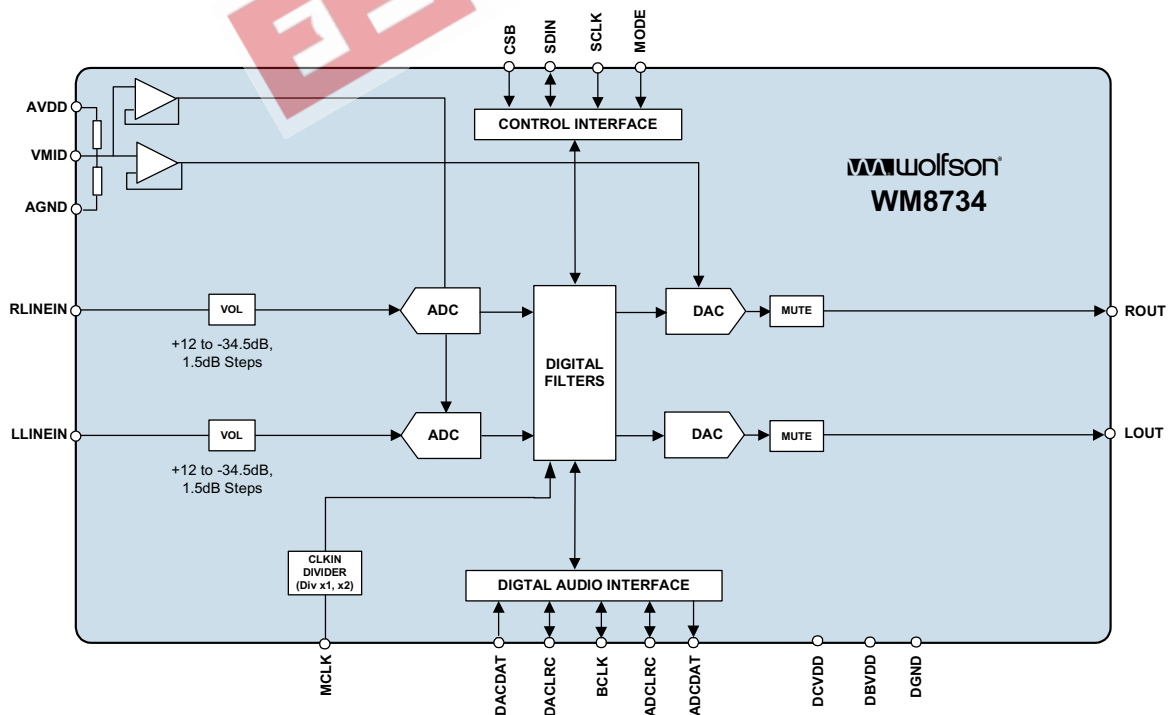
### FEATURES

- Audio Performance
  - 90dB SNR ('A' weighted @ 48kHz) ADC
  - 100dB SNR ('A' weighted @ 48kHz) DAC
  - 2.7 – 3.6V Digital Supply Operation
  - 2.7 – 3.6V Analogue Supply Operation
- ADC and DAC Sampling Frequency: 8kHz – 96kHz
- Selectable ADC High Pass Filter
- 2 or 3-Wire MPU Serial Control Interface
- Programmable Audio Data Interface Modes
  - I<sup>2</sup>S, Left, Right Justified or DSP
  - 16/20/24/32 bit Word Lengths
  - Master or Slave Clocking Mode
- Stereo Audio Inputs and Outputs
- 20-lead SSOP or 5x5mm QFN Package Options

### APPLICATIONS

- CD and Minidisc Recorder
- MP3 Player / Recorder

### BLOCK DIAGRAM



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## PIN CONFIGURATION – SSOP

|         |                          |     |    |                          |         |
|---------|--------------------------|-----|----|--------------------------|---------|
| DGND    | <input type="checkbox"/> | 1 ● | 20 | <input type="checkbox"/> | DCVDD   |
| DBVDD   | <input type="checkbox"/> | 2   | 19 | <input type="checkbox"/> | MCLK    |
| BCLK    | <input type="checkbox"/> | 3   | 18 | <input type="checkbox"/> | SCLK    |
| DACDAT  | <input type="checkbox"/> | 4   | 17 | <input type="checkbox"/> | SDIN    |
| DACLRRC | <input type="checkbox"/> | 5   | 16 | <input type="checkbox"/> | CSB     |
| ADCDAT  | <input type="checkbox"/> | 6   | 15 | <input type="checkbox"/> | MODE    |
| ADCLRRC | <input type="checkbox"/> | 7   | 14 | <input type="checkbox"/> | LLINEIN |
| LOUT    | <input type="checkbox"/> | 8   | 13 | <input type="checkbox"/> | RLINEIN |
| ROUT    | <input type="checkbox"/> | 9   | 12 | <input type="checkbox"/> | VMID    |
| AVDD    | <input type="checkbox"/> | 10  | 11 | <input type="checkbox"/> | AGND    |

## ORDERING INFORMATION - SSOP

| DEVICE       | TEMPERATURE RANGE | PACKAGE                                    | MOISTURE SENSITIVITY LEVEL | PEAK SOLDERING TEMPERATURE |
|--------------|-------------------|--|----------------------------|----------------------------|
| XWM8734EDS   | -25 to +85°C      | 20-lead SSOP<br>(Pb-free)                  | MSL1                       | 260°C                      |
| XWM8734EDS/R | -25 to +85°C      | 20-lead SSOP<br>(Pb-free<br>tape and reel) | MSL1                       | 260°C                      |

**Note:**

Reel quantity = 2,000

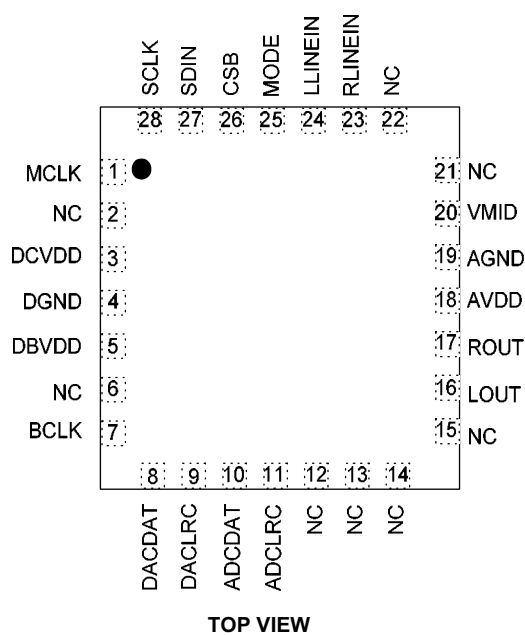
## PIN DESCRIPTION - SSOP

| PIN | NAME    | TYPE                 | DESCRIPTION   |
|-----|---------|----------------------|---|
| 1   | DGND    | Ground               | Digital GND   |
| 2   | DBVDD   | Supply               | Digital Buffers VDD   |
| 3   | BCLK    | Digital Input/Output | Digital Audio Bit Clock, Pull Down, (see Note 1)  |
| 4   | DACDAT  | Digital Input        | DAC Digital Audio Data Input  |
| 5   | DACLRC  | Digital Input/Output | DAC Sample Rate Left/Right Clock. Pull Down (see Note 1)  |
| 6   | ADCDAT  | Digital Output       | ADC Digital Audio Data Output   |
| 7   | ADCLRC  | Digital Input/Output | ADC Sample Rate Left/Right Clock, Pull Down (see Note 1)  |
| 8   | LOUT    | Analogue Output      | Left Channel Line Output  |
| 9   | ROUT    | Analogue Output      | Right Channel Line Output   |
| 10  | AVDD    | Supply               | Analogue VDD  |
| 11  | AGND    | Ground               | Analogue GND  |
| 12  | VMID    | Analogue Output      | Mid-rail reference decoupling point   |
| 13  | RLINEIN | Analogue Input       | Right Channel Line Input (AC coupled)   |
| 14  | LLINEIN | Analogue Input       | Left Channel Line Input (AC coupled)  |
| 15  | MODE    | Digital Input        | Control Interface Selection, Pull Up (see Note 1)   |
| 16  | CSB     | Digital Input        | 3-Wire MPU Chip Select / 2-Wire MPU interface address selection, active low, Pull up (see Note 1) |
| 17  | SDIN    | Digital Input/Output | 3-Wire MPU Data Input / 2-Wire MPU Data Input   |
| 18  | SCLK    | Digital Input        | 3-Wire MPU Clock Input / 2-Wire MPU Clock Input   |
| 19  | MCLK    | Digital Input        | Master Clock Input (MCLK)   |
| 20  | DCVDD   | Supply               | Digital Core VDD  |

**Note:**

1. Pull Up/Down only present when Control Register Interface ACTIVE = 0 to conserve power.

## PIN CONFIGURATION – QFN



## ORDERING INFORMATION - QFN

| DEVICE       | TEMPERATURE RANGE | PACKAGE  | MOISTURE SENSITIVITY LEVEL | PEAK SOLDERING TEMPERATURE |
|--------------|-------------------|--|----------------------------|----------------------------|
| WM8734SEFL   | -25 to +85°C      | 28-lead QFN<br>(5x5x0.9mm)<br>(Pb-free)                | MSL 1                      | 260°C                      |
| WM8734SEFL/R | -25 to +85°C      | 28-lead QFN<br>(5x5x0.9mm)<br>(Pb-free, tape and reel) | MSL 1                      | 260°C                      |

**Note:**

Reel quantity = 3,500

## PIN DESCRIPTION - QFN

| PIN | NAME    | TYPE                 | DESCRIPTION   |
|-----|---------|----------------------|---|
| 1   | MCLK    | Digital Input        | Master Clock Input (MCLK)   |
| 2   | NC      | Do Not Connect       | Test Pin, must be left unconnected  |
| 3   | DCVDD   | Supply               | Digital Core VDD  |
| 4   | DGND    | Ground               | Digital GND   |
| 5   | DBVDD   | Supply               | Digital Buffers VDD   |
| 6   | NC      | Do Not Connect       | Test Pin, must be left unconnected  |
| 7   | BCLK    | Digital Input/Output | Digital Audio Bit Clock, Pull Down, (see Note 1)  |
| 8   | DACDAT  | Digital Input        | DAC Digital Audio Data Input  |
| 9   | DACLRC  | Digital Input/Output | DAC Sample Rate Left/Right Clock. Pull Down (see Note 1)  |
| 10  | ADCDAT  | Digital Output       | ADC Digital Audio Data Output   |
| 11  | ADCLRC  | Digital Input/Output | ADC Sample Rate Left/Right Clock, Pull Down (see Note 1)  |
| 12  | NC      | Do Not Connect       | Test Pin, must be left unconnected  |
| 13  | NC      | Do Not Connect       | Test Pin, must be left unconnected  |
| 14  | NC      | Do Not Connect       | Test Pin, must be left unconnected  |
| 15  | NC      | Do Not Connect       | Test Pin, must be left unconnected  |
| 16  | LOUT    | Analogue Output      | Left Channel Line Output  |
| 17  | ROUT    | Analogue Output      | Right Channel Line Output   |
| 18  | AVDD    | Supply               | Analogue VDD  |
| 19  | AGND    | Ground               | Analogue GND  |
| 20  | VMID    | Analogue Output      | Mid-rail reference decoupling point   |
| 21  | NC      | Do Not Connect       | Test Pin, must be left unconnected  |
| 22  | NC      | Do Not Connect       | Test Pin, must be left unconnected  |
| 23  | RLINEIN | Analogue Input       | Right Channel Line Input (AC coupled)   |
| 24  | LLINEIN | Analogue Input       | Left Channel Line Input (AC coupled)  |
| 25  | MODE    | Digital Input        | Control Interface Selection, Pull Up (see Note 1)   |
| 26  | CSB     | Digital Input        | 3-Wire MPU Chip Select / 2-Wire MPU interface address selection, active low, Pull up (see Note 1) |
| 27  | SDIN    | Digital Input/Output | 3-Wire MPU Data Input / 2-Wire MPU Data Input   |
| 28  | SCLK    | Digital Input        | 3-Wire MPU Clock Input / 2-Wire MPU Clock Input   |

**Note:** It is recommended that the QFN ground paddle is connected to analogue ground on the application PCB.

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

| CONDITION                                   | MIN        | MAX        |
|---|------------|------------|
| Digital supply voltage                      | -0.3V      | +3.63V     |
| Analogue supply voltage                     | -0.3V      | +3.63V     |
| Voltage range digital inputs                | DGND -0.3V | DVDD +0.3V |
| Voltage range analogue inputs               | AGND -0.3V | AVDD +0.3V |
| Operating temperature range, T <sub>A</sub> | -25°C      | +85°C      |
| Storage temperature after soldering         | -65°C      | +150°C     |

### Notes:

- Analogue and digital grounds must always be within 0.3V of each other.
- The digital supply core voltage (DCVDD) must always be less than or equal to the analogue supply voltage (AVDD)

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER                     | SYMBOL         | TEST CONDITIONS              | MIN | TYP | MAX | UNIT |
|-------------------------------|----------------|------------------------------|-----|-----|-----|------|
| Digital supply range (Core)   | DCVDD          |                              | 2.7 |     | 3.6 | V    |
| Digital supply range (Buffer) | DBVDD          |                              | 2.7 |     | 3.6 | V    |
| Analogue supply range         | AVDD           |                              | 2.7 |     | 3.6 | V    |
| Ground                        | DGND, AGND     |                              |     | 0   |     | V    |
| Total analogue supply current | IAVDD          | DCVDD, DBVDD,<br>AVDD = 3.3V |     | 16  |     | mA   |
| Digital supply current        | IDCVDD, IDBVDD | DCVDD, DBVDD<br>AVDD = 3.3V  |     | 8   |     | mA   |
| Standby Current Consumption   |                |                              |     | 5   |     | uA   |

## ELECTRICAL CHARACTERISTICS

## Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, T<sub>A</sub> = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

| PARAMETER                                 | SYMBOL              | TEST CONDITIONS                                      | MIN         | TYP             | MAX          | UNIT             |
|---|---------------------|--|-------------|-----------------|--------------|------------------|
| <b>Digital Logic Levels (CMOS Levels)</b> |                     |  |             |                 |              |                  |
| Input LOW level                           | V <sub>IL</sub>     |  |             |                 | 0.3 x DBVDD  | V                |
| Input HIGH level                          | V <sub>IH</sub>     |  | 0.7 x DBVDD |                 |              | V                |
| Output LOW                                | V <sub>OL</sub>     |  |             |                 | 0.10 x DBVDD | V                |
| Output HIGH                               | V <sub>OH</sub>     |  | 0.9 x DBVDD |                 |              | V                |
| <b>Power On Reset Threshold (DCVDD)</b>   |                     |  |             |                 |              |                  |
| DCVDD Threshold On -> Off                 | V <sub>th</sub>     |  |             | 0.9             |              | V                |
| Hysteresis                                | V <sub>IH</sub>     |  |             | 0.3             |              | V                |
| DCVDD Threshold Off -> On                 | V <sub>OL</sub>     |  |             | 0.6             |              | V                |
| <b>Analogue Reference Levels</b>          |                     |  |             |                 |              |                  |
| Reference voltage                         | V <sub>VMID</sub>   |  |             | AVDD/2          |              | V                |
| Potential divider resistance              | R <sub>VMID</sub>   |  |             | 50k             |              | Ω                |
| <b>Line Input to ADC</b>                  |                     |  |             |                 |              |                  |
| Input Signal Level (0dB)                  | V <sub>INLINE</sub> |  |             | 1.0<br>AVDD/3.3 |              | V <sub>rms</sub> |
| Signal to Noise Ratio<br>(Note 1,2,3)     | SNR                 | A-weighted, 0dB gain<br>@ fs = 48kHz                 | 85          | 90              |              | dB               |
|   |                     | A-weighted, 0dB gain<br>@ fs = 96kHz                 |             | 90              |              |                  |
|   |                     | A-weighted, 0dB gain<br>@ fs = 48kHz,<br>AVDD = 2.7V |             | 88              |              |                  |
| Dynamic Range (Note 3)                    | DNR                 | A-weighted, -60dB full<br>scale input                | 85          | 90              |              | dB               |
| Total Harmonic Distortion                 | THD                 | -1dB input, 0dB gain                                 |             | -84             | -74          | dB               |
| Power Supply Rejection Ratio              | PSSR                | 1kHz 100mVpp   |             | 50              |              | dB               |
|   |                     | 20Hz to 20kHz<br>100mVpp                             |             | 45              |              |                  |
| ADC channel separation                    |                     | 1kHz input   |             | 90              |              | dB               |
| Programmable Gain                         |                     | 1kHz input<br>R <sub>source</sub> < 50Ω              | -34.5       | 0               | +12          | dB               |
| Programmable Gain Step Size               |                     | Guaranteed Monotonic                                 |             | 1.5             |              | dB               |
| Mute attenuation                          |                     | 0dB, 1kHz input                                      |             | 80              |              | dB               |
| Input Resistance                          | R <sub>INLINE</sub> | 0dB gain   | 20k         | 30k             |              | Ω                |
|   |                     | 12dB gain  | 10k         | 15k             |              |                  |
| Input Capacitance                         | C <sub>INLINE</sub> |  |             | 10              |              | pF               |



**Test Conditions**

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V, T<sub>A</sub> = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

| PARAMETER  | SYMBOL | TEST CONDITIONS                             | MIN | TYP               | MAX | UNIT |
|--|--------|---|-----|-------------------|-----|------|
| <b>Line Output for DAC Playback Only (Load = 47kΩ, 50pF)</b> |        |   |     |                   |     |      |
| 0dBfs Full scale output voltage                              |        | At LINE outputs                             |     | 1.0 x<br>AVDD/3.3 |     | Vrms |
| Signal to Noise Ratio<br>(Note 1,2,3)                        | SNR    | A-weighted,<br>@ fs = 48kHz                 | 95  | 100               |     | dB   |
|  |        | A-weighted<br>@ fs = 96kHz                  |     | 98                |     |      |
|  |        | A-weighted,<br>@ fs = 48kHz,<br>AVDD = 2.7V |     | 98                |     |      |
| Dynamic Range (Note 3)                                       | DNR    | A-weighted, -60dB full<br>scale input       | 85  | 95                |     | dB   |
| Total Harmonic Distortion                                    | THD    | 1kHz, 0dBfs                                 |     | -88               | -80 | dB   |
|  |        | 1kHz, -3dBfs                                |     | -92               |     |      |
| Power Supply Rejection Ratio                                 | PSSR   | 1kHz 100mVpp                                |     | 50                |     | dB   |
|  |        | 20Hz to 20kHz<br>100mVpp                    |     | 45                |     |      |
| DAC channel separation                                       |        | 1kHz, 0dB                                   |     | 100               |     | dB   |

**Notes:**

- Ratio of output level with 1kHz full scale input, to the output level with the input short circuited, measured 'A' weighted over a 20Hz to 20kHz bandwidth using an Audio analyser.
- Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20Hz to 20kHz bandwidth.
- All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
- VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).

**TERMINOLOGY**

- Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
- Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
- THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
- Stop band attenuation (dB) – Is the degree to which the frequency spectrum is attenuated (outside audio band).
- Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
- Pass-Band Ripple – Any variation of the frequency response in the pass-band region.

**POWER CONSUMPTION (EXAMPLES)**

| MODE DESCRIPTION              | POWEROFF | OUTPD | DACPD | ADCPD | LINEINPD | CURRENT CONSUMPTION<br>TYPICAL |                 |                 |       |
|-------------------------------|----------|-------|-------|-------|----------|--------------------------------|-----------------|-----------------|-------|
|                               |          |       |       |       |          | AVDD<br>(3.3V)                 | DCVDD<br>(1.5V) | DBVDD<br>(3.3V) | UNITS |
| Record and Playback           | 0        | 0     | 0     | 0     | 0        | 12.2                           | 3.2             | 0.07            | mA    |
| Playback Only                 | 0        | 0     | 0     | 1     | 1        | 3.3                            | 2.3             | 0.07            | mA    |
| Record Only                   | 0        | 1     | 1     | 0     | 0        | 9.2                            | 2.6             | 0.07            | mA    |
| Standby (clock running)       | 0        | 1     | 1     | 1     | 1        | 16                             | 77              | 65              | μA    |
| Standby (clock stopped)       |          | 1     | 1     | 1     | 1        | 16                             | 0.3             | 0.2             | μA    |
| Power Down<br>(clock running) | 1        | 1     | 1     | 1     | 1        | 0.3                            | 77              | 65              | μA    |
| Power Down<br>(clock stopped) | 1        | 1     | 1     | 1     | 1        | 0.3                            | 0.3             | 0.3             | μA    |

**Notes:**

1. The data presented here was measured with the audio interface in slave mode (MS = 0)
2. All figures are quiescent, with no signal.

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### MASTER CLOCK TIMING

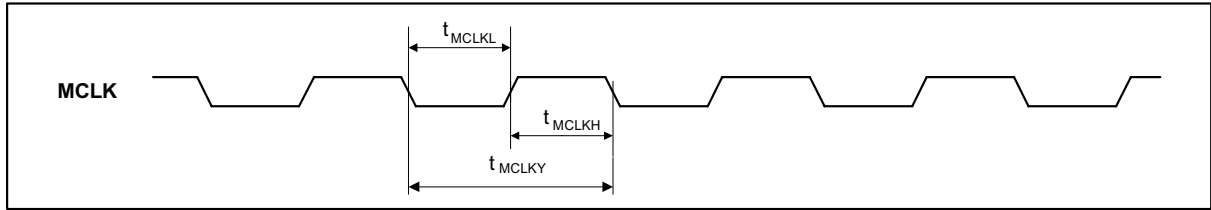


Figure 1 System Clock Timing Requirements

**Test Conditions**

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V,  $T_A = +25^\circ\text{C}$ , Slave Mode,  $f_s = 48\text{kHz}$ , MCLK = 256fs unless otherwise stated.

| PARAMETER                              | SYMBOL    | TEST CONDITIONS | MIN   | TYP | MAX   | UNIT |
|--|-----------|-----------------|-------|-----|-------|------|
| <b>System Clock Timing Information</b> |           |                 |       |     |       |      |
| MCLK System clock pulse width high     | $T_{XTH}$ |                 | 18    |     |       | ns   |
| MCLK System clock pulse width low      | $T_{XTL}$ |                 | 18    |     |       | ns   |
| MCLK System clock cycle time           | $T_{XTY}$ |                 | 54    |     |       | ns   |
| MCLK Duty cycle                        |           |                 | 40:60 |     | 60:40 |      |

### DIGITAL AUDIO INTERFACE – MASTER MODE

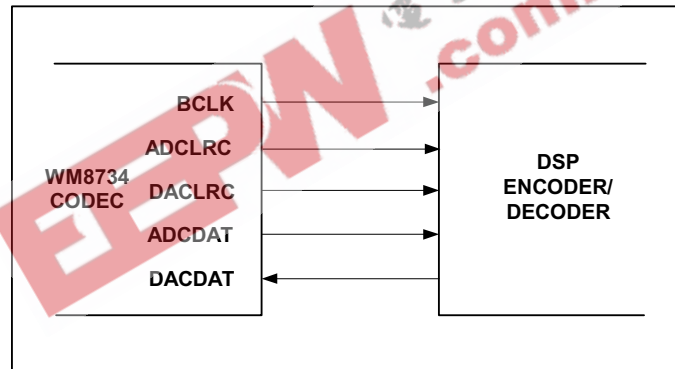


Figure 2 Master Mode Connection

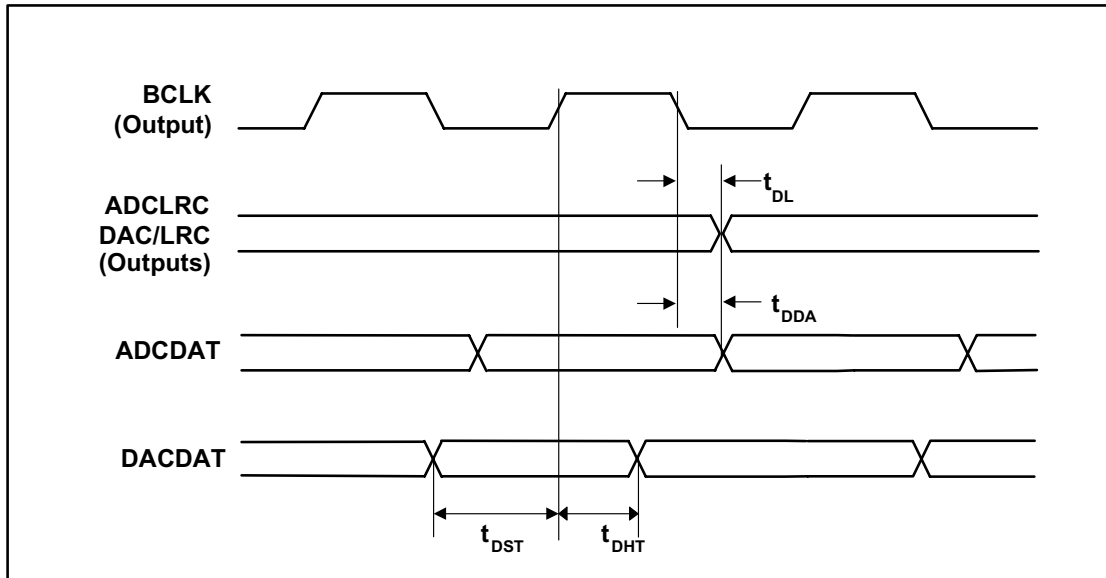


Figure 3 Digital Audio Data Timing – Master Mode

**Test Conditions**

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V,  $T_A = +25^\circ\text{C}$ , Slave Mode,  $f_s = 48\text{kHz}$ , MCLK = 256fs unless otherwise stated.

| PARAMETER  | SYMBOL    | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------|-----------------|-----|-----|-----|------|
| <b>Audio Data Input Timing Information</b>             |           |                 |     |     |     |      |
| ADCLRC/DACLRC propagation delay from BCLK falling edge | $t_{DL}$  |                 | 0   |     | 10  | ns   |
| ADCDAT propagation delay from BCLK falling edge        | $t_{DDA}$ |                 | 0   |     | 15  | ns   |
| DACDAT setup time to BCLK rising edge                  | $t_{DST}$ |                 | 10  |     |     | ns   |
| DACDAT hold time from BCLK rising edge                 | $t_{DHT}$ |                 | 10  |     |     | ns   |

**DIGITAL AUDIO INTERFACE – SLAVE MODE**

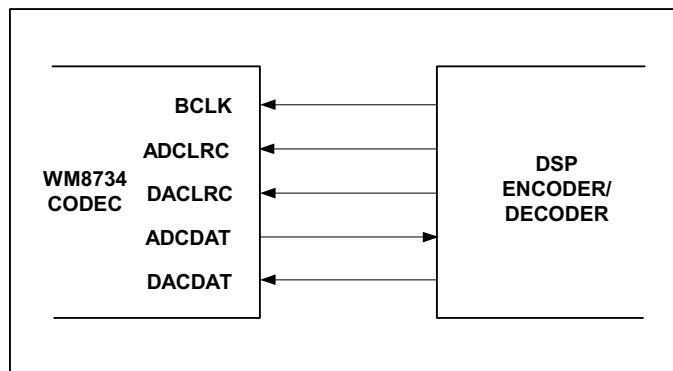


Figure 4 Slave Mode Connection

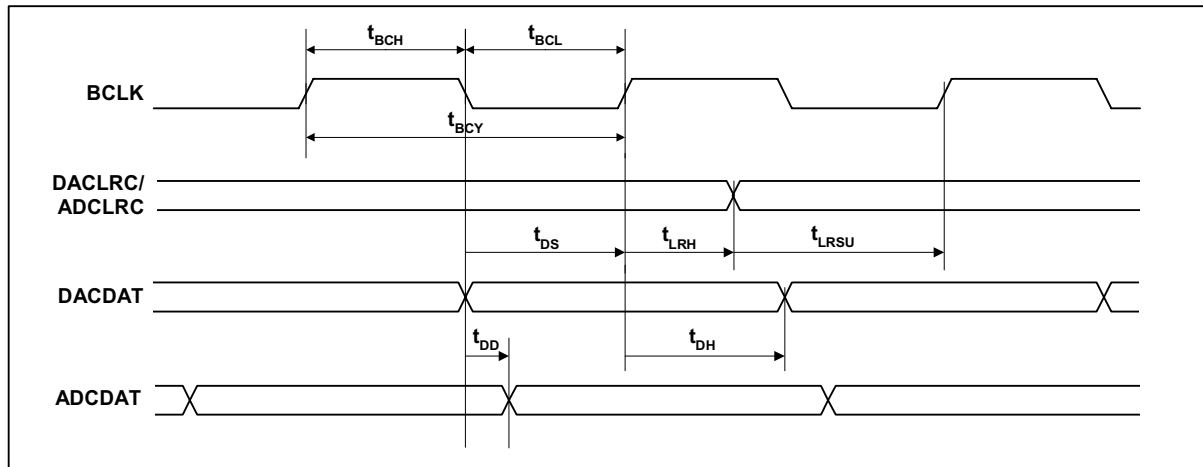


Figure 5 Digital Audio Data Timing – Slave Mode

**Test Conditions**

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V,  $T_A = +25^\circ\text{C}$ , Slave Mode,  $f_s = 48\text{kHz}$ , MCLK = 256fs unless otherwise stated.

| PARAMETER                                       | SYMBOL     | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|------------|-----------------|-----|-----|-----|------|
| <b>Audio Data Input Timing Information</b>      |            |                 |     |     |     |      |
| BCLK cycle time                                 | $t_{BCY}$  |                 | 50  |     |     | ns   |
| BCLK pulse width high                           | $t_{BCH}$  |                 | 20  |     |     | ns   |
| BCLK pulse width low                            | $t_{BCL}$  |                 | 20  |     |     | ns   |
| DACLRC/ADCLRC set-up time to BCLK rising edge   | $t_{LRSU}$ |                 | 10  |     |     | ns   |
| DACLRC/ADCLRC hold time from BCLK rising edge   | $t_{LRH}$  |                 | 10  |     |     | ns   |
| DACDAT set-up time to BCLK rising edge          | $t_{DS}$   |                 | 10  |     |     | ns   |
| DACDAT hold time from BCLK rising edge          | $t_{DH}$   |                 | 10  |     |     | ns   |
| ADCDAT propagation delay from BCLK falling edge | $t_{DD}$   |                 | 0   |     | 10  | ns   |

## MPU INTERFACE TIMING

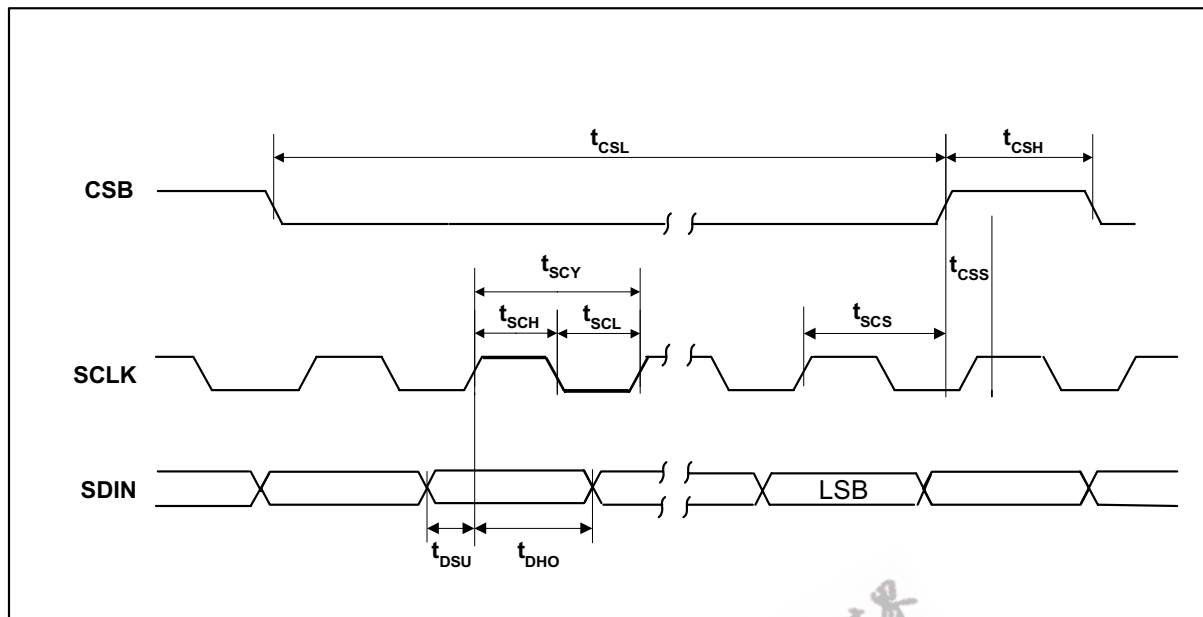


Figure 6 Program Register Input Timing – 3-Wire MPU Serial Control Mode

## Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V,  $T_A = +25^\circ\text{C}$ , Slave Mode,  $f_s = 48\text{kHz}$ ,  $MCLK = 256\text{fs}$  unless otherwise stated.

| PARAMETER                                 | SYMBOL    | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------|-----------------|-----|-----|-----|------|
| <b>Program Register Input Information</b> |           |                 |     |     |     |      |
| SCLK rising edge to CSB rising edge       | $t_{SCS}$ |                 | 60  |     |     | ns   |
| SCLK pulse cycle time                     | $t_{SCY}$ |                 | 80  |     |     | ns   |
| SCLK pulse width low                      | $t_{SCL}$ |                 | 20  |     |     | ns   |
| SCLK pulse width high                     | $t_{SCH}$ |                 | 20  |     |     | ns   |
| SDIN to SCLK set-up time                  | $t_{DSU}$ |                 | 20  |     |     | ns   |
| SCLK to SDIN hold time                    | $t_{DHO}$ |                 | 20  |     |     | ns   |
| CSB pulse width low                       | $t_{CSL}$ |                 | 20  |     |     | ns   |
| CSB pulse width high                      | $t_{CSH}$ |                 | 20  |     |     | ns   |
| CSB rising to SCLK rising                 | $t_{CSS}$ |                 | 20  |     |     | ns   |

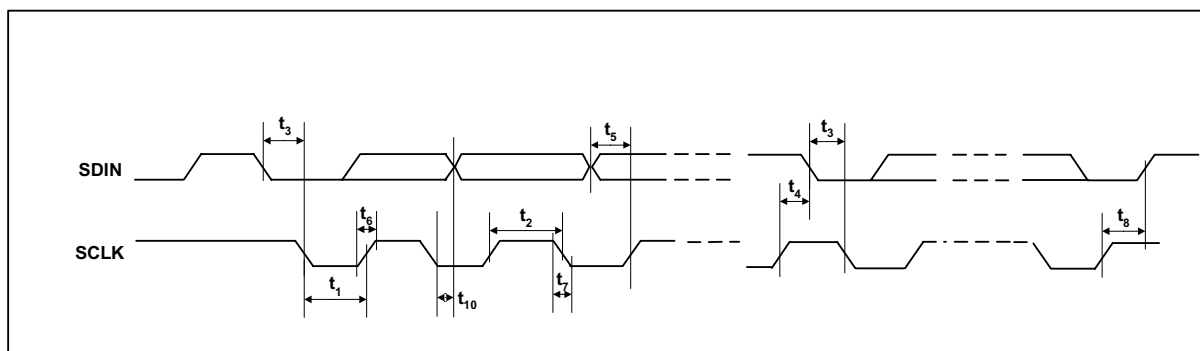


Figure 7 Program Register Input Timing – 2-Wire MPU Serial Control Mode

#### Test Conditions

AVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 3.3V, DGND = 0V,  $T_A = +25^\circ\text{C}$ , Slave Mode,  $f_s = 48\text{kHz}$ , MCLK = 256fs unless otherwise stated.

| PARAMETER                                 | SYMBOL   | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|----------|-----------------|-----|-----|-----|------|
| <b>Program Register Input Information</b> |          |                 |     |     |     |      |
| SCLK Frequency                            |          |                 | 0   |     | 526 | kHz  |
| SCLK Low Pulsewidth                       | $t_1$    |                 | 1.3 |     |     | us   |
| SCLK High Pulsewidth                      | $t_2$    |                 | 600 |     |     | ns   |
| Hold Time (Start Condition)               | $t_3$    |                 | 600 |     |     | ns   |
| Setup Time (Start Condition)              | $t_4$    |                 | 600 |     |     | ns   |
| Data Setup Time                           | $t_5$    |                 | 100 |     |     | ns   |
| SDIN, SCLK Rise Time                      | $t_6$    |                 |     |     | 300 | ns   |
| SDIN, SCLK Fall Time                      | $t_7$    |                 |     |     | 300 | ns   |
| Setup Time (Stop Condition)               | $t_8$    |                 | 600 |     |     | ns   |
| Data Hold Time                            | $t_{10}$ |                 |     |     | 900 | ns   |

## DEVICE DESCRIPTION

The WM8734 is a high performance audio CODEC designed specifically for audio applications that require recording and playback features.

The CODEC includes line inputs to the on-board ADC, line outputs from the on-board DAC, a configurable digital audio interface and a choice of 2 or 3 wire MPU control interface. It is fully compatible and an ideal partner for a range of industry standard microprocessors, controllers and DSPs.

The CODEC includes a stereo low noise input. Line inputs have +12dB to -34dB logarithmic volume level adjustments and mute. All the required input filtering is contained within the device.

The on-board stereo analogue to digital converter (ADC) is of a high quality using a multi-bit high-order oversampling architecture delivering optimum performance with low power consumption. The output from the ADC is available on the digital audio interface. The ADC includes an optional digital high pass filter to remove unwanted dc components from the audio signal.

The on-board digital to analogue converter (DAC) accepts digital audio from the digital audio interface. Digital filter de-emphasis at 32kHz, 44.1kHz and 48kHz can be applied to the digital data under software control. The DAC employs a high quality multi-bit high-order oversampling architecture to again deliver optimum performance with low power consumption.

Special techniques allow the audio to be muted and the device safely placed into standby, sections of the device powered off and volume levels adjusted without any audible clicks, pops or zipper noises. Therefore standby and power off modes may be used dynamically under software control, whenever recording or playback is not required.

The device caters for a number of different sampling rates including industry standard 8kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz and 96kHz. The digital filters used for both record and playback are optimised for each sampling rate used.

The digitised output is available in a number of audio data formats I<sup>2</sup>S, DSP Mode (a burst mode in which frame sync plus 2 data packed words are transmitted), MSB-First, left justified and MSB-First, right justified. The digital audio interface can operate in both master or slave modes.

The software control uses either a 2 or 3-wire MPU interface.

## AUDIO SIGNAL PATH

### LINE INPUTS

The WM8734 provides Left and Right channel line inputs (RLINEIN and LLINEIN). The inputs are high impedance and low capacitance, thus ideally suited to receiving line level signals from external hi-fi or audio equipment.

Both line inputs include independent programmable volume level adjustments and input mute. The scheme is illustrated in Figure 8. Passive RF and active Anti-Alias filters are also incorporated within the line inputs. These prevent high frequencies aliasing into the audio band or otherwise degrading performance.



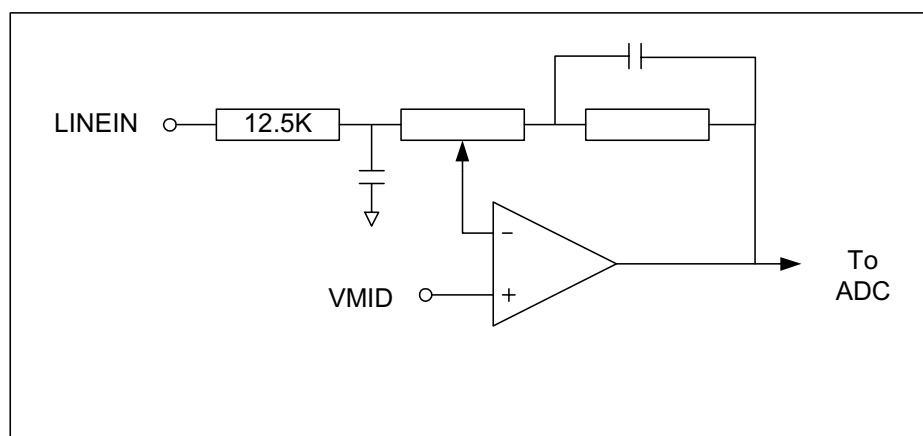


Figure 8 Line Input Schematic

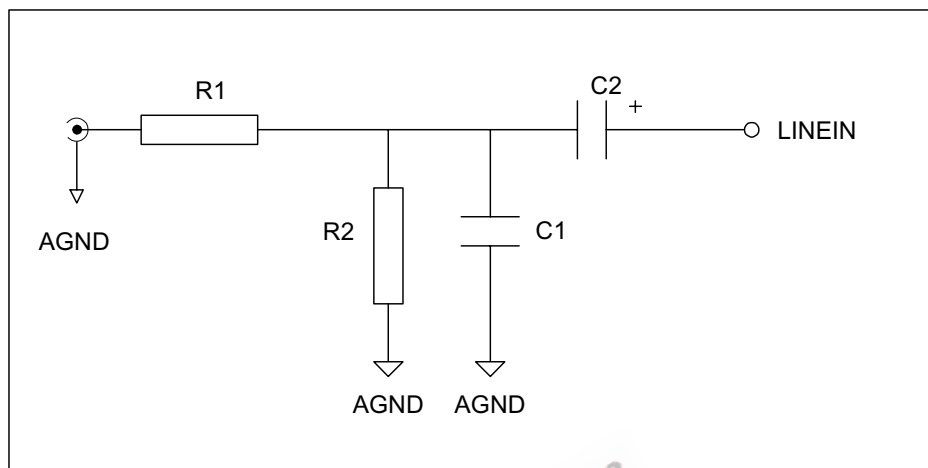
The gain between the line inputs and the ADC is logarithmically adjustable from +12dB to -34.5dB in 1.5dB steps under software control. The ADC Full Scale input is 1.0V rms at AVDD = 3.3 volts. Any voltage greater than full scale will possibly overload the ADC and cause distortion. Note that the full scale input tracks directly with AVDD. The gain is independently adjustable on both Right and Left Line Inputs. However, by setting the INBOTH bit whilst programming the volume control, both channels are simultaneously updated with the same value. Use of INBOTH reduces the required number of software writes required. The line inputs to the ADC can be muted in the analogue domain under software control. The software control registers are shown below.

| REGISTER ADDRESS         | BIT | LABEL       | DEFAULT        | DESCRIPTION  |
|--------------------------|-----|-------------|----------------|--|
| 0000000<br>Left Line In  | 4:0 | LINVOL[4:0] | 10111<br>(0dB) | Left Channel Line Input Volume Control<br>11111 = +12dB . . 1.5dB steps down<br>to 00000 = -34.5dB   |
|                          | 7   | LINMUTE     | 1              | Left Channel Line Input Mute to ADC<br>1 = Enable Mute<br>0 = Disable Mute   |
|                          | 8   | LRINBOTH    | 0              | Left to Right Channel Line Input<br>Volume and Mute Data Load Control<br>1 = Enable Simultaneous Load of<br>LINVOL[4:0] and LINMUTE to<br>RINVOL[4:0] and RINMUTE<br>0 = Disable Simultaneous Load |
| 0000001<br>Right Line In | 4:0 | RINVOL[4:0] | 10111<br>(0dB) | Right Channel Line Input Volume<br>Control<br>11111 = +12dB . . 1.5dB steps down<br>to 00000 = -34.5dB   |
|                          | 7   | RINMUTE     | 1              | Right Channel Line Input Mute to<br>ADC<br>1 = Enable Mute<br>0 = Disable Mute   |
|                          | 8   | RLINBOTH    | 0              | Right to Left Channel Line Input<br>Volume and Mute Data Load Control<br>1 = Enable Simultaneous Load of<br>RINVOL[4:0] and RINMUTE to<br>LINVOL[4:0] and LINMUTE<br>0 = Disable Simultaneous Load |

Table 1 Line Input Software Control

The line inputs are biased internally through the operational amplifier to VMID. Whenever the line inputs are muted or the device placed into standby mode, the line inputs are kept biased to VMID using special anti-thump circuitry. This reduces any audible clicks that may otherwise be heard when re-activating the inputs.

The external components required to complete the line input application is shown in the Figure 9.



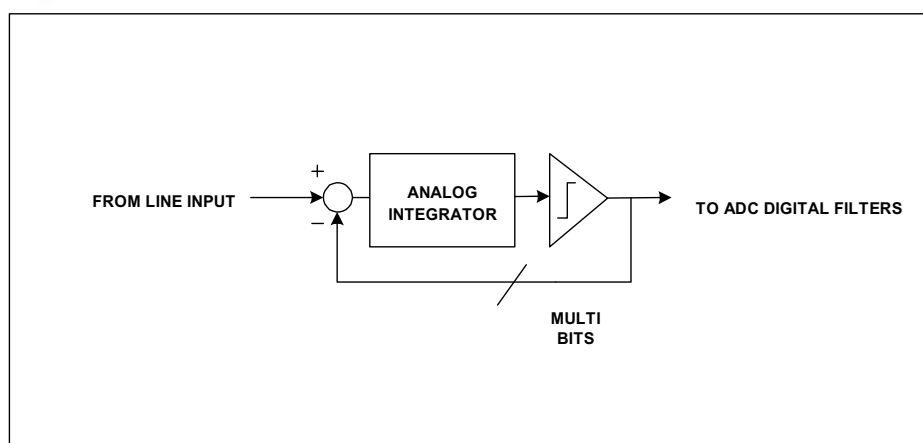
**Figure 9 Line Input Application Drawing**

For interfacing to a typical CD system, it is recommended that the input is scaled to ensure that there is no clipping of the signal.  $R1 = 5K$ ,  $R2 = 5K$ ,  $C1 = 47pF$ ,  $C2 = 470nF$  (10V npo ceramic type).

$R1$  and  $R2$  form a resistive divider to attenuate the  $2 V_{rms}$  output from a CD player to a  $1 V_{rms}$  level, so avoiding overloading the inputs.  $R2$  also provides a discharge path for  $C2$ , thus preventing the input to  $C2$  charging to an excessive voltage which may otherwise damage any equipment connected that is not suitably protected against high voltages.  $C1$  forms an RF low pass filter for increasing the rejection of RF interference picked up on any cables.  $C2$  forms a DC blocking capacitor to remove the DC path between the WM8734 and the driving audio equipment.  $C2$  together with the input impedance of the WM8734 form a high pass filter.

### ADC

The WM8734 uses a multi-bit oversampled sigma-delta ADC. A single channel of the ADC is illustrated in the Figure 10.



**Figure 10 Multi-Bit Oversampling Sigma Delta ADC Schematic**

The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise.

The ADC Full Scale input is 1.0V rms at AVDD = 3.3 volts. Any voltage greater than full scale will possibly overload the ADC and cause distortion. Note that the full scale input tracks directly with AVDD. The device employs a pair of ADCs. The two channels cannot be selected independently.

The digital data from the ADC is fed for signal processing to the ADC Filters.

### ADC FILTERS

The ADC filters perform true 24 bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface. Figure 11 illustrates the digital filter path.

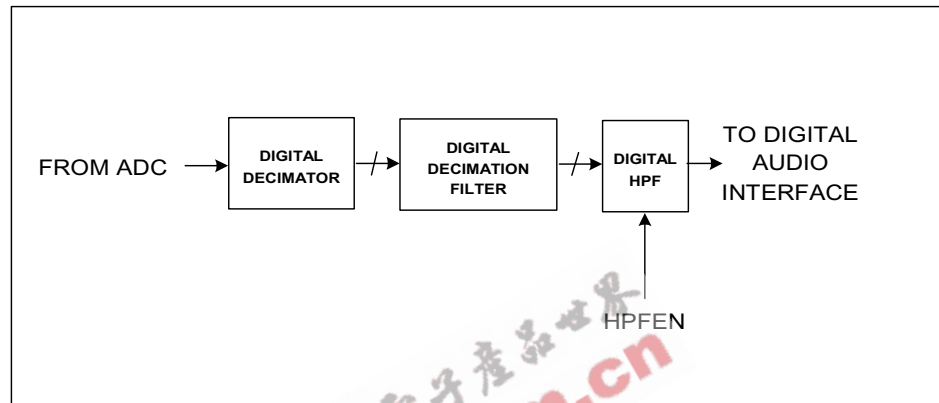


Figure 11 ADC Digital Filter

The ADC digital filters contain a digital high pass filter, selectable via software control. The high-pass filter response detailed in Digital Filter Characteristics. When the high-pass filter is enabled the dc offset is continuously calculated and subtracted from the input signal. By setting HPOR the last calculated dc offset value is stored when the high-pass filter is disabled and will continue to be subtracted from the input signal. If the dc offset changed, the stored and subtracted value will not change unless the high-pass filter is enabled. The software control is shown in Table 2.

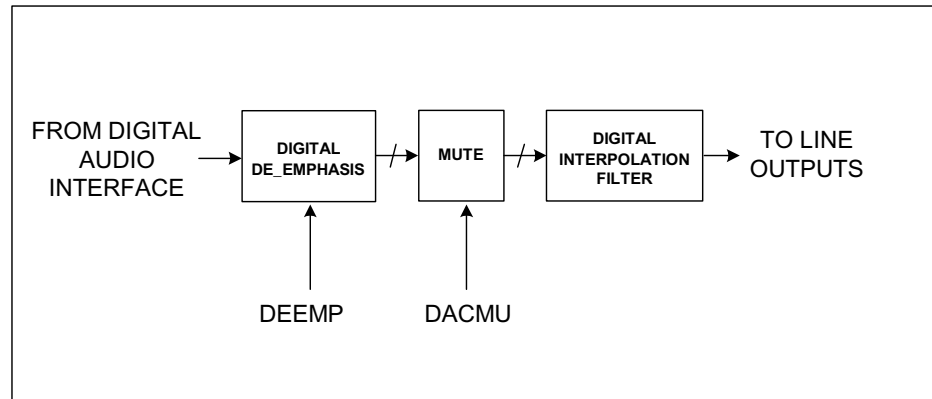
| REGISTER ADDRESS                       | BIT | LABEL  | DEFAULT | DESCRIPTION  |
|--|-----|--------|---------|--|
| 00000101<br>Digital Audio Path Control | 0   | ADCHPD | 0       | ADC High Pass Filter Enable (Digital)<br>1 = Disable High Pass Filter<br>0 = Enable High Pass Filter |
|  | 4   | HPOR   | 0       | Store dc offset when High Pass Filter disabled<br>1 = store offset<br>0 = clear offset               |

Table 2 ADC Software Control

There are several types of ADC filters, frequency and phase responses of these are shown in Digital Filter Characteristics. The filter types are automatically configured depending on the sample rate chosen. Refer to the sample rate section for more details.

### DAC FILTERS

The DAC filters perform true 24 bit signal processing to convert the incoming digital audio data from the digital audio interface at the specified sample rate to multi-bit oversampled data for processing by the analogue DAC. Figure 12 illustrates the DAC digital filter path.



**Figure 12 DAC Filter Schematic**

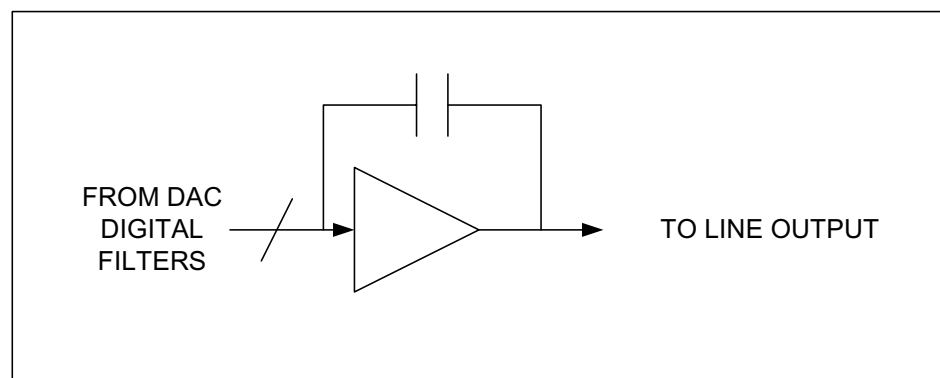
The DAC digital filter can apply digital de-emphasis under software control, as shown in Table 3. The DAC can also perform a soft mute where the audio data is digitally brought to a mute level. This removes any abrupt step changes in the audio that might otherwise result in audible clicks in the audio outputs.

| REGISTER ADDRESS                      | BIT | LABEL      | DEFAULT | DESCRIPTION   |
|---------------------------------------|-----|------------|---------|---|
| 0000101<br>Digital Audio Path Control | 2:1 | DEEMP[1:0] | 00      | De-emphasis Control (Digital)<br>11 = 48kHz<br>10 = 44.1kHz<br>01 = 32kHz<br>00 = Disable |
|                                       | 3   | DACMU      | 1       | DAC Soft Mute Control (Digital)<br>1 = Enable soft mute<br>0 = Disable soft mute          |

**Table 3 DAC Software Control**

### DAC

The WM8734 employs a multi-bit sigma delta oversampling digital to analogue converter. The scheme for the converter is illustrated in Figure 13.



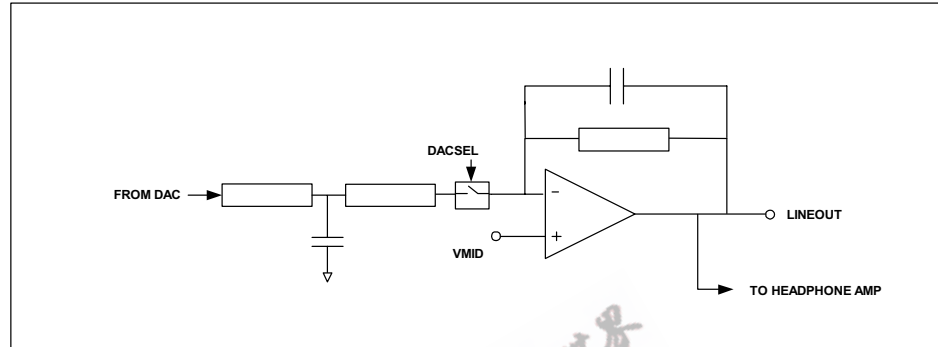
**Figure 13 Multi-Bit Oversampling Sigma Delta Schematic**

The DAC converts the multi-level digital audio data stream from the DAC digital filters into high quality analogue audio.

**LINE OUTPUTS**

The WM8734 provides two low impedance line outputs LLINEOUT and RLINEOUT, suitable for driving typical line loads of impedance 10K and capacitance 50pF. The line output is used to selectively sum the outputs from the DAC or/and the Line inputs in bypass mode.

The LLINEOUT and RLINEOUT outputs are only available at a line output level and are not level adjustable in the analogue domain, having a fixed gain of 0dB. The level is fixed such that at the DAC full scale level the output level is  $V_{rms}$  at  $AVDD = 3.3$  volts. Note that the DAC full scale level tracks directly with  $AVDD$ . The scheme is shown in Figure 14. The line output includes a low order audio low pass filter for removing out-of band components from the sigma-delta DAC. Therefore no further external filtering is required in most applications.



**Figure 14 Line Output Schematic**

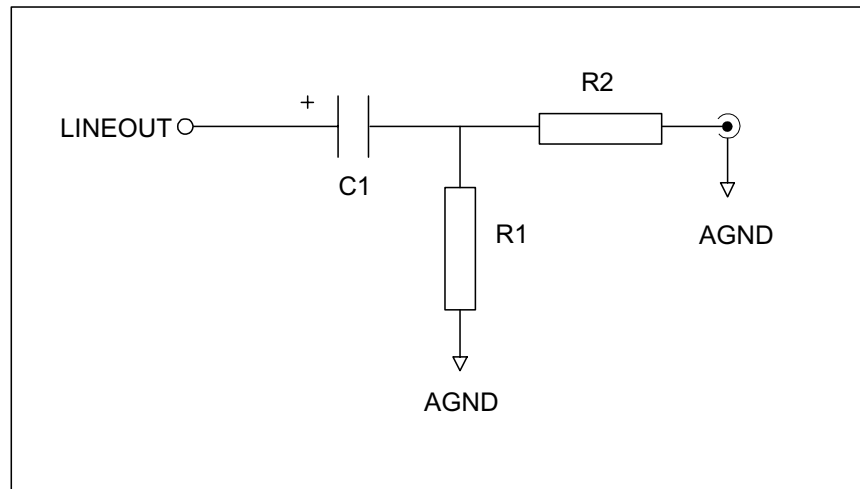
The line output is muted by either muting the DAC (analogue) or Soft Muting (digital). Refer to the DAC section for more details. Whenever the DAC is muted or the device placed into standby mode the DC voltage is maintained at the line outputs to prevent any audible clicks from being present.

The software control for the line outputs is shown in Table 4.

| REGISTER ADDRESS                       | BIT | LABEL  | DEFAULT | DESCRIPTION  |
|--|-----|--------|---------|--|
| 0000100<br>Analogue Audio Path Control | 4   | DACSEL | 0       | DAC Select<br>1 = Select DAC<br>0 = Don't select DAC |

**Table 4 Output Software Control**

The recommended external components are shown in Figure 15.



**Figure 15 Line Outputs Application Drawing**

Recommended values are C1 = 470nF (10V npo type), R1 = 47K $\Omega$ , R2 = 100 $\Omega$

C1 forms a DC blocking capacitor to the line outputs. R1 prevents the output voltage from drifting so protecting equipment connected to the line output. R2 forms a de-coupling resistor preventing abnormal loads from disturbing the device. Note that poor choice of dielectric material for C1 can have dramatic effects on the measured signal distortion at the output.

## DEVICE OPERATION

### DEVICE RESETTING

The WM8734 contains a power on reset circuit that resets the internal state of the device to a known condition. The power on reset is applied as DCVDD powers on and released only after the voltage level of DCVDD crosses a minimum turn off threshold. If DCVDD later falls below a minimum turn on threshold voltage then the power on reset is re-applied. The threshold voltages and associated hysteresis are shown in the Electrical Characteristics table.

The user also has the ability to reset the device to a known state under software control as shown in the table below.

| REGISTER ADDRESS          | BIT | LABEL | DEFAULT   | DESCRIPTION  |
|---------------------------|-----|-------|-----------|--|
| 0001111<br>Reset Register | 8:0 | RESET | not reset | Reset Register<br>Writing 00000000 to register resets device |

**Table 5 Software Control of Reset**

When using the software reset. In 3-wire mode the reset is applied on the rising edge of CSB and released on the next rising edge of SCLK. In 2-wire mode the reset is applied for the duration of the ACK signal (approximately 1 SCLK period, refer to Figure 24).

### CLOCKING SCHEMES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. To allow WM8734 to be used in a centrally clocked system, the WM8734 is capable of deriving the sample rate clock from this Master Clock (Master Mode) or receiving the sample rate clock from an external source (Slave Mode).

### CORE CLOCK

The WM8734 DSP core can be clocked either by MCLK or MCLK divided by 2. This is controlled by software as shown in Table 6 below.

| REGISTER ADDRESS            | BIT | LABEL    | DEFAULT | DESCRIPTION  |
|-----------------------------|-----|----------|---------|--|
| 0001000<br>Sampling Control | 6   | CLKIDIV2 | 0       | Core Clock divider select<br>1 = Core Clock is MCLK divided by 2<br>0 = Core Clock is MCLK |

**Table 6 Software Control of Core Clock**

Having a programmable MCLK divider allows the device to be used in applications where higher frequency master Clocks are available. For example the device can support 512fs master clocks whilst fundamentally operating in a 256fs mode.

### DIGITAL AUDIO INTERFACES

WM8734 may be operated in either one of the 4 offered audio interface modes. These are:

- Right justified
- Left justified
- I<sup>2</sup>S
- DSP mode

All four of these modes are MSB first and operate with data 16 to 32 bits, except right justified mode which does not support 32 bits.

The digital audio interface takes the data from the internal ADC digital filter and places it on the ADCDAT output. ADCDAT is the formatted digital audio data stream output from the ADC digital filters with left and right channels multiplexed together. ADCLRC is an alignment clock that controls whether Left or Right channel data is present on the ADCDAT lines. ADCDAT and ADCLRC are synchronous with the BCLK signal with each data bit transition signified by a BCLK high to low transition. BCLK maybe an input or an output dependent on whether the device is in master or slave mode. Refer to the MASTER/SLAVE OPERATION section.

The digital audio interface also receives the digital audio data for the internal DAC digital filters on the DACDAT input. DACDAT is the formatted digital audio data stream output to the DAC digital filters with left and right channels multiplexed together. DACLRC is an alignment clock that controls whether Left or Right channel data is present on DATDAT. DACDAT and DACLRC are synchronous with the BCLK signal with each data bit transition signified by a BCLK transition. DACDAT is always an input. BCLK and DACLRC are either outputs or inputs depending whether the device is in master or slave mode. Refer to the MASTER/SLAVE OPERATION section

There are four digital audio interface formats accommodated by the WM8734. These are shown in the figures below. Refer to the Electrical Characteristic section for timing information.

Left Justified mode is where the MSB is available on the first rising edge of BCLK following a ADCLR or DACLRC transition.

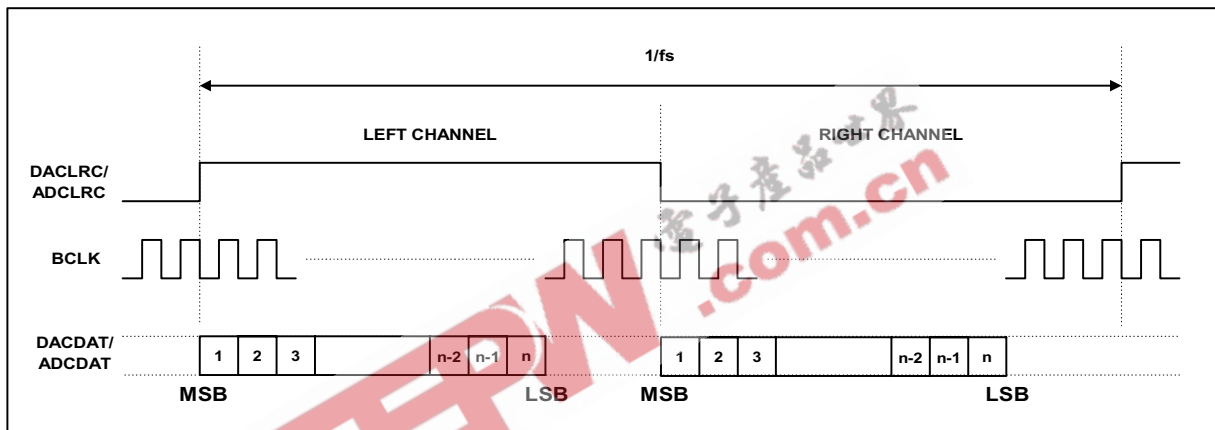


Figure 16 Left Justified Mode

I<sup>2</sup>S mode is where the MSB is available on the 2<sup>nd</sup> rising edge of BCLK following a DACLRC or ADCLRC transition.

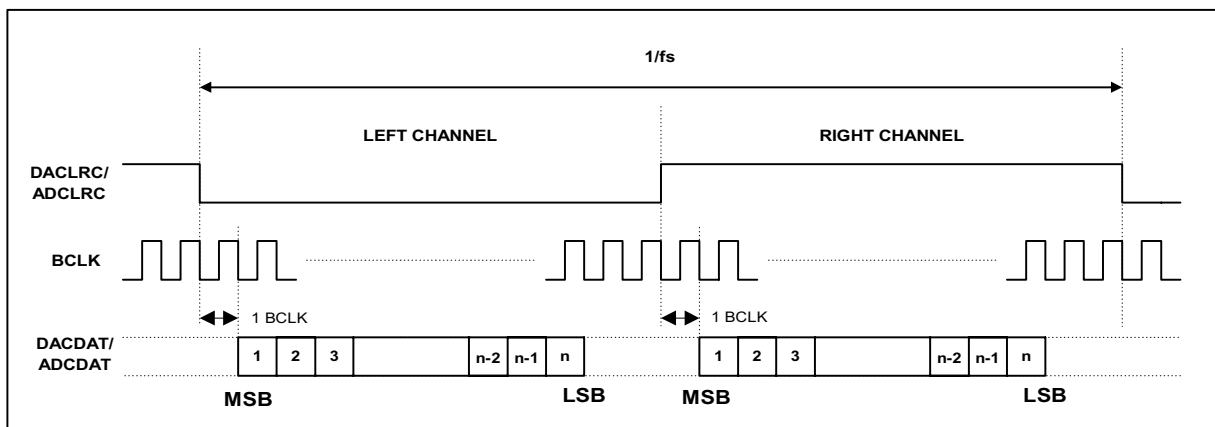


Figure 17 I<sup>2</sup>S Mode

Right Justified mode is where the LSB is available on the rising edge of BCLK preceding a DACLRC or ADCLRC transition, yet MSB is still transmitted first.

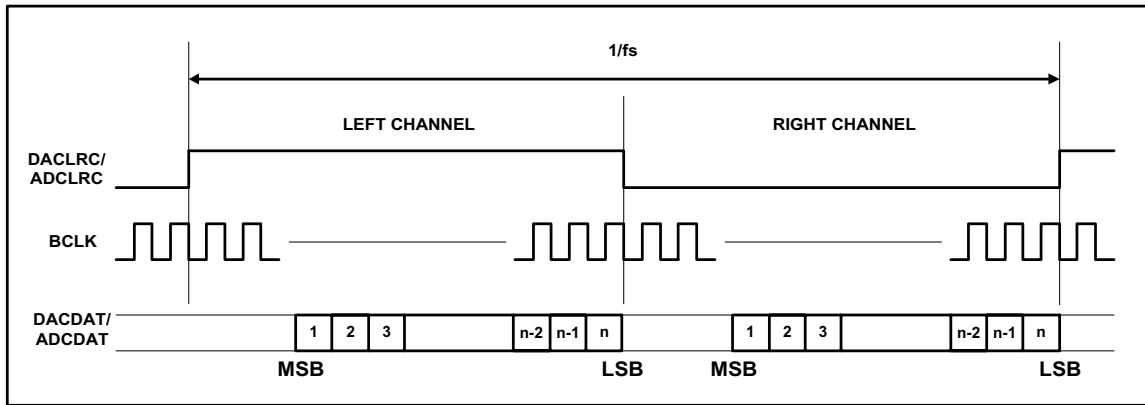


Figure 18 Right Justified Mode

In DSP/PCM mode, the left channel MSB is available on either the 1<sup>st</sup> (mode B) or 2<sup>nd</sup> (mode A) rising edge of BCLK (selectable by LRP) following a rising edge of LRC. Right channel data immediately follows left channel cycles. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

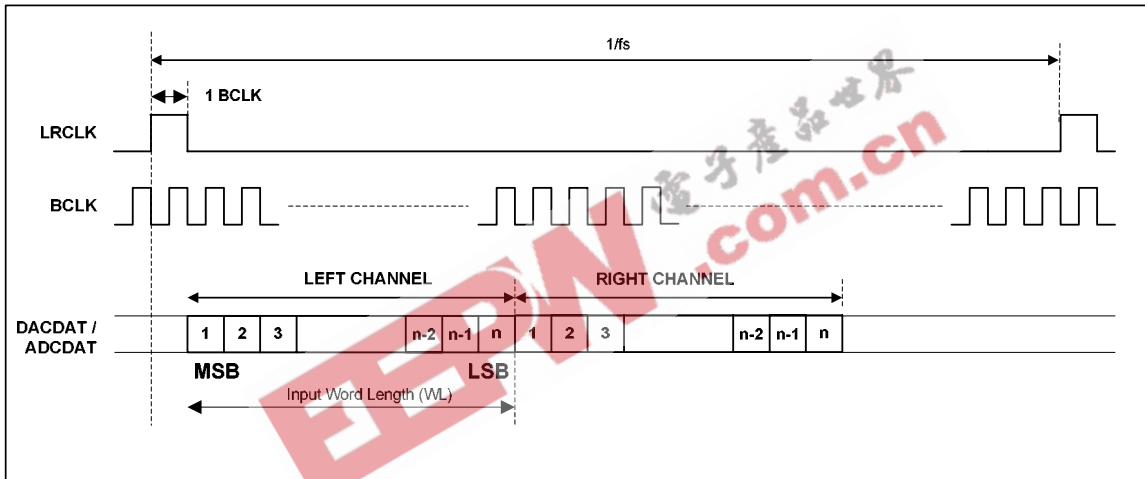


Figure 19 DSP/PCM Mode Audio Interface (mode A, LRP=1)

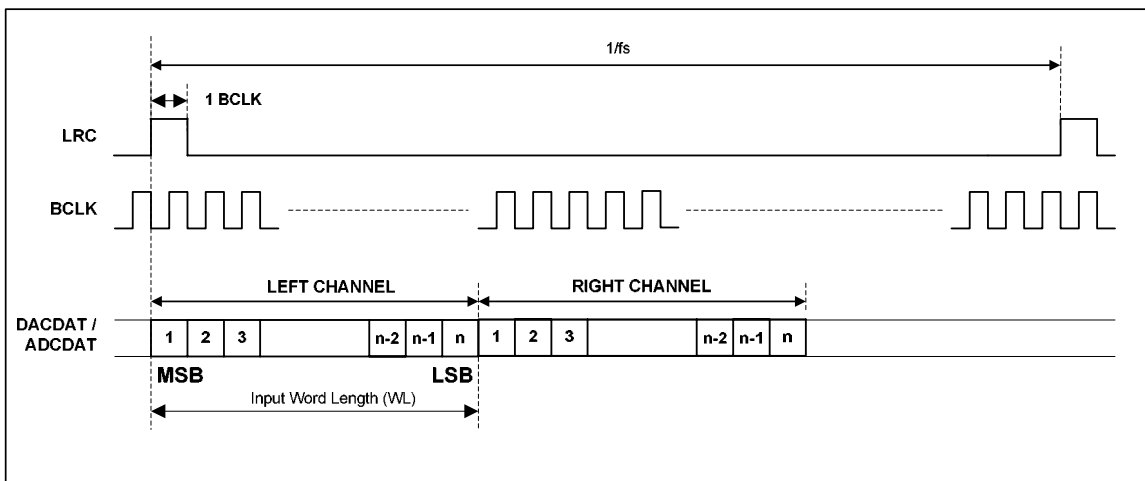


Figure 20 DSP/PCM Mode Audio Interface (mode B, LRP=0)



In all modes DACLRC and ADCLRC must always change on the falling edge of BCLK, refer to Figure 16, Figure 17, Figure 18, Figure 19 and Figure 20.

Operating the digital audio interface in DSP mode allows ease of use for supporting the various sample rates and word lengths. The only requirement is that all data is transferred within the correct number of BCLK cycles to suit the chosen word length.

In order for the digital audio interface to offer similar support in the three other modes (Left Justified, I<sup>2</sup>S and Right Justified), the DACLRC, ADCLRC and BCLK frequencies, continuity and mark-space ratios need more careful consideration.

In Slave mode, DACLRC and ADCLRC inputs are not required to have a 50:50 mark-space ratio. BCLK input need not be continuous. It is however required that there are sufficient BCLK cycles for each DACLRC/ADCLRC transition to clock the chosen data word length.

In Master mode, DACLRC and ADCLRC will be output with a 50:50 mark-space ratio with BCLK output at 64fs.

The ADC and DAC digital audio interface modes are software configurable as indicated in Table 7. Note that dynamically changing the software format may result in erroneous operation of the interfaces and is therefore not recommended. The length of the digital audio data is programmable at 16/20/24 or 32 bits. Refer to the software control table below. The data is signed 2's complement. Both ADC and DAC are fixed at the same data length. The ADC and DAC digital filters process data using 24 bits. If the ADC is programmed to output 16 or 20 bit data then it strips the LSBs from the 24 bit data. If the ADC is programmed to output 32 bits then it packs the LSBs with zeros. If the DAC is programmed to receive 16 or 20 bit data, the WM8734 packs the LSBs with zeros. If the DAC is programmed to receive 32 bit data, then it strips the LSBs.

The DAC outputs can be swapped under software control using LRP and LRSWAP as shown in Table 7. Stereo samples are normally generated as a Left/Right sampled pair. LRSWAP reverses the order of that a Left sample goes to the right DAC output and a Right sample goes to the left DAC output. LRP swaps the phasing so that a Right/Left sampled pair is expected and preserves the correct channel phase difference.

To accommodate system timing requirements the interpretation of BCLK may be inverted, this is controlled via the software shown in Table 6. This is especially appropriate for DSP mode.

ADCDAT lines are always outputs. They power up and return from standby low.

DACDAT is always an input. It is expected to be set low by the audio interface controller when the WM8734 is powered off or in standby.

ADCLRC, DACLRC and BCLK can be either outputs or inputs depending on whether the device is configured as a master or slave. If the device is a master then the ADCLRC, DACLRC and BCLK signals are outputs that default low. If the device is a slave then the ADCLRC, DACLRC and BCLK are inputs.

| REGISTER ADDRESS                          | BIT | LABEL       | DEFAULT | DESCRIPTION  |
|---|-----|-------------|---------|--|
| 0000111<br>Digital Audio Interface Format | 1:0 | FORMAT[1:0] | 10      | Audio Data Format Select<br>11 = DSP Mode, frame sync + 2 data packed words<br>10 = I <sup>2</sup> S Format, MSB-First left-1 justified<br>01 = MSB-First, left justified<br>00 = MSB-First, right justified   |
|   | 3:2 | IWL[1:0]    | 10      | Input Audio Data Bit Length Select<br>11 = 32 bits<br>10 = 24 bits<br>01 = 20 bits<br>00 = 16 bits   |
|   | 4   | LRP         | 0       | DACLRRC phase control (in left, right or I <sup>2</sup> S modes)<br>1 = Right Channel DAC data when DACLRRC high<br>0 = Right Channel DAC data when DACLRRC low<br>(opposite phasing in I <sup>2</sup> S mode)<br>or<br>DSP mode A/B select (in DSP mode only)<br>1 = MSB is available on 2nd BCLK rising edge after ADCLRRC/DACLRRC rising edge<br>0 = MSB is available on 1st BCLK rising edge after ADCLRRC/DACLRRC rising edge |
|   | 5   | LRSWAP      | 0       | DAC Left Right Clock Swap<br>1 = Right Channel DAC Data Left<br>0 = Right Channel DAC Data Right   |
|   | 6   | MS          | 0       | Master Slave Mode Control<br>1 = Enable Master Mode<br>0 = Enable Slave Mode   |
|   | 7   | BCLKINV     | 0       | Bit Clock Invert<br>1 = Invert BCLK<br>0 = Don't invert BCLK   |

Table 7 Digital Audio Interface Control

**Note:** If right justified 32 bit mode is selected then the WM8734 defaults to 24 bits.

#### MASTER AND SLAVE MODE OPERATION

The WM8734 can be configured as either a master or slave mode device. As a master mode device the WM8734 controls sequencing of the data and clocks on the digital audio interface. As a slave device the WM8734 responds with data to the clocks it receives over the digital audio interface. The mode is set with the MS bit of the control register as shown in Table 8.

| REGISTER ADDRESS                          | BIT | LABEL | DEFAULT | DESCRIPTION  |
|---|-----|-------|---------|--|
| 0000111<br>Digital Audio Interface Format | 6   | MS    | 0       | Master Slave Mode Control<br>1 = Enable Master Mode<br>0 = Enable Slave Mode |

Table 8 Programming Master/Slave Modes

As a master mode device the WM8734 controls the sequencing of data transfer (ADCDAT, DACDAT) and output of clocks (BCLK, ADCLRC, DACLRC) over the digital audio interface. It uses the timing generated from either its on-board crystal or the MCLK input as the reference for the clock and data transitions. This is illustrated in Figure 21. ADCDAT is always an output from and DACDAT is always an input to the WM8734 independent of master or slave mode.

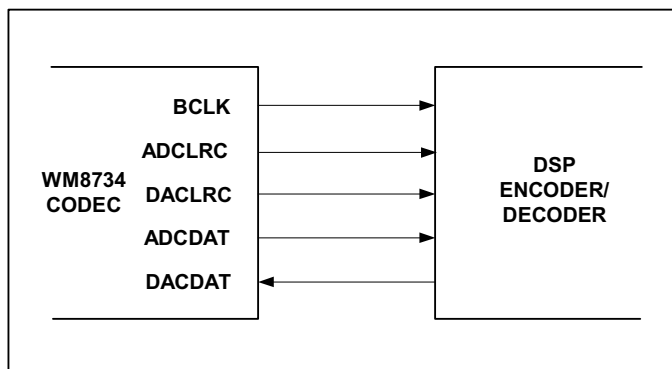


Figure 21 Master Mode

As a slave device the WM8734 sequences the data transfer (ADCDAT, DACDAT) over the digital audio interface in response to the external applied clocks (BCLK, ADCLRC, DACLRC). This is illustrated in Figure 22.

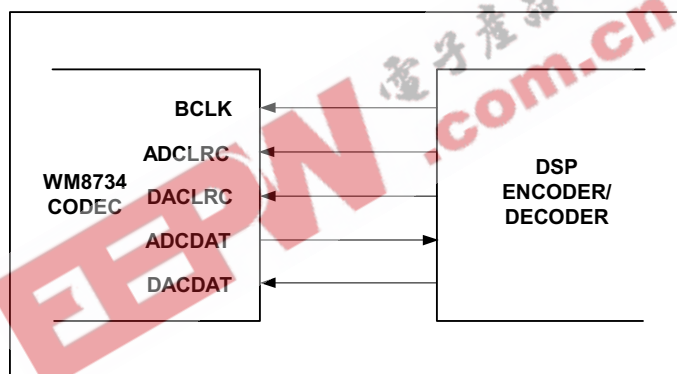


Figure 22 Slave Mode

Note that the WM8734 relies on controlled phase relationships between audio interface BCLK, DACLRC and the master MCLK. To avoid any timing hazards, refer to the timing section for detailed information.

## AUDIO DATA SAMPLING RATES

The WM8734 provides for two modes of operation (normal and USB) to generate the required DAC and ADC sampling rates. Normal and USB modes are programmed under software control according to the table below.

In Normal mode, the user controls the sample rate by using an appropriate MCLK or crystal frequency and the sample rate control register setting. The WM8734 can support sample rates from 8ks/s up to 96ks/s.

In USB mode, the user must use a fixed MCLK or crystal frequency of 12MHz to generate sample rates from 8ks/s to 96ks/s. It is called USB mode since the common USB (Universal Serial Bus) clock is at 12MHz and the WM8734 can be directly used within such systems. WM8734 can generate all the normal audio sample rates from this one Master Clock frequency, removing the need for different master clocks or PLL circuits.

Uniquely, the WM8734 offers the user the ability to sample the ADC and DAC at different rates under software control in both Normal and USB modes. This reduces the burden on any controlling DSP. However, the signal processing in the ADC and DAC over-sampling filters is tightly coupled together in order to minimise power consumption. To this end, only the combinations of sample rates listed in the following sections are supported. Note that these rates supported are anticipated to be the likely combinations used in typical audio systems.

| REGISTER ADDRESS            | BIT                                | LABEL  | DEFAULT  | DESCRIPTION   |                                    |  |
|-----------------------------|------------------------------------|--|--|---|------------------------------------|--|
| 0001000<br>Sampling Control | 0                                  | USB/<br>NORMAL   | 0  | Mode Select<br>1 = USB mode (250/272fs)<br>0 = Normal mode (256/384fs)  |                                    |  |
|                             | 1                                  | BOSR   | 0  | Base Over-Sampling Rate<br><table border="1" style="width: 100%;"> <tr> <td>USB Mode<br/>0 = 250fs<br/>1 = 272fs</td> <td>Normal Mode<br/>96/88.2 kHz<br/>0 = 256fs<br/>0 = 128fs<br/>1 = 384fs<br/>1 = 192fs</td> </tr> </table> | USB Mode<br>0 = 250fs<br>1 = 272fs | Normal Mode<br>96/88.2 kHz<br>0 = 256fs<br>0 = 128fs<br>1 = 384fs<br>1 = 192fs |
|                             | USB Mode<br>0 = 250fs<br>1 = 272fs | Normal Mode<br>96/88.2 kHz<br>0 = 256fs<br>0 = 128fs<br>1 = 384fs<br>1 = 192fs |  |   |                                    |  |
| 5:2                         | SR[3:0]                            | 0000   | ADC and DAC sample rate control;<br>See USB Mode and Normal Mode<br>Sample Rate sections for operation |   |                                    |  |

Table 9 Sample Rate Control

### SAMPLE RATE SETTING

In normal mode MCLK/crystal oscillator is set up according to the desired sample rates of the ADC and DAC. For ADC or DAC sampling rates of 8, 32, 48 or 96kHz, MCLK frequencies of either 12.288MHz (256fs) or 18.432MHz (384fs) can be used. For ADC or DAC sampling rates of 8, 44.1 or 88.2kHz from MCLK frequencies of either 11.2896MHz (256fs) or 16.9344MHz (384fs) can be used.

The table below should be used to set up the device to work with the various sample rate combinations. For example if the user wishes to use the WM8734 in normal mode with the ADC and DAC sample rates at 48kHz and 48kHz respectively then the device should be programmed with BOSR = 0, SR3 = 0, SR2 = 0, SR1 = 0 and SR0 = 0 with a 12.288MHz MCLK or with BOSR = 1, SR3 = 0, SR2 = 0, SR1 = 0 and SR0 = 0 with a 18.432MHz MCLK. The ADC and DAC will then operate with a Digital Filter of type 1, refer to Digital Filter Characteristics section for an explanation of the different filter types.

| SAMPLING RATE |               | MCLK FREQUENCY | SAMPLE RATE REGISTER SETTINGS |     |     |     |     | DIGITAL FILTER TYPE |
|---------------|---------------|----------------|-------------------------------|-----|-----|-----|-----|---------------------|
| ADC           | DAC           |                | BOSR                          | SR3 | SR2 | SR1 | SR0 |                     |
| kHz           | kHz           | MHz            |                               |     |     |     |     |                     |
| 48            | 48            | 12.288         | 0 (256fs)                     | 0   | 0   | 0   | 0   | 1                   |
|               |               | 18.432         | 1 (384fs)                     | 0   | 0   | 0   | 0   |                     |
| 48            | 8             | 12.288         | 0 (256fs)                     | 0   | 0   | 0   | 1   | 1                   |
|               |               | 18.432         | 1 (384fs)                     | 0   | 0   | 0   | 1   |                     |
| 8             | 48            | 12.288         | 0 (256fs)                     | 0   | 0   | 1   | 0   | 1                   |
|               |               | 18.432         | 1 (384fs)                     | 0   | 0   | 1   | 0   |                     |
| 8             | 8             | 12.288         | 0 (256fs)                     | 0   | 0   | 1   | 1   | 1                   |
|               |               | 18.432         | 1 (384fs)                     | 0   | 0   | 1   | 1   |                     |
| 32            | 32            | 12.288         | 0 (256fs)                     | 0   | 1   | 1   | 0   | 1                   |
|               |               | 18.432         | 1 (384fs)                     | 0   | 1   | 1   | 0   |                     |
| 96            | 96            | 12.288         | 0 (128fs)                     | 0   | 1   | 1   | 1   | 2                   |
|               |               | 18.432         | 1 (192fs)                     | 0   | 1   | 1   | 1   |                     |
| 44.1          | 44.1          | 11.2896        | 0 (256fs)                     | 1   | 0   | 0   | 0   | 1                   |
|               |               | 16.9344        | 1 (384fs)                     | 1   | 0   | 0   | 0   |                     |
| 44.1          | 8<br>(Note 1) | 11.2896        | 0 (256fs)                     | 1   | 0   | 0   | 1   | 1                   |
|               |               | 16.9344        | 1 (384fs)                     | 1   | 0   | 0   | 1   |                     |
| 8<br>(Note 1) | 44.1          | 11.2896        | 0 (256fs)                     | 1   | 0   | 1   | 0   | 1                   |
|               |               | 16.9344        | 1 (384fs)                     | 1   | 0   | 1   | 0   |                     |
| 8<br>(Note 1) | 8<br>(Note 1) | 11.2896        | 0 (256fs)                     | 1   | 0   | 1   | 1   | 1                   |
|               |               | 16.9344        | 1 (384fs)                     | 1   | 0   | 1   | 1   |                     |
| 88.2          | 88.2          | 11.2896        | 0 (128fs)                     | 1   | 1   | 1   | 1   | 2                   |
|               |               | 16.9344        | 1 (192fs)                     | 1   | 1   | 1   | 1   |                     |

Table 10 Normal Mode Sample Rate Look-up Table

## Notes:

- 8k not exact, actual = 8.018kHz
- All other combinations of BOSR and SR[3:0] that are not in the truth table are invalid

The BOSR bit represents the base over-sampling rate. This is the rate that the WM8734 digital signal processing is carried out at. In Normal mode, with BOSR = 0, the base over-sampling rate is at 256fs, with BOSR = 1, the base over-sampling rate is at 384fs. This can be used to determine the actual audio data rate produced by the ADC and required by the DAC.

Example scenarios are:

- with a requirement that the ADC data rate is 8kHz and DAC data rate is 48kHz, then choosing MCLK = 12.288MHz the device is programmed with BOSR = 0 (256fs), SR3 = 0, SR2 = 0, SR1 = 1, SR0 = 0. The ADC output data rate will then be exactly 8kHz (derived from 12.288MHz/256 x 1/6) and the DAC expects data at exactly 48kHz (derived from 12.288MHz/256)
- with a requirement that ADC data rate is 8kHz and DAC data rate is 44.1kHz, then choosing MCLK = 16.9344MHz the device is programmed with BOSR = 1 (384fs), SR3 = 1, SR2 = 0, SR1 = 0, SR0 = 1. The ADC will no longer output data at exactly 8.000kHz, instead it will be 8.018kHz (derived from 16.9344MHz/384 x 2/11), the DAC still is at exactly 44.1kHz (derived from 16.9344MHz/384). A slight (sub 0.5%) pitch shift will therefore result in the 8kHz audio data and (importantly) the user must ensure that the data across the digital interface is correctly synchronised at the 8.018kHz rate.

The exact sample rates achieved are defined by the relationships in Table 11 below.

| TARGET SAMPLING RATE | ACTUAL SAMPLING RATE                       |   |  |   |
|----------------------|--|---|--|---|
|                      | BOSR=0                                     |   | BOSR=1                                     |   |
|                      | MCLK=12.288                                | MCLK=11.2896                                    | MCLK=18.432                                | MCLK=16.9344                                    |
| kHz                  | kHz  | kHz   | kHz  | kHz   |
| 8                    | 8<br><small>(12.288MHz/256) x 1/6</small>  | 8.018<br><small>(11.2896MHz/256) x 2/11</small> | 8<br><small>(18.432MHz/384) x 1/6</small>  | 8.018<br><small>(16.9344MHz/384) x 2/11</small> |
| 32                   | 32<br><small>(12.288MHz/256) x 2/3</small> | <i>not available</i>                            | 32<br><small>(18.432MHz/384) x 2/3</small> | <i>not available</i>                            |
| 44.1                 | <i>not available</i>                       | 44.1<br><small>11.2896MHz/256</small>           | <i>not available</i>                       | 44.1<br><small>16.9344MHz /384</small>          |
| 48                   | 48<br><small>12.288MHz/256</small>         | <i>not available</i>                            | 48<br><small>18.432MHz/384</small>         | <i>not available</i>                            |
| 88.2                 | <i>not available</i>                       | 88.2<br><small>(11.2896MHz/384) x 2</small>     | <i>not available</i>                       | 88.2<br><small>(16.9344MHz /384) x 2</small>    |
| 96                   | 96<br><small>(12.288MHz/256) x 2</small>   | <i>not available</i>                            | 96<br><small>(18.432MHz/384) x 2</small>   | <i>not available</i>                            |

Table 11 Normal Mode Actual Sample Rates

### 128/192fs NORMAL MODE

The Normal Mode sample rates are designed for standard 256fs and 384fs MCLK rates. However the WM8734 is also capable of being clocked from a 128 or 192fs MCLK for application over limited sampling rates as shown in the table below.

| SAMPLING RATE |      | MCLK FREQUENCY | SAMPLE RATE REGISTER SETTINGS |     |     |     |     | DIGITAL FILTER TYPE |
|---------------|------|----------------|-------------------------------|-----|-----|-----|-----|---------------------|
| ADC           | DAC  |                | BOSR                          | SR3 | SR2 | SR1 | SR0 |                     |
| kHz           | kHz  | MHz            |                               |     |     |     |     |                     |
| 48            | 48   | 6.144          | 0                             | 0   | 1   | 1   | 1   | 2                   |
|               |      | 9.216          | 1                             | 0   | 1   | 1   | 1   |                     |
| 44.1          | 44.1 | 5.6448         | 0                             | 1   | 1   | 1   | 1   | 2                   |
|               |      | 8.4672         | 1                             | 1   | 1   | 1   | 1   |                     |

Table 12 128fs Normal Mode Sample Rate Look-up Table

### 512/768fs NORMAL MODE

512 fs and 768 fs MCLK rates can be accommodated by using the CLKIDIV2 bit. The core clock to the DSP will be divided by 2 so an external 512/768 MCLK will become 256/384 fs internally and the device otherwise operates as in Table 8 but with MCLK at twice the specified rate. See Table 6 for software control.

### USB MODE SAMPLE RATES

In USB mode the MCLK/crystal oscillator input is 12MHz only.

| SAMPLING RATE    |                  | MCLK FREQUENCY | SAMPLE RATE REGISTER SETTINGS |     |     |     |     | DIGITAL FILTER TYPE |
|------------------|------------------|----------------|-------------------------------|-----|-----|-----|-----|---------------------|
| ADC              | DAC              |                | BOSR                          | SR3 | SR2 | SR1 | SR0 |                     |
| 48               | 48               | 12.000         | 0                             | 0   | 0   | 0   | 0   | 0                   |
| 44.1<br>(Note 2) | 44.1<br>(Note 2) | 12.000         | 1                             | 1   | 0   | 0   | 0   | 1                   |
| 48               | 8                | 12.000         | 0                             | 0   | 0   | 0   | 1   | 0                   |
| 44.1<br>(Note 2) | 8<br>(Note 1)    | 12.000         | 1                             | 1   | 0   | 0   | 1   | 1                   |
| 8                | 48               | 12.000         | 0                             | 0   | 0   | 1   | 0   | 0                   |
| 8<br>(Note 1)    | 44.1<br>(Note 2) | 12.000         | 1                             | 1   | 0   | 1   | 0   | 1                   |
| 8                | 8                | 12.000         | 0                             | 0   | 0   | 1   | 1   | 0                   |
| 8<br>(Note 1)    | 8<br>(Note 1)    | 12.000         | 1                             | 1   | 0   | 1   | 1   | 1                   |
| 32               | 32               | 12.000         | 0                             | 0   | 1   | 1   | 0   | 0                   |
| 96               | 96               | 12.000         | 0                             | 0   | 1   | 1   | 1   | 3                   |
| 88.2<br>(Note 3) | 88.2<br>(Note 3) | 12.000         | 1                             | 1   | 1   | 1   | 1   | 2                   |

**Table 13 USB Mode Sample Rate Look-up Table**

#### Notes:

- 8k not exact, actual = 8.021kHz
- 44.1k not exact, actual = 44.118kHz
- 88.1k not exact, actual = 88.235kHz
- All other combinations of BOSR and SR[3:0] that are not in the truth table are invalid

The table above can be used to set up the device to work with various sample rate combinations. For example if the user wishes to use the WM8734 in USB mode with the ADC and DAC sample rates at 48kHz and 48kHz respectively then the device should be programmed with BOSR = 0, SR3 = 0, SR2 = 0, SR1 = 0 and SR0 = 0. The ADC and DAC will then operate with a Digital Filter of type 0, refer to Digital Filter Characteristics section for an explanation of the different filter types.

The BOSR bit represents the base over-sampling rate. This is the rate that the WM8734 digital signal processing is carried out at and the sampling rate will always be a sub-multiple of this. In USB mode, with BOSR = 0, the base over-sampling rate is defined at 250fs, with BOSR = 1, the base over-sampling rate is defined at 272fs. This can be used to determine the actual audio sampling rate produced by the ADC and required by the DAC.

Example scenarios are, :-

- with a requirement that the ADC data sampling rate is 8kHz and DAC data sampling rate is 48kHz the device is programmed with BOSR = 0 (250fs), SR3 = 0, SR2 = 0, SR1 = 1, SR0 = 0. The ADC will then be exactly 8kHz ( derived from  $12\text{MHz}/250 \times 1/6$  ) and the DAC expects data at exactly 48kHz ( derived from  $12\text{MHz}/250$  ).
- with a requirement that ADC data rate is 8kHz and DAC data rate is 44.1kHz the device is programmed with BOSR = 0 (272fs), SR3 = 0, SR2 = 0, SR1 = 1, SR0 = 0. The ADC will not output data at exactly 8kHz, instead it will be 8.021kHz ( derived from  $12\text{MHz}/272 \times 2/11$  ) and the DAC at 44.118kHz ( derived from  $12\text{MHz}/272$  ). A slight (sub 0.5%) pitch shift will therefore results in the 8kHz and 44.1kHz audio data and ( more importantly ) the user must ensure that

the data across the digital interface is correctly synchronised at the 8.021kHz and 44.117kHz rates.

The exact sample rates supported for all combinations are defined by the relationships in Table 14 below.

| TARGET SAMPLING RATE | ACTUAL SAMPLING RATE |                      |
|----------------------|----------------------|----------------------|
|                      | BOSR=0<br>(250fs)    | BOSR=1<br>(272fs)    |
| kHz                  | kHz                  | kHz                  |
| 8                    | 8                    | 8.021                |
|                      | 12MHz/(250 x 48/8)   | 12MHz/(272 x 11/2)   |
| 32                   | 32                   | <i>not available</i> |
|                      | 12MHz/(250 x 48/32)  |                      |
| 44.1                 | <i>not available</i> | 44.117               |
|                      |                      | 12MHz/272            |
| 48                   | 48                   | <i>not available</i> |
|                      | 12MHz/250            |                      |
| 88.2                 | <i>not available</i> | 88.235               |
|                      |                      | 12MHz/136            |
| 96                   | 96                   | <i>not available</i> |
|                      | 12MHz/125            |                      |

Table 14 USB Mode Actual Sample Rates

## ACTIVATING DSP AND DIGITAL AUDIO INTERFACE

To prevent any communication problems from arising across the Digital Audio Interface the Audio Interface is disabled (tristate with weak 100k pulldown). Once the Audio Interface and the Sampling Control has been programmed it is activated by setting the ACTIVE bit under Software Control.

| REGISTER ADDRESS          | BIT | LABEL  | DEFAULT | DESCRIPTION                                      |
|---------------------------|-----|--------|---------|--|
| 0001001<br>Active Control | 0   | ACTIVE | 0       | Activate Interface<br>1 = Active<br>0 = Inactive |

Table 15 Activating DSP and Digital Audio Interface

It is recommended that between changing any content of Digital Audio Interface or Sampling Control Register that the active bit is reset then set.

## SOFTWARE CONTROL INTERFACE

The software control interface may be operated using either a 3-wire (SPI-compatible) or 2-wire MPU interface. Selection of interface format is achieved by setting the state of the MODE pin.

In 3-wire mode, SDIN is used for the program data, SCLK is used to clock in the program data and CSB is used to latch in the program data. In 2-wire mode, SDIN is used for serial data and SCLK is used for the serial clock. In 2-wire mode, the state of CSB pin allows the user to select one of two addresses.

Unused register bits should always be set to '0' unless specified otherwise.

### SELECTION OF SERIAL CONTROL MODE

The serial control interface may be selected to operate in either 2 or 3-wire modes. This is achieved by setting the state of the MODE pin.

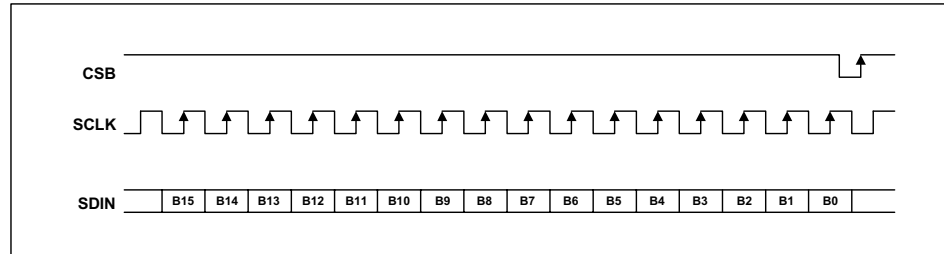
| MODE | INTERFACE FORMAT |
|------|------------------|
| 0    | 2 wire           |
| 1    | 3 wire           |

Table 16 Control Interface Mode Selection



**3-WIRE (SPI COMPATIBLE) SERIAL CONTROL MODE**

The WM8734 can be controlled using a 3-wire serial interface. SDIN is used for the program data, SCLK is used to clock in the program data and CSB is use to latch in the program data. The 3-wire interface protocol is shown in Figure 23.



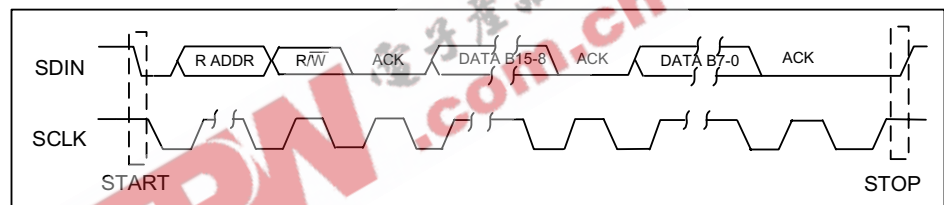
**Figure 23 3-Wire Serial Interface**

**Notes:**

1. B[15:9] are Control Address Bits
2. B[8:0] are Control Data Bits

**2-WIRE SERIAL CONTROL MODE**

The WM8734 supports a 2-wire MPU serial interface. The device operates as a slave device only. The WM8734 has one of two slave addresses that are selected by setting the state of pin 10, (CSB).



**Figure 24 2-Wire Serial Interface**

**Notes:**

1. B[15:9] are Control Address Bits
2. B[8:0] are Control Data Bits

| CSB STATE<br>(Default = LOW) | Address |
|------------------------------|---------|
| 0                            | 0011010 |
| 1                            | 0011011 |

**Table 17 2-Wire MPU Interface Address Selection**

To control the WM8734 on the 2-wire bus the master control device must initiate a data transfer by establishing a start condition, defined by a high to low transition on SDIN while SCLK remains high. This indicates that an address and data transfer will follow. All peripherals on the 2-wire bus respond to the start condition and shift in the next eight bits (7-bit address + R/W bit). The transfer is MSB first. The 7-bit address consists of a 6-bit base address + a single programmable bit to select one of two available addresses for this device (see table 24). If the correct address is received and the R/W bit is '0', indicating a write, then the WM8734 will respond by pulling SDIN low on the next clock pulse (ACK). The WM8734 is a write only device and will only respond to the R/W bit indicating a write. If the address is not recognised the device will return to the idle condition and wait for a new start condition and valid address.

Once the WM8734 has acknowledged a correct address, the controller will send eight data bits (bits B[15]-B[8]). WM8734 will then acknowledge the sent data by pulling SDIN low for one clock pulse. The controller will then send the remaining eight data bits (bits B[7]-B[0]) and the WM8734 will then acknowledge again by pulling SDIN low.

A stop condition is defined when there is a low to high transition on SDIN while SCLK is high. If a start or stop condition is detected out of sequence at any point in the data transfer then the device will jump to the idle condition.

After receiving a complete address and data sequence the WM8734 returns to the idle state and waits for another start condition. Each write to a register requires the complete sequence of start condition, device address and R/W bit followed by the 16 register address and data bits.

Note that the 16 bit control word is made up of 7 address bits, B[15:9], and 9 data bits, B[8:0]. These are transmitted as 2 blocks of 8 bits. The first block contains 7 address bits and the data HSB. The second block contains the 8 data LSBs.

## POWER DOWN MODES

The WM8734 contains power conservation modes in which various circuit blocks may be safely powered down in order to conserve power. This is software programmable as shown in the table below.

| REGISTER ADDRESS              | BIT | LABEL    | DEFAULT | DESCRIPTION   |
|-------------------------------|-----|----------|---------|---|
| 0000110<br>Power Down Control | 0   | LINEINPD | 1       | Line Input Power Down<br>1 = Enable Power Down<br>0 = Disable Power Down  |
|                               | 2   | ADCPD    | 1       | ADC Power Down<br>1 = Enable Power Down<br>0 = Disable Power Down         |
|                               | 3   | DACPD    | 1       | DAC Power Down<br>1 = Enable Power Down<br>0 = Disable Power Down         |
|                               | 4   | OUTPD    | 1       | Line Output Power Down<br>1 = Enable Power Down<br>0 = Disable Power Down |
|                               | 7   | POWEROFF | 1       | Power Off Device<br>1 = Device Power Off<br>0 = Device Power On           |

**Table 18 Power Conservation Modes Software Control**

When writing to the powerdown register bits 1,5 and 6 should be set to '1'.

The power down control can be used to either a) permanently disable functions when not required in certain applications or b) to dynamically power up and down functions depending on the operating mode, e.g.: during playback or record. Please follow the special instructions below if dynamic implementations are being used.

**LINEINPD:** Simultaneously powers down both the Line Inputs. This can be done dynamically without any audible effects either on the ADC or to the Line Outputs in Bypass mode. This is of use when the device enters Playback, Pause or Stop modes or the Microphone input has been selected.

**ADCPD:** Powers down the ADC and ADC Filters. If this is done dynamically then audible pops will result if any signals were present through the ADC. To overcome this whenever the ADC is to be powered down, either mute the Microphone Input (MUTEIN) or MUTELINEIN, then change ADCPD. This is of use when the device enters Playback, Pause or Stop modes regardless of whether Microphone or Line Inputs are selected.

**DACPD:** Powers down the DAC and DAC Digital Filters. If this is done dynamically then audible pops will result unless the following guidelines are followed. In order to prevent pops, the DAC should first be soft-muted (DACMU), the output should then be de-selected from the line and headphone output (DACSEL), then the DAC powered down (DACPD). This is of use when the device enters Record, Pause, Stop or Bypass modes.

The device can be put into a standby mode (STANDBY) by powering down all the audio circuitry under software control as shown in Table 18. Provision has been made to independently power off these areas according to Table 19.

| POWER OFF | DACPD | ADCPD | LINEINPD | OUTPD | DESCRIPTION |
|-----------|-------|-------|----------|-------|-------------|
| 0         | 1     | 1     | 1        | 1     | STANDBY     |

Table 19 Standby Mode

In STANDBY mode the Control Interface, a small portion of the digital and areas of the analogue circuitry remain active. The active analogue includes the analogue VMID reference so that the analogue line inputs, line outputs and headphone outputs remain biased to VMID. This reduces any audible effects caused by DC glitches when entering or leaving STANDBY mode.

The device can be powered off by writing to the POWEROFF bit of the Power Down register. In POWEROFF mode the Control Interface and a small portion of the digital remain active. The analogue VMID reference is disabled.

| POWER OFF | DACPD | ADCPD | LINEINPD | OUTPD | DESCRIPTION |
|-----------|-------|-------|----------|-------|-------------|
| 1         | X     | X     | X        | X     | POWEROFF    |

Table 20 Poweroff Mode

## REGISTER MAP

The complete register map is shown in Table 21. The detailed description can be found in the relevant text of the device description. There are 8 registers with 9 bits per register. These can be controlled using either the 2 wire or 3 wire MPU interface.

| REGISTER ADDRESS                       | BIT | LABEL       | DEFAULT          | DESCRIPTION   |
|--|-----|-------------|------------------|---|
| 0000000<br>Left Line In                | 4:0 | LINVOL[4:0] | 10111<br>( 0dB ) | Left Channel Line Input Volume Control<br>11111 = +12dB . . 1.5dB steps down to 00000 = -34.5dB   |
|  | 7   | LINMUTE     | 1                | Left Channel Line Input Mute to ADC<br>1 = Enable Mute<br>0 = Disable Mute  |
|  | 8   | LRINBOTH    | 0                | Left to Right Channel Line Input Volume and Mute Data Load Control<br>1 = Enable Simultaneous Load of LINVOL[4:0] and LINMUTE to RINVOL[4:0] and RINMUTE<br>0 = Disable Simultaneous Load |
| 0000001<br>Right Line In               | 4:0 | RINVOL[4:0] | 10111<br>( 0dB ) | Right Channel Line Input Volume Control<br>11111 = +12dB . . 1.5dB steps down to 00000 = -34.5dB  |
|  | 7   | RINMUTE     | 1                | Right Channel Line Input Mute to ADC<br>1 = Enable Mute<br>0 = Disable Mute   |
|  | 8   | RLINBOTH    | 0                | Right to Left Channel Line Input Volume and Mute Data Load Control<br>1 = Enable Simultaneous Load of RINVOL[4:0] and RINMUTE to LINVOL[4:0] and LINMUTE<br>0 = Disable Simultaneous Load |
| 0000100<br>Analogue Audio Path Control | 4   | DACSEL      | 0                | DAC Select<br>1 =Select DAC<br>0 = Don't select DAC   |
| 0000101<br>Digital Audio Path Control  | 0   | ADCHPD      | 0                | ADC High Pass Filter Enable<br>1 = Enable High Pass Filter<br>0 = Disable High Pass Filter  |
|  | 2:1 | DEEMP[1:0]  | 00               | De-emphasis Control<br>11 = 48kHz<br>10 = 44.1kHz<br>01 = 32kHz<br>00 = Disable   |
|  | 3   | DACMU       | 1                | DAC Soft Mute Control<br>1 = Enable soft mute<br>0 = Disable soft mute  |
|  | 4   | HPOR        | 0                | Store dc offset when High Pass Filter disabled<br>1 = store offset<br>0 = clear offset  |

| REGISTER ADDRESS                          | BIT | LABEL       | DEFAULT | DESCRIPTION  |
|---|-----|-------------|---------|--|
| 0000110<br>Power Down Control             | 0   | LINEINPD    | 1       | Line Input Power Down<br>1 = Enable Power Down<br>0 = Disable Power Down   |
|   | 2   | ADCPD       | 1       | ADC Power Down<br>1 = Enable Power Down<br>0 = Disable Power Down  |
|   | 3   | DACPD       | 1       | DAC Power Down<br>1 = Enable Power Down<br>0 = Disable Power Down  |
|   | 4   | OUTPD       | 1       | Line Output Power Down<br>1 = Enable Power Down<br>0 = Disable Power Down  |
|   | 7   | POWEROFF    | 1       | POWEROFF mode<br>1 = Enable POWEROFF<br>0 = Disable POWEROFF   |
| 0000111<br>Digital Audio Interface Format | 1:0 | FORMAT[1:0] | 10      | Audio Data Format Select<br>11 = DSP Mode, frame sync + 2 data packed words<br>10 = I <sup>2</sup> S Format, MSB-First left-1 justified<br>01 = MSB-First, left justified<br>00 = MSB-First, right justified   |
|   | 3:2 | IWL[1:0]    | 10      | Input Audio Data Bit Length Select<br>11 = 32 bits<br>10 = 24 bits<br>01 = 20 bits<br>00 = 16 bits   |
|   | 4   | LRP         | 0       | DACLRC phase control (in left, right or I <sup>2</sup> S modes)<br>1 = Right Channel DAC data when DACLRC high<br>0 = Right Channel DAC data when DACLRC low (opposite phasing in I <sup>2</sup> S mode)<br>or<br>DSP mode A/B select (in DSP mode only)<br>1 = MSB is available on 2nd BCLK rising edge after ADCLRC/DACLRC rising edge<br>0 = MSB is available on 1st BCLK rising edge after ADCLRC/DACLRC rising edge |
|   | 5   | LRSWAP      | 0       | DAC Left Right Clock Swap<br>1 = Right Channel DAC Data Left<br>0 = Right Channel DAC Data Right   |
|   | 6   | MS          | 0       | Master Slave Mode Control<br>1 = Enable Master Mode<br>0 = Enable Slave Mode   |
|   | 7   | BCLKINV     | 0       | Bit Clock Invert<br>1 = Invert BCLK<br>0 = Don't invert BCLK   |

| REGISTER ADDRESS            | BIT | LABEL          | DEFAULT | DESCRIPTION  |
|-----------------------------|-----|----------------|---------|--|
| 0001000<br>Sampling Control | 0   | USB/<br>NORMAL | 0       | Mode Select<br>1 = USB mode (250/272fs)<br>0 = Normal mode (256/384fs)                     |
|                             | 1   | BOSR           | 0       | Base Over-Sampling Rate<br>0 = 256fs<br>1 = 384fs  |
|                             | 5:2 | SR[3:0]        | 0000    | ADC and DAC sample rate control  |
|                             | 6   | CLKIDIV2       | 0       | Core Clock divider select<br>1 = Core Clock is MCLK divided by 2<br>0 = Core Clock is MCLK |
| 0001001<br>Active Control   | 0   | ACTIVE         | 0       | Activate Interface<br>1 = Active<br>0 = Inactive   |

Table 21 Register Map Description

**Note:**

Unused register bits should be set to '0' except when writing to Register 0000110, when bits 1,5 and 6 should be set to '1'.

**DIGITAL FILTER CHARACTERISTICS**

The ADC and DAC employ different digital filters. There are 4 types of digital filter, called Type 0, 1, 2 and 3. The performance of Types 0 and 1 is listed in the table below, the responses of all filters is shown in the proceeding pages.

| PARAMETER   | TEST CONDITIONS | MIN      | TYP   | MAX      | UNIT |
|---|-----------------|----------|-------|----------|------|
| <b>ADC Filter Type 0 (USB Mode, 250fs operation)</b>                |                 |          |       |          |      |
| Passband  | +/- 0.05dB      | 0        |       | 0.416fs  |      |
|   | -6dB            |          | 0.5fs |          |      |
| Passband Ripple   |                 |          |       | +/- 0.05 | dB   |
| Stopband  |                 | 0.584fs  |       |          |      |
| Stopband Attenuation  | f > 0.584fs     | -60      |       |          | dB   |
| <b>ADC Filter Type 1 (USB mode, 272fs or Normal mode operation)</b> |                 |          |       |          |      |
| Passband  | +/- 0.05dB      | 0        |       | 0.4535fs |      |
|   | -6dB            |          | 0.5fs |          |      |
| Passband Ripple   |                 |          |       | +/- 0.05 | dB   |
| Stopband  |                 | 0.5465fs |       |          |      |
| Stopband Attenuation  | f > 0.5465fs    | -60      |       |          | dB   |
| High Pass Filter Corner Frequency                                   | -3dB            |          | 3.7   |          | Hz   |
|   | -0.5dB          |          | 10.4  |          |      |
|   | -0.1dB          |          | 21.6  |          |      |
| <b>DAC Filter Type 0 (USB mode, 250fs operation)</b>                |                 |          |       |          |      |
| Passband  | +/- 0.03dB      | 0        |       | 0.416fs  |      |
|   | -6dB            |          | 0.5fs |          |      |
| Passband Ripple   |                 |          |       | +/-0.03  | dB   |
| Stopband  |                 | 0.584fs  |       |          |      |
| Stopband Attenuation  | f > 0.584fs     | -50      |       |          | dB   |
| <b>DAC Filter Type 1 (USB mode, 272fs or Normal mode operation)</b> |                 |          |       |          |      |
| Passband  | +/- 0.03dB      | 0        |       | 0.4535fs |      |
|   | -6dB            |          | 0.5fs |          |      |
| Passband Ripple   |                 |          |       | +/- 0.03 | dB   |
| Stopband  |                 | 0.5465fs |       |          |      |
| Stopband Attenuation  | f > 0.5465fs    | -50      |       |          | dB   |

Table 22 Digital Filter Characteristics

**TERMINOLOGY**

1. Stop Band Attenuation (dB) - the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

**DAC FILTER RESPONSES**

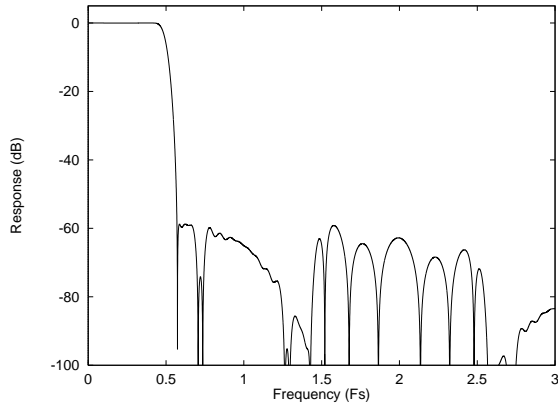


Figure 25 DAC Digital Filter Frequency Response –Type 1

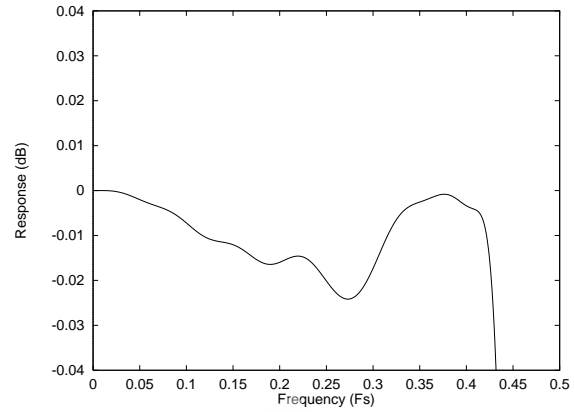


Figure 26 DAC Digital Filter Ripple –Type 1

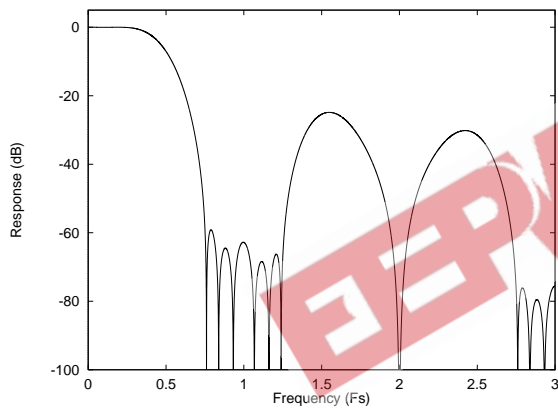


Figure 27 DAC Digital Filter Frequency Response –Type 2

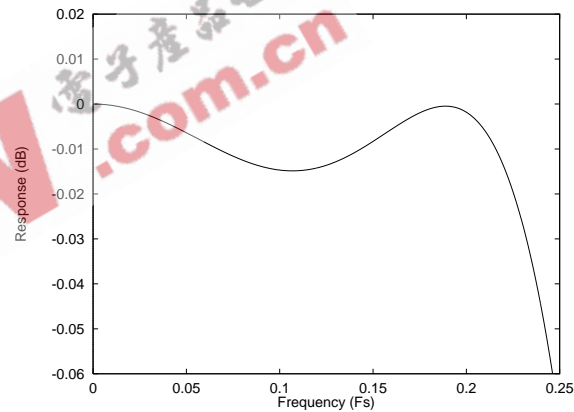


Figure 28 DAC Digital Filter Ripple –Type 2

**ADC FILTER RESPONSES**

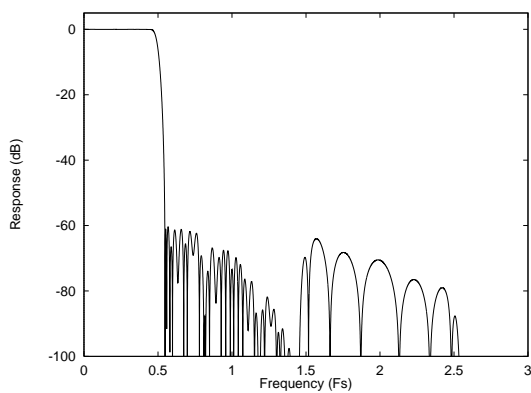


Figure 29 ADC Digital Filter Frequency Response –Type 1

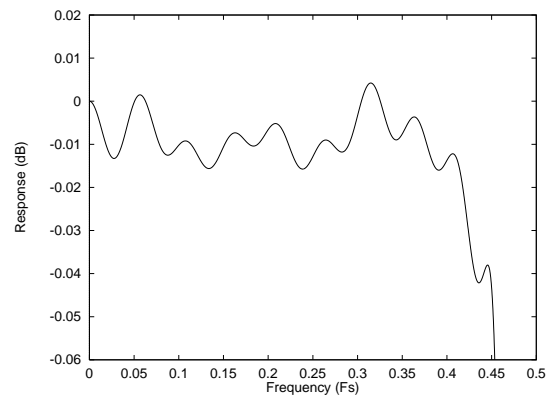


Figure 30 ADC Digital Filter Ripple –Type 1

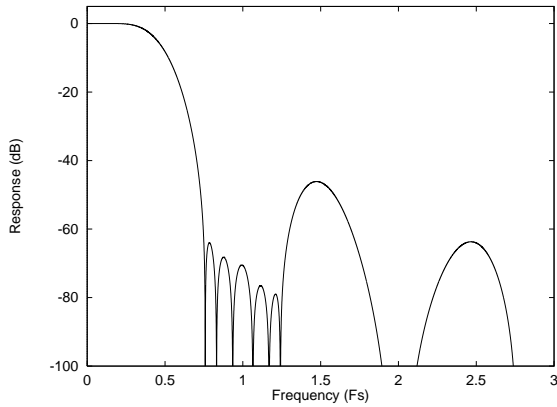


Figure 31 ADC Digital Filter Frequency Response –Type 2

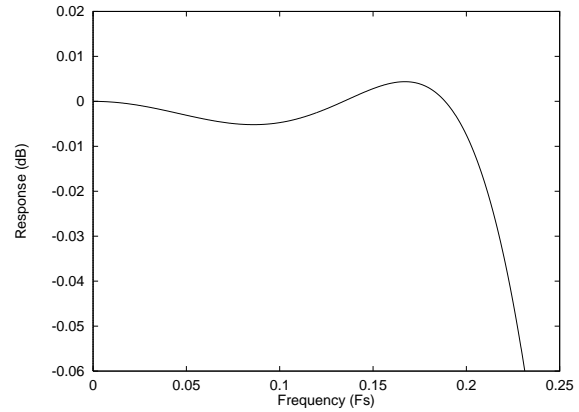


Figure 32 ADC Digital Filter Ripple –Type 2

### ADC HIGH PASS FILTER

The WM8734 has a selectable digital high pass filter to remove DC offsets. The filter response is characterised by the following polynomial.

$$H(z) = \frac{1 - z^{-1}}{1 - 0.9995 z^{-1}}$$

### DIGITAL DE-EMPHASIS CHARACTERISTICS

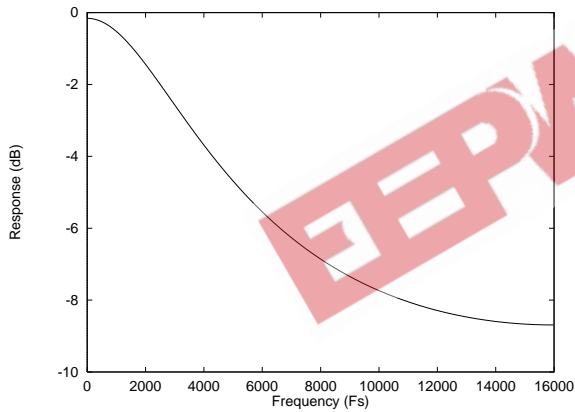


Figure 33 De-Emphasis Frequency Response (32kHz)

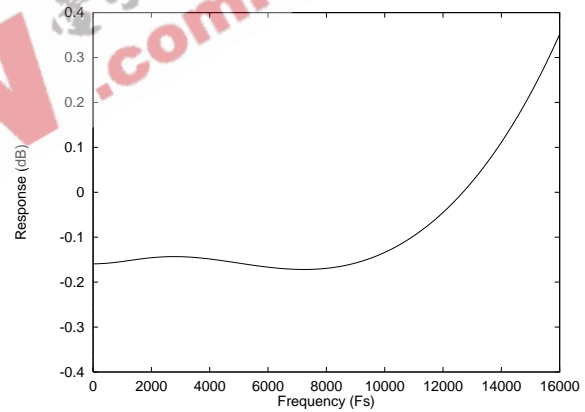


Figure 34 De-Emphasis Error (32kHz)

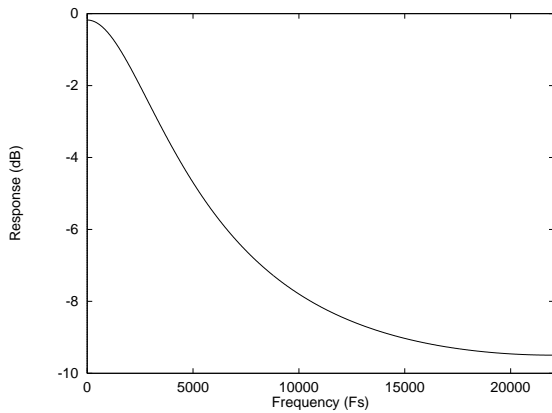


Figure 35 De-Emphasis Frequency Response (44.1kHz)

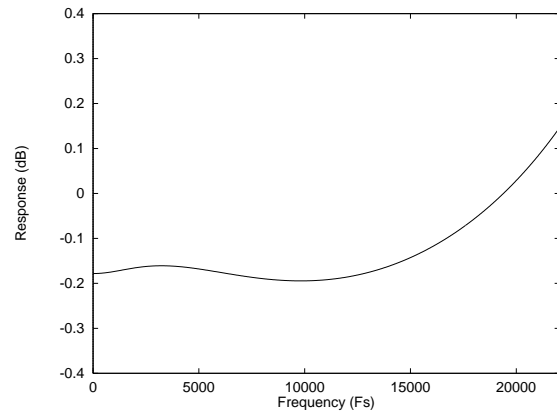


Figure 36 De-Emphasis Error (44.1kHz)



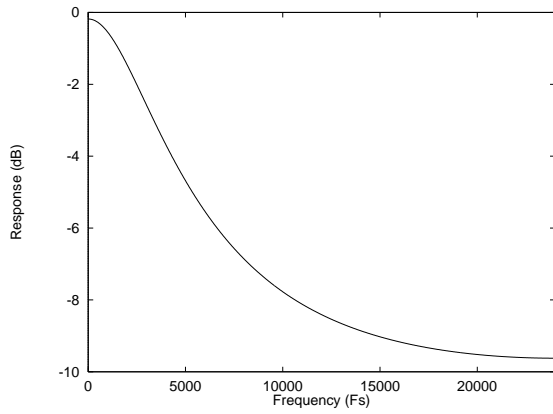


Figure 37 De-Emphasis Frequency Response (48kHz)

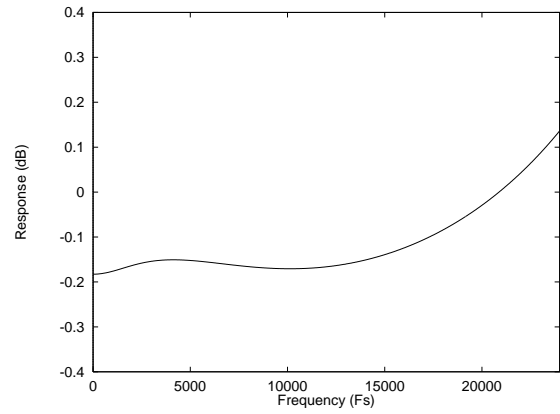


Figure 38 De-Emphasis Error (48kHz)

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## MINIMISING POP NOISE AT THE ANALOGUE OUTPUTS

To minimise any pop or click noise when the system is powered up or down, the following procedures are recommended.

### POWER UP SEQUENCE

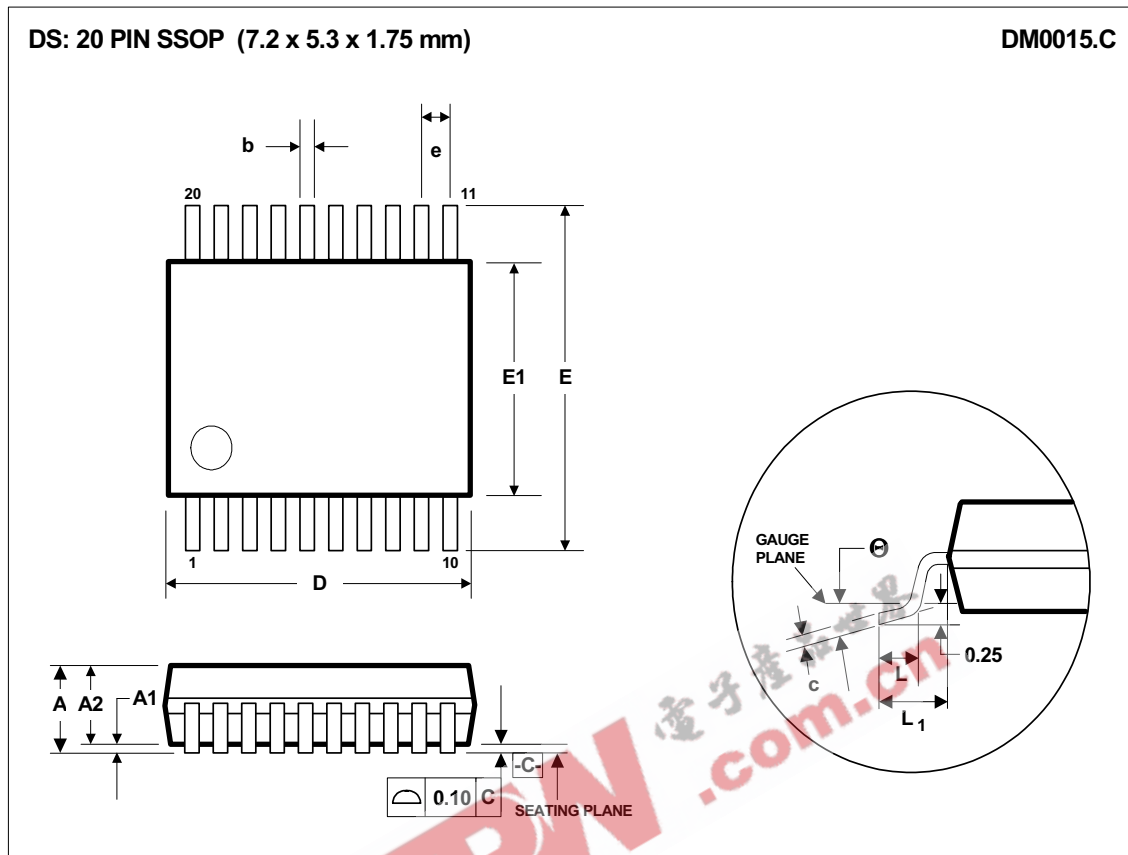
- Switch on power supplies. By default the WM8734 is in Standby Mode, the DAC is digitally muted and the Audio Interface and Outputs are all OFF.
- Set all required bits in the Power Down register (0Ch) to '0'; EXCEPT the OUTPD bit, this should be set to '1' (Default).
- Set required values in all other registers except 12h (Active).
- Set the 'Active' bit in register 12h.
- The last write of the sequence should be setting OUTPD to '0' (active) in register 0Ch, enabling the DAC signal path, free of any significant power-up noise.

### POWER DOWN SEQUENCE

- Set the OUTPD bit to '1' (power down).
- Remove the WM8734 supplies.

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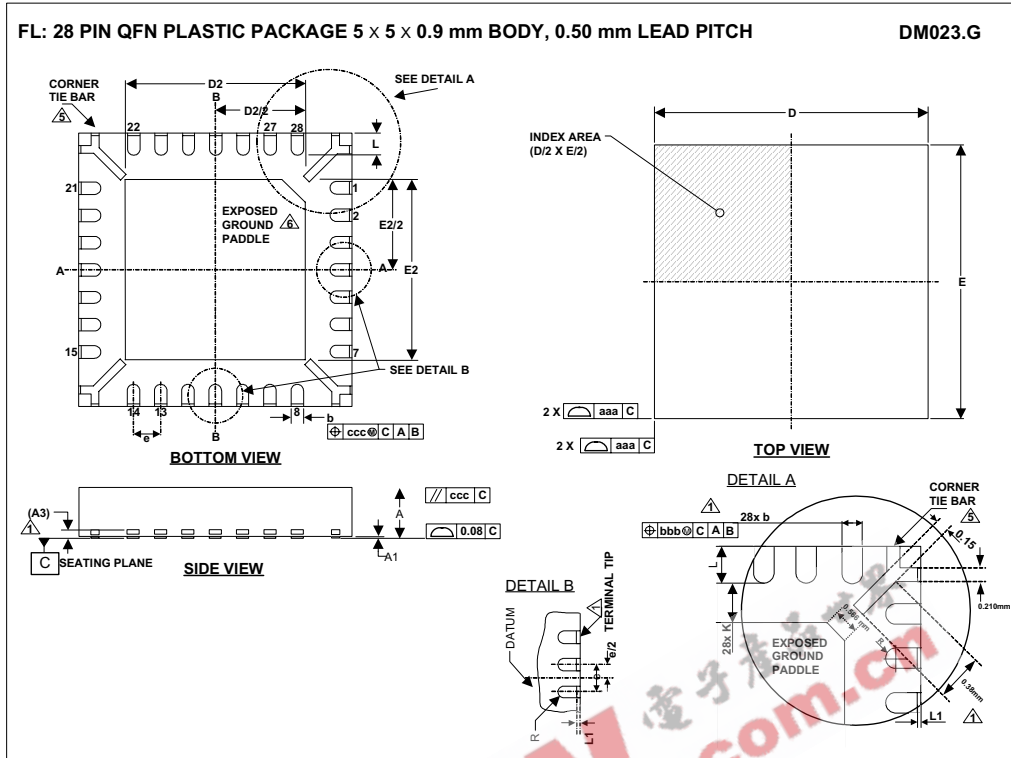
PACKAGE DIMENSIONS (SSOP)



| Symbols              | Dimensions (mm)  |       |       |
|----------------------|------------------|-------|-------|
|                      | MIN              | NOM   | MAX   |
| <b>A</b>             | -----            | ----- | 2.0   |
| <b>A<sub>1</sub></b> | 0.05             | ----- | ----- |
| <b>A<sub>2</sub></b> | 1.65             | 1.75  | 1.85  |
| <b>b</b>             | 0.22             | 0.30  | 0.38  |
| <b>c</b>             | 0.09             | ----- | 0.25  |
| <b>D</b>             | 6.90             | 7.20  | 7.50  |
| <b>e</b>             | 0.65 BSC         |       |       |
| <b>E</b>             | 7.40             | 7.80  | 8.20  |
| <b>E<sub>1</sub></b> | 5.00             | 5.30  | 5.60  |
| <b>L</b>             | 0.55             | 0.75  | 0.95  |
| <b>L<sub>1</sub></b> | 1.25 REF         |       |       |
| <b>θ</b>             | 0°               | 4°    | 8°    |
| <b>REF:</b>          | JEDEC.95, MO-150 |       |       |

- NOTES:
- A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
  - B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
  - C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
  - D. MEETS JEDEC.95 MO-150, VARIATION = AE. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

PACKAGE DIMENSIONS (QFN)



| Symbols                                | Dimensions (mm)                 |          |      | NOTE |
|--|---------------------------------|----------|------|------|
|  | MIN                             | NOM      | MAX  |      |
| A                                      | 0.85                            | 0.90     | 1.00 |      |
| A1                                     | 0                               | 0.02     | 0.05 |      |
| A3                                     |                                 | 0.2 REF  |      |      |
| b                                      | 0.18                            | 0.23     | 0.30 | 1    |
| D                                      |                                 | 5.00 BSC |      |      |
| D2                                     | 3.2                             | 3.3      | 3.4  | 2    |
| E                                      |                                 | 5.00 BSC |      |      |
| E2                                     | 3.2                             | 3.3      | 3.4  | 2    |
| e                                      |                                 | 0.5 BSC  |      |      |
| L                                      | 0.35                            | 0.4      | 0.45 |      |
| L1                                     |                                 |          | 0.1  | 1    |
| R                                      | b(min)/2                        |          |      |      |
| K                                      | 0.20                            |          |      |      |
| <b>Tolerances of Form and Position</b> |                                 |          |      |      |
| aaa                                    | 0.15                            |          |      |      |
| bbb                                    | 0.10                            |          |      |      |
| ccc                                    | 0.10                            |          |      |      |
| REF:                                   | JEDEC, MO-220, VARIATION VHHD-1 |          |      |      |

- NOTES:
- DIMENSION b APPLIED TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL PULL BACK FROM PACKAGE SIDE WALL. MAXIMUM OF 0.1mm IS ACCEPTABLE. WHERE TERMINAL PULL BACK EXISTS, ONLY UPPER HALF OF LEAD IS VISIBLE ON PACKAGE SIDE WALL DUE TO HALF ETCHING OF LEADFRAME.
  - FALLS WITHIN JEDEC, MO-220 WITH THE EXCEPTION OF D2, E2:
  - D2, E2: LARGER PAD SIZE CHOSEN WHICH IS JUST OUTSIDE JEDEC SPECIFICATION
  - ALL DIMENSIONS ARE IN MILLIMETRES
  - THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
  - SHAPE AND SIZE OF CORNER TIE BAR MAY VARY WITH PACKAGE TERMINAL COUNT. CORNER TIE BAR IS CONNECTED TO EXPOSED PAD INTERNALLY
  - REFER TO APPLICATION NOTE WAN\_0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.

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